R.G.B.Y. SWITCH UNIT UN9/544

Introduction

The UN9/544 accepts R, G, B and Y signals, and a feed of mixed-syncs. It provides a line-sequential output (see Fig. 1) which consists of one line-period of each of the input signals followed by a line period at blanking level. An auxiliary pulse output is provided at one-fifth of line-frequency for triggering an oscilloscope. Provision is made for any one of three d.c. components to be added to the output signal to facilitate multi-trace display.

The video inputs to the unit can be either composite or non-composite; where inputs are non-composite an optional connection is provided in the unit to permit mixed-syncs to be added to the output signal.

The UN9/544 consists of two printed-wiring boards mounted on a CH1/26B chassis with index peg positions 7 and 43. Power supplies at 12 volts and at 5·2 volts are derived from an integral mains-driven power supplier.

General Specification

Input-signal Amplitudes	
Composite video	1V p-p
Non-composite video	0·7V p-p
Mixed-syncs	2V p-p
Input Impedances	high w.r.t. 75 ohms
Output-signal Amplitudes	
Video	1V p-p
Trigger pulses	2V p-p
Output Impedances	75 ohms
Power Consumption	40 mA at 240V

Circuit Description

A block diagram of the unit is given in Fig. 2 and circuit diagrams of the two printed-wiring boards are given in Fig. 3 (Card B) and 4 (Card A).

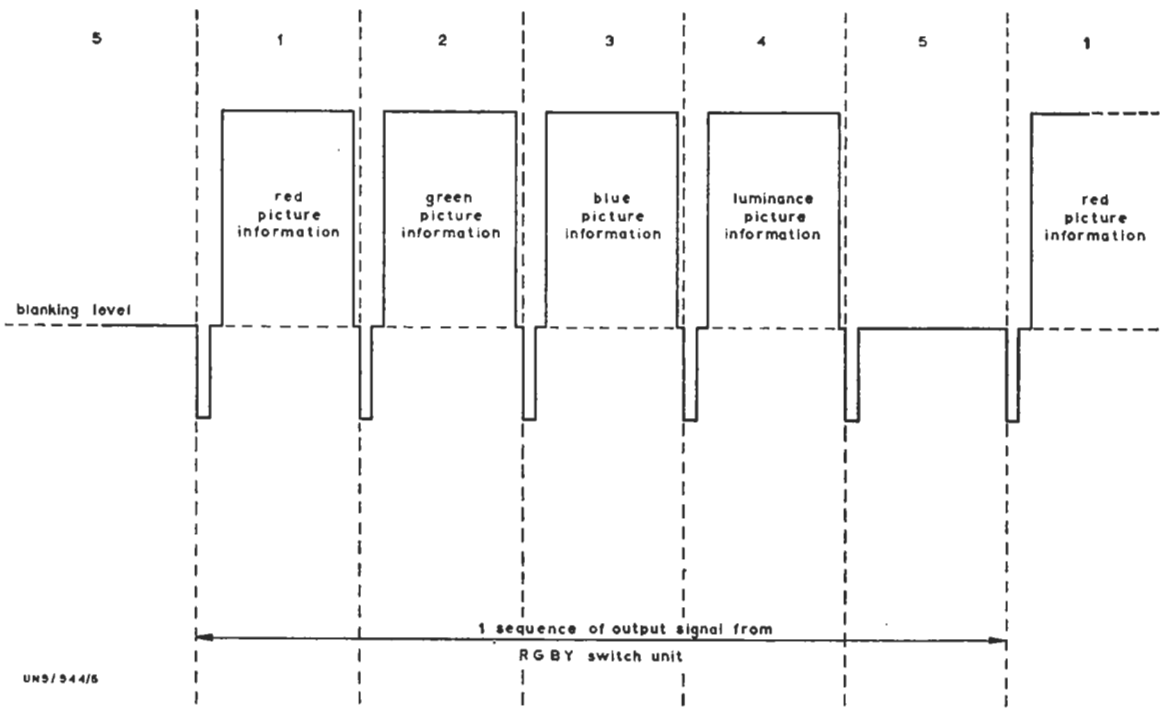


Fig. 1 Sequence of Component Elements in the Output Signal of the UN9/544

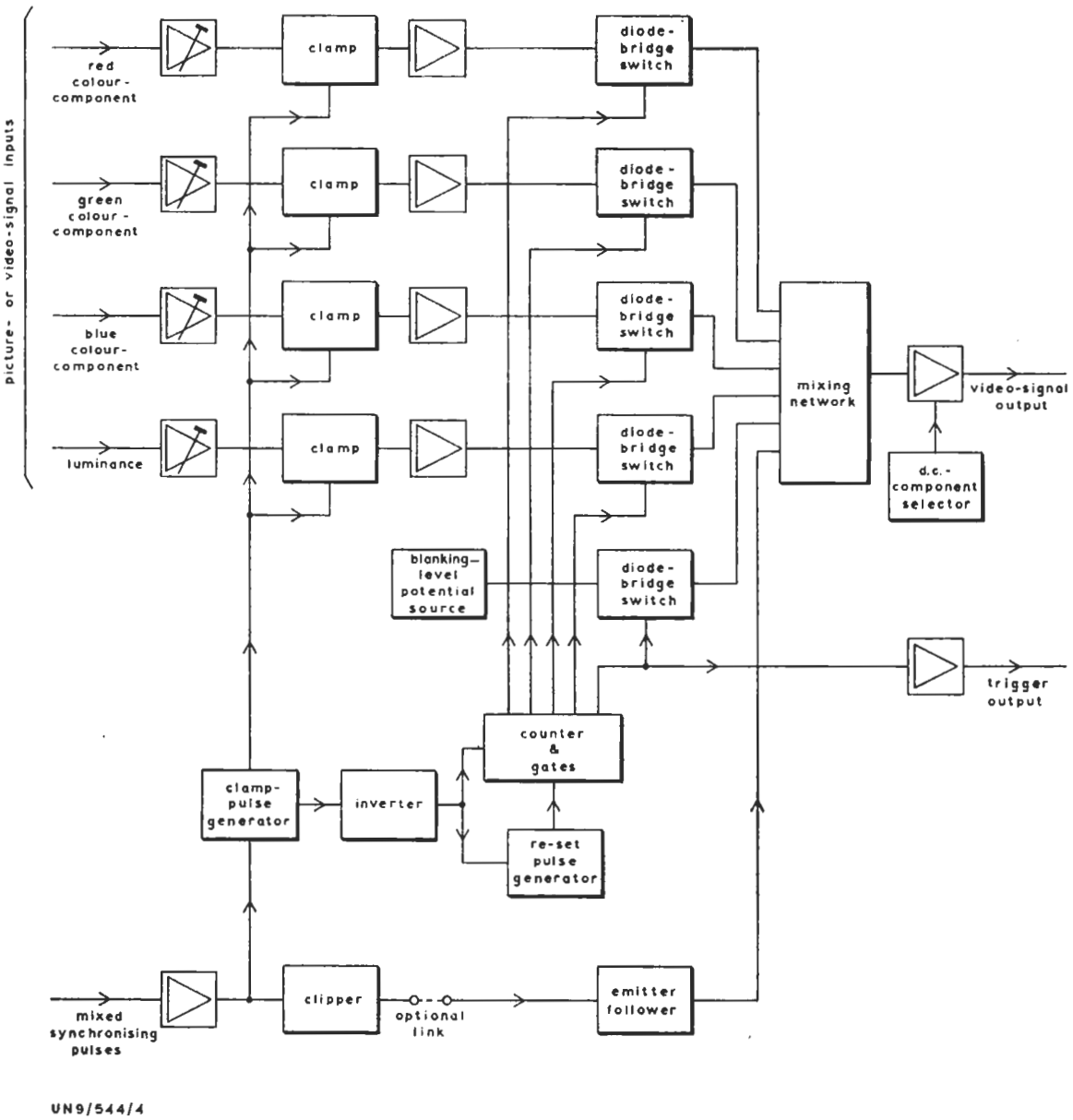


Fig. 2 Block Diagram of the RGBY Switch Unit UN9/544

input amplifiers | clamping | high input impedance amplifiers | switches | switch drives | clamping potential adjustments

red input (11) · green input (12) · luminance input (14) · blue input (13)

TR1 C111 · TR2 V405A · TR3 2N706A · TR4 2N706A · TR5 OC141 · TR6 OC141 · TR7 OC171 · TR8 2N706A · TR9 2N706A · TR10 2N706A · TR11 ASZ21

TR12 C111 · TR13 V405A · TR14 2N706A · TR15 2N706A · TR16 OC141 · TR17 OC141 · TR18 OC171 · TR19 2N706A · TR20 2N706A · TR21 2N706A · TR22 ASZ21

TR24 C111 · TR25 V405A · TR26 2N706A · TR27 2N706A · TR28 OC141 · TR29 OC141 · TR30 OC171 · TR31 2N706A · TR32 2N706A · TR33 2N706A · TR34 ASZ21

TR41 C111 · TR42 V405A · TR43 2N706A · TR44 2N706A · TR45 OC141 · TR46 OC141 · TR47 OC171 · TR48 2N706A · TR49 2N706A · TR50 2N706A · TR51 ASZ21

'A' / 'B' — clamping potential adjustments: P33 30k A01, R54 30k A01, R148 30k A01, R149 30k A01; R29, R30, R31, R32 470

from D19499A1 issue 4 parts list D19500 A4

emitter-follower: TR23 2N706A; R64 2k; R66 3k; R67 1·1k; R65 2·2k; R68 2·7k; syncs (8); 'A' (7), 'B' (9)

blanking level potential source: R99 560, C20 250, R100 27, R101 470, C22 100, C21 0·01

switch: D16–D19 AAZ 13

switch drive: R102 8·2k, R104 5·6k, R106 5·9k, R103 1·5k, C25 50, R105 470, R108 2·7k, R107 4·8k, TR35 2N706A, TR36 2N706A

trigger output amplifier: D20 AAZ13, R109 1·2k, C24 50, R110 51k, R112 4·7k, R115 220, R111 10k, R113 3·9k, R114 560, R147 33, R116 75, C26 50, TR37 ASZ21, TR38 2N706A, TR39 V405A, TR40 2N706A; (15), (10), (1)

blanking level switching pulse (1) · red switching pulse (2) · green switching pulse (3) · blue switching pulse (4) · luminance switching pulse (5) · to output amplifier (6)

Transistor terminations View on leads

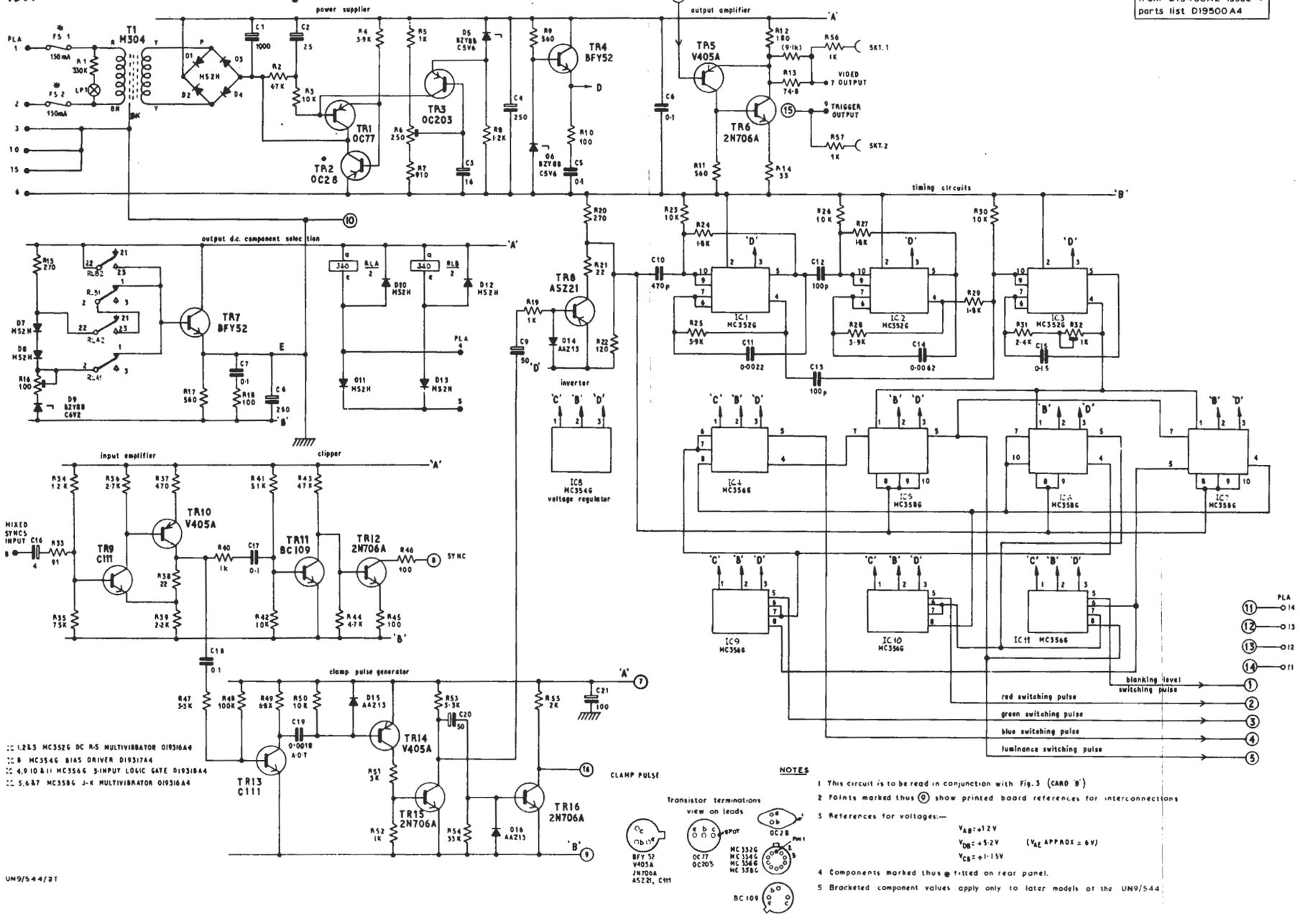
C111 · V405A · 2N706 · 2N706A · ASZ21 — OC171 — OC141 (dot)

Notes:
1. References for voltages:- V_{AB} = +12V (V_{AE} = 6V Approx)
2. Points marked thus (9) show printed board references or interconnections
3. This circuit is to be read in conjunction with Fig.4 (Card 'A')

UN9/544/3T

Fig.3 Circuit of Board B in RGBY Switch Unit UN9/544

from D19498A2 issue 4
parts list D19500A4



NOTES

1 This circuit is to be read in conjunction with Fig.3 (CARD 'B')

2 Points marked thus ⓪ show printed board references for interconnections

3 References for voltages:—

V_{AB} = +12V

V_{DB} = +5·2V (V_{AE} APPROX = 6V)

V_{CB} = +1·15V

4 Components marked thus * fitted on rear panel.

5 Bracketed component values apply only to later models of the UN9/544

Fig.4 Circuit of Board A in R.G.B.Y. Switch Unit UN9/544

Signal Path

The four incoming video signals are applied to similar input circuits (see Fig. 3), therefore only the red-signal circuit is described below.

The input signal is applied to a feedback amplifier comprising transistors TR1 and TR2; variable resistor R7 functions as a gain control. From the collector of TR2 the signal is fed to emitter-followers TR3 and TR4 whose outputs are coupled together by resistor R15. The signal is clamped at this point by the action of the synchronous-switch transistors TR5 and TR6. The low-pass filter formed by R15 and C3 is interposed in the clamping path to eliminate high-frequency components of the clamping pulses. To prevent the filter shunting the video-signal path (as would occur if C3 were returned to the negative side of the supply) C3 is connected to emitter-follower TR4 which applies to it the same signal as appears at the clamped point. Thus signal current does not flow in R15, but the low output impedance of TR4 effectively connects C3 to the negative side of the supply.

The clamped signal is applied via a complementary emitter-follower stage consisting of transistors TR7 and TR8 to a diode-bridge switching circuit comprising diodes D1 to D4. A positive-going, line-duration signal at one-fifth line frequency is applied to TR11. This signal is inverted and fed to the long-tailed pair comprising transistors TR9 and TR10; the resulting push-pull signals drive the bridge diodes into conduction and allow one line period of the red signal to pass through the bridge to a resistive mixing network, where it is combined with the outputs of the green, blue and luminance circuits. Other inputs to the mixing network are: a potential corresponding to blanking level and a mixed-sync signal, applied to the network via emitter-follower TR23. The mixed-sync feed is disconnected at R46 (see Fig. 4) if the unit is fed with composite video signals.

From the mixing network the signal is fed to the output of the unit via a feedback amplifier comprising transistors TR5 and TR6 (see Fig. 4). To facilitate multi-trace c.r.o. displays, using two or more UN9/544 units each with its own source of input signals, the standing potential with respect to earth on which the putput signal is superimposed can be selected as OV, −0·7V or −2·5V. This is done by means of an adjustable potential divider comprising TR7 and R17 (Fig. 4). The three potentials involved are derived from the potential divider D7, D8, R16, D9 and the required one is selected by means of relay contacts. The relays are energised by linking either pin 5 or pin 4 of the unit connector to pin 6. The possible conditions are shown in Table 1. Variable resistor R16 is a fine-adjustment control to compensate for tolerances in diode D9.

TABLE 1

Pins Linked	*Relays Operated*	*Base Potential Selected*	*d.c. Component of Output*
None	None	Positive side of R16	0V
4-6	RLA	Negative side of R15	−0·7V
5-6	RLA RLB	Positive side of R15	−2·5V

The clamp-pulse generator (see Fig. 4) comprises transistors TR13 to TR16; it is fed with mixed-syncs and generates negative-going pulses coincident with the trailing edges of the line-sync pulses. The pulse duration is 4 μs. In addition to driving the clamps, the clamp-pulse generator is used to trigger the timing circuits. Pulses from the collector of TR15 are fed via inverter stage TR8 to integrated circuit modules IC1 and IC5 to IC7.

Timing Circuits

Integrated circuits IC1 to IC3 function as monostable multivibrators. IC1 produces pulses with a duration of 10μs, IC2 is triggered from IC1 and produces pulses with a duration of 25 μs and IC3 accepts the outputs of IC1 and IC2. During normal picture lines the 10 μs and 25 μs pulses arrive successively at the inputs of IC3 and are of insufficient amplitude to trigger it. However, during the field-blanking period the twice-line-frequency equalising pulses cause IC1 to produce two outputs per line. Thus, for a period of about 3 μs, pulses from IC1 and IC2 are simultaneously present at the inputs to IC3 and the module is triggered into the unstable state. The pulse output from IC3 has a duration of about 550 μs (variable between 400 and 600 μs by means of R32) and this is applied as a reset pulse to the counter circuit

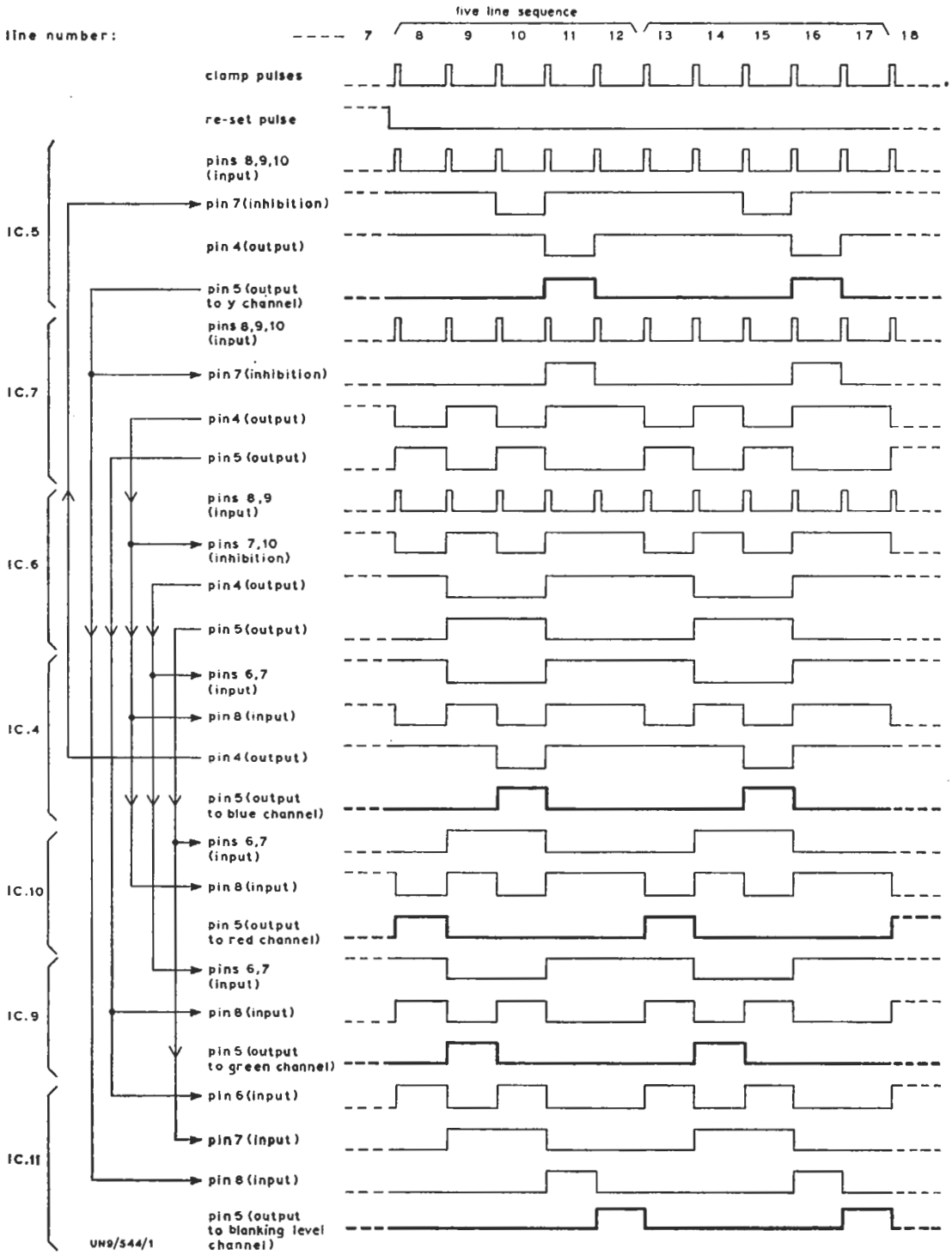


Fig. 5 Counter Waveforms in the RGBY Switch Unit UN9/544

(IC4 to IC7) which drives the diode bridges.

Integrated circuits IC4 to IC7 form a counter circuit and produce a sequence of output signals which are repeated at one fifth of line frequency. IC4 consists of *Or* and *Nor* gates, and modules IC5 to IC7 function as bistable multivibrators which can be inhibited by applying positive potentials to their tags 7 to 10. The counter is stopped at the end of each field by the reset pulse output of IC3 and starts operating again when the reset pulse ceases, at the commencement of the eighth line in each field.

Fig. 5 shows the waveforms at various points in the counter circuit and also the waveforms, derived from those in the counter circuit, which are produced by the *Nor* gates contained in integrated circuits IC9 to IC11. The signals which open the diode-bridge switches are shown in heavy lines; the sequence of component line periods in the composite output signal is: red (IC10), green (IC9), blue (IC4), luminance (IC5), blanking level (IC11). In addition to switching the blanking-level potential, the output from IC11 is fed, via the trigger-output amplifier comprising transistors TR38 to TR40, to pin 9 of the unit to provide the triggering facility mentioned under Introduction.

Power Supplies

A stabilised power supply at 12 volts is provided by a conventional stabiliser circuit (see Fig. 4) comprising transistors TR1 to TR3 and zener diode D5. Note that neither side of the supply is earthed.

The integrated circuits require a supply of power at 5·2 volts. This voltage is derived from the 12-volt supply via a series stabiliser comprising TR4 and D6. An additional power supply for the integrated circuits is derived from IC8 which provides an output of 1·15 volts.

Maintenance

Apparatus Required

Avometer Model 8
Cathode-ray oscilloscope with probe (sensitivity: 50 mV/cm)
625-line pulse-and-bar generator
Test circuit as shown in Fig. 6
Feed of mixed-syncs
R, G, B and Y video signals, all synchronous, with mixed-syncs

Test Procedure

1. Set all the variable resistors to mid-range and disconnect one end of R46 (Fig. 4).

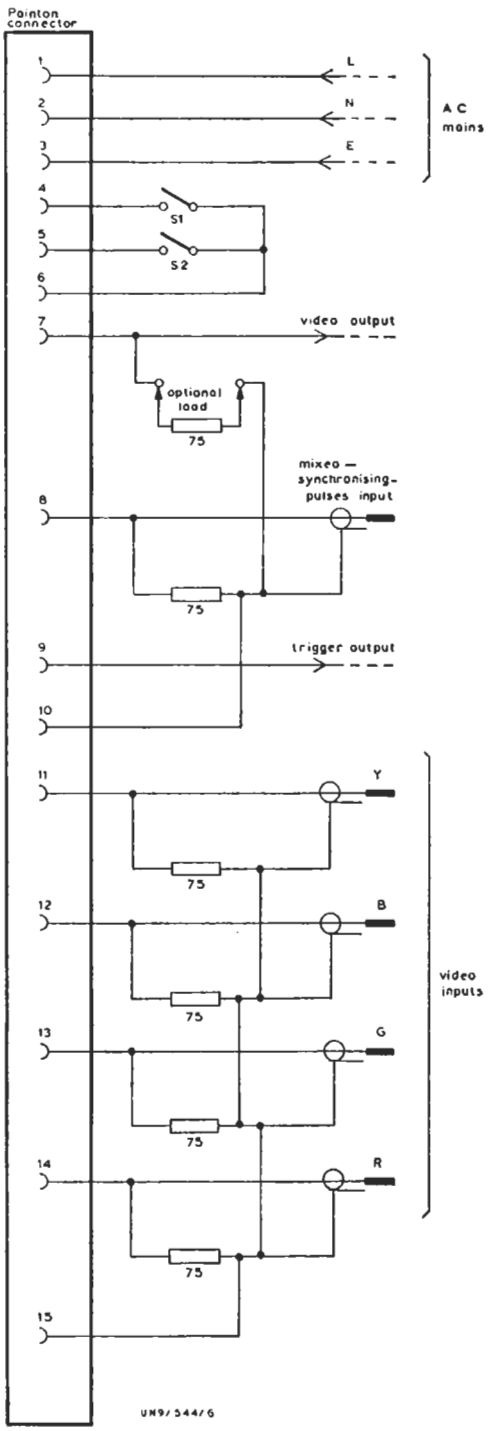


Fig. 6 Test Connector

2. Plug the unit into the test circuit and switch on.
3. Measure the d.c. potential across C4 (Fig. 4) and adjust R6 to make this 12V.
   Measure the d.c. potential between the negative end of C8 and chassis; it should be between 4·7 and 5·7 volts.
   Check that switches S1 and S2 in the test circuit are both open. Measure the potential between the negative end of C4 and chassis, and check that it can be varied between 5 and 7 volts by means of R16.
4. Apply mixed-syncs to the appropriate connector of the test circuit and examine the waveform at the collector of TR10 (Fig. 4). The sync pulse amplitude should be similar to that at the input.
5. Examine the waveform at pin 4 of IC3 and adjust R32 to obtain a pulse-duration of 550 μs.
6. Examine the waveforms at pin 5 on IC4, IC5, IC9, IC10 and IC11; each should consist of one-fifth-line-frequency pulses with an amplitude of 0·8V p-p and a duration of one line.
7. Examine the waveforms at the collectors of TR9, TR10, TR20, TR21, TR32, TR33, TR49 and TR50 (Fig. 3); each should consist of one-fifth-line-frequency pulse with a duration of one line and an amplitude of about 7V p-p.
8. Examine the *Trigger Output* pulses; they should have an amplitude of 4V p-p when the circuit is not loaded.
9. Apply R, G, B and Y video signals to the unit via the test circuit.
   Trigger the oscilloscope with the *Trigger Output* pulses.
   Examine the waveform of the video output signal with the 75-ohm load not connected. The component parts of the output signal should be displayed in the order R, G, B, Y, with one line of blanking level between sequences.
10. Measure the blanking-level potential of the output signal and adjust this potential to zero volts by means of R16 (Fig. 4).
11. Connect the 75 ohm load into the video-output wiring of the test circuit. Adjust the gains of the R, G, B and Y input amplifiers by means of R7, R42, R76 and R123 respectively (see Fig. 3) to obtain overall gains of 0 dB $\pm$0·1 dB.
12. Close S1 of the test circuit and check that the blanking-level of the video output signal is now about 0·7 V. Open S1.
13. Close S2 of the test circuit and check that the blanking-level of the video output signal is now about 2·5 V. Open S2.
14. Check that the hum and noise potentials during the active line periods are less than 10 mV p-p.
15. Re-connect the free end of R46 (Fig. 4).
16. Remove the four video inputs and check that the video output signal consists of mixed-sync pulses with an amplitude of 0·3V p-p $\pm$20%.
17. Apply to the Y-input of the test circuit a signal without field blanking; e.g. a line-synchronous pulse-and-bar test signal.
    Examine the output waveform, using an oscilloscope triggered at field rate, and adjust R32 (Fig. 4) to select the red input-signal during the eighth line-period of each field counting line periods from the leading edge of the first broad pulse.
18. Connect the output of the pulse-and-bar generator to each video-input of the test circuit in turn and confirm that the 2T pulse-to-bar ratio is better than 99%.
19. Apply the 50-cycle square-wave output of the pulse-and-bar generator to each test circuit input in turn. Check that the output-signal amplitude does not fall by more than 20 mV during one pulse of the waveform.

Reference

1. Designs Department Specification No. 8.248(67).

DEH/TES 9/69