SECTION 34

GATING UNIT UN9/534

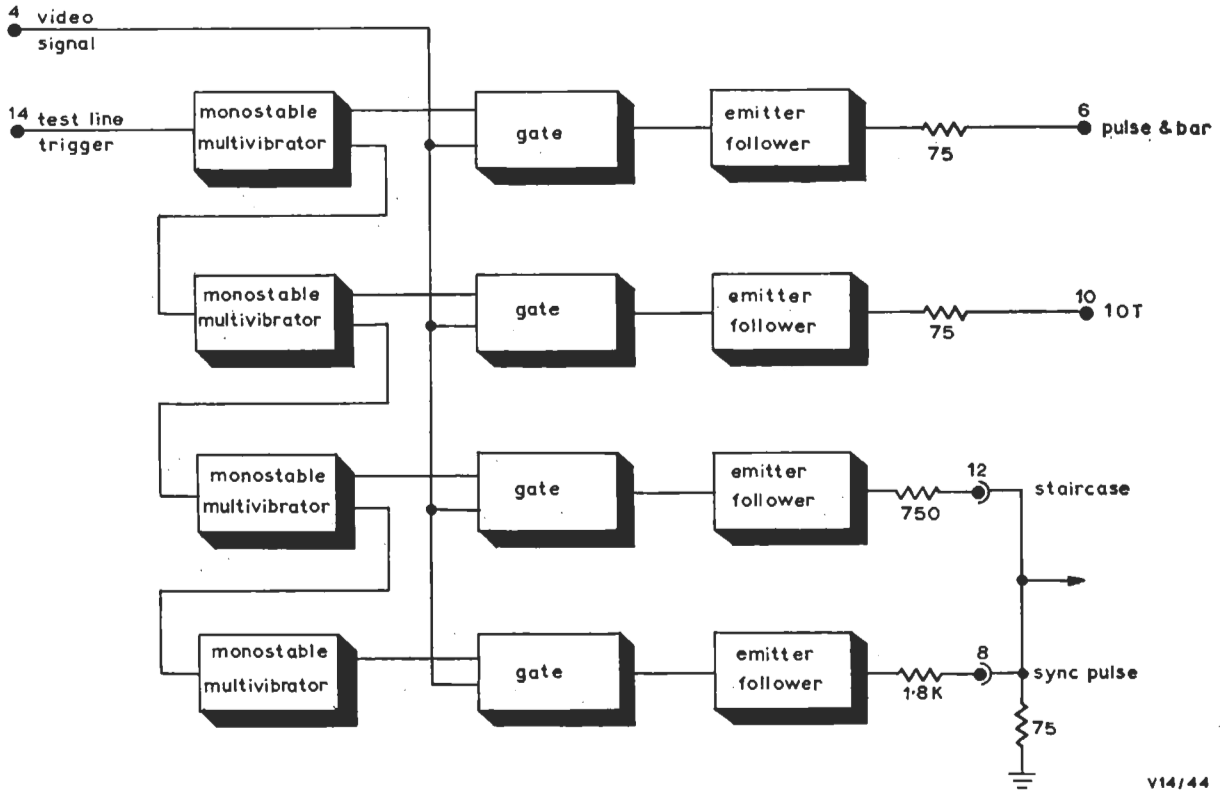

Fig. 34.1 Block Diagram of the UN9/534

Introduction

The UN9/534 accepts a clamped video signal and a test-line trigger pulse; its four outputs are selected portions of the test-line signal and the subsequent line sync pulse.

The UN9/534 is constructed on a CH1/12A chassis with index peg positions 19 and 24.

General Description

Fig. 34.1 shows a block diagram of the UN9/534. The test-line input pulse triggers four sequentially connected monostable multivibrators. The outputs of these multivibrators gate out various portions of the video input signal as shown in Fig. 34.2. The outputs of the staircase and sync-pulse gating circuits are mixed to give a waveform in which all the positive-going voltage transitions are equal under normal conditions. The 10T gating circuit is provided for a possible future 10T colour-test pulse.

Circuit Description

The circuit of the UN9/534 is given on page 34.3. The monostable multivibrators are shunted by 100 pF capacitors, slowing down the edges of the pulses to prevent switching transients appearing on the sampled waveforms. The emitters of the sampling transistors are fed with the video signal via emitter followers. The d.c. potentials at the collectors of the sampling transistors are set at the clamped

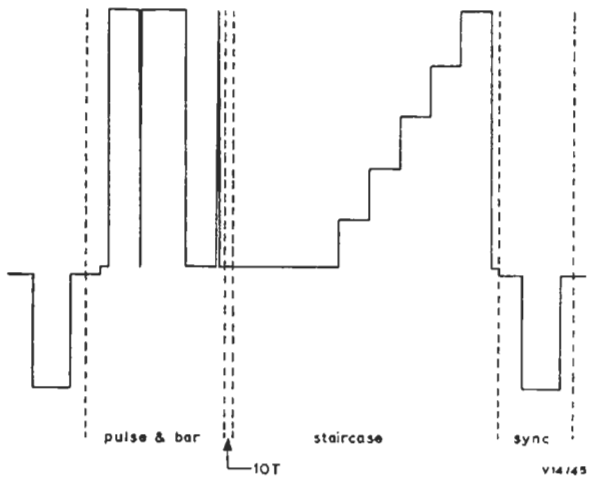

Fig. 34.2 Showing how the Test Line is Divided Up by Gating

black level of the video signal (about + 17·5 volts). Their bases are returned to a more negative potential to ensure that the sampling transistors remain cut off except during the sampling pulses. The outputs of the UN9/534 are fed via emitter followers.

Test Procedure

The UN9/534 is tested as part of an Automatic Monitor Major.

Bibliography

1. *Emitter-timed Monostable Circuits:* Mullard Technical Communications, Vol. 5, No. 49, July 1961.

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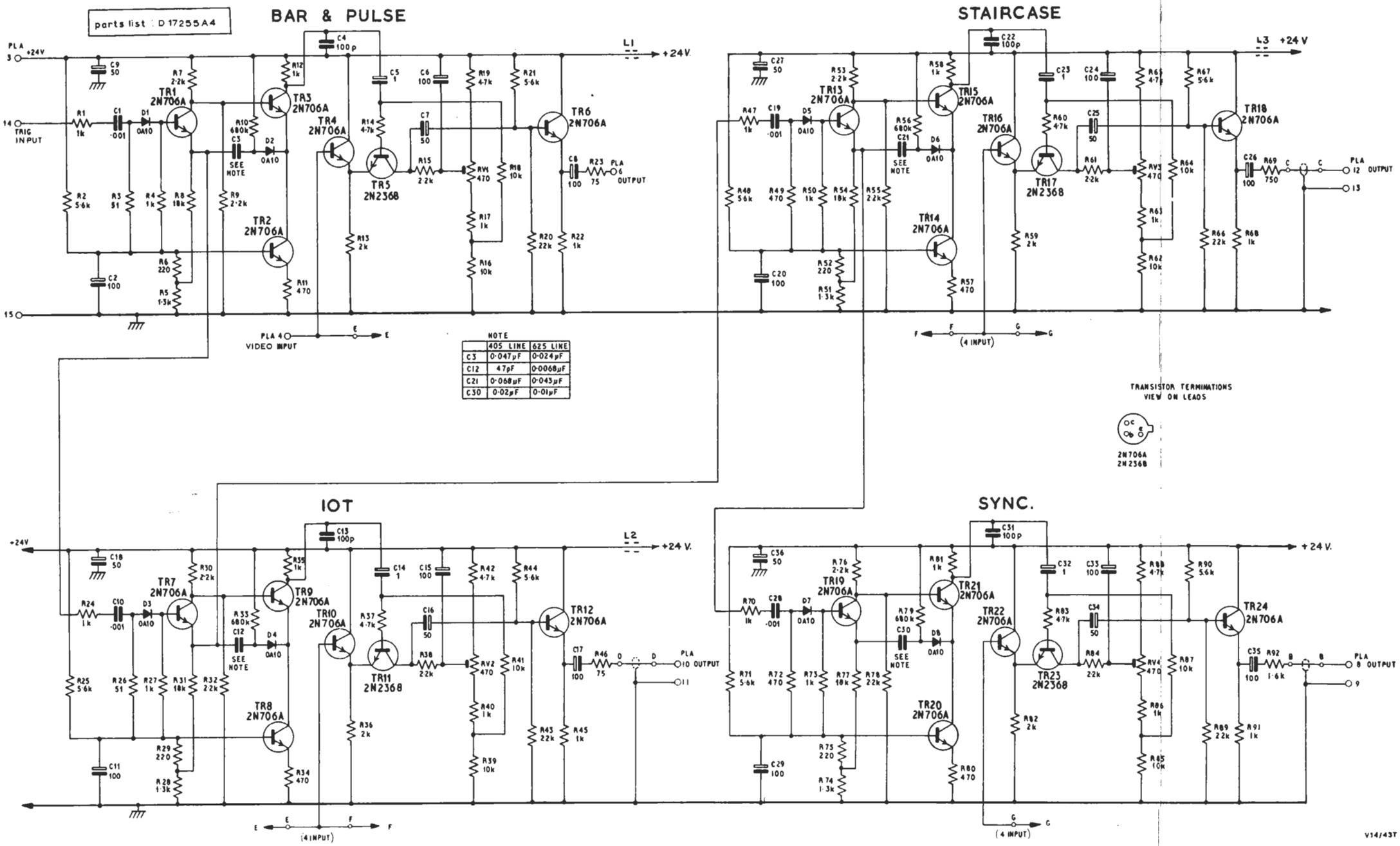

34.3

Fig. 34.3 Circuit of the UN9/534