VIDEO SWITCH UNIT UN9/521 SERIES

Introduction

The UN9/521 accepts two video inputs, two pairs of clamp pulse inputs and a pair of switch pulse inputs: its output is switched between the two video inputs according to the instantaneous values of the switch pulse inputs.

The UN9/521 is constructed on a CH1/12A chassis with index peg positions 7 and 15.

Circuit Description

The circuit of the UN9/521, given in Fig. 1, consists of two identical clamped input amplifiers followed by a video switch and an output amplifier.

Transistors TR1 and TR2 form part of a complementary direct-coupled negative-feedback amplifier whose output is fed to two emitter followers TR3 and TR4. The clamp pulses are fed to the output of transistor TR4 via a subcarrier-frequency rejection circuit and diodes D1 and D2. The outputs of transistors TR3 and TR4 are coupled via resistor R14. This resistor and capacitors C5 and C6 form a low-pass filter which prevents the high-frequency out-of-balance components of the clamp pulses from reaching the base of transistor TR5. The low-frequency components of the clamp pulses are balanced in the clamp pulse generator. Thus there are no clamp-pulse transients in the output of the unit. Transistors TR5 and TR6 form a compound emitter follower feeding the video switch circuit. The negative-going excursion of the switch pulse input on pin 12 causes diode D3 to conduct. This produces a voltage drop across resistor R21 which reverse biases diode D4 thereby switching off video input A. The positive-going excursion of the switch pulse reverse biases diode D3 causing diode D4 to conduct and switching on video input A. The crosstalk via the capacitance of diode D4 when it is reverse-biased is balanced out by the capacitor C19 feeding the base of transistor TR7.

The shunt inductor L4 in the collector load of transistor TR7 provides high-frequency correction to the switched video signal. Transistors TR8 to TR10 in the output amplifier are connected as emitter followers. Resistor R31 is a gain control and resistor R34 sets the d.c. level of the output signal.

Test Procedure

Routine maintenance is not required. It is convenient to check the unit when it is plugged into the parent unit, e.g. PA18/518 or PA18/522; the waveforms as indicated in Fig. 1 should be obtained.

Reference

1. Designs Department Specification No. 8.167(64).

MJR 2/67
AIB 8/70

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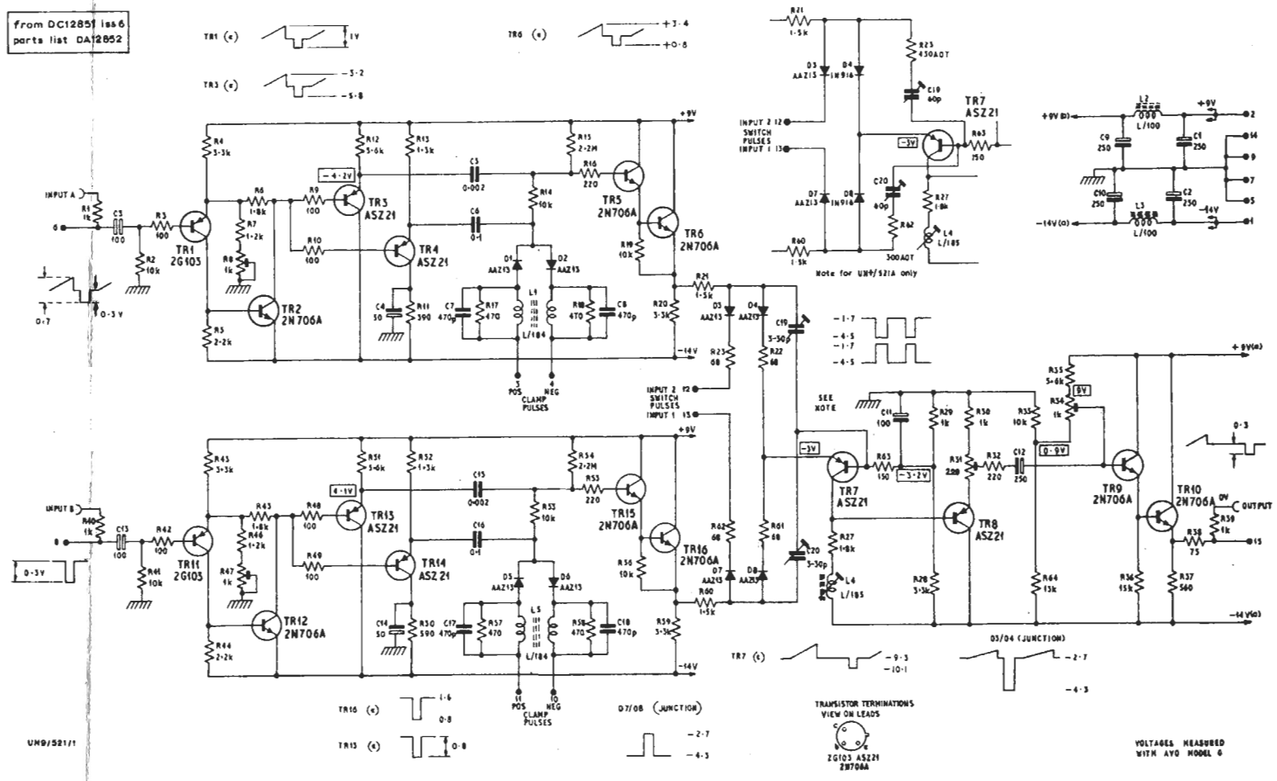

Fig. 1 Circuit of the Video Switch Unit UN9/521 and UN9/521A