CLOCK AND STORE LOGIC UNIT UN23/535

Introduction

The UN23/535 accepts a number of d.c. inputs which are used to perform particular switching functions or to provide particular d.c. output signals in accordance with decoding circuits in the unit. In addition the unit contains a clock-pulse generator which provides an output of 5-volt pulses at a repitition rate of 2 p.p.s. Another clock-pulse output is obtained via a gate which is controlled by certain of the input signals.

The unit is designed for use with a Television Automatic Monitor MN2M/518. It is built on a printed wiring board and mounted in an ISEP chassis assembly with standard index pegs in positions 5, 7 and 21.

General Specification

Direct clock-pulse output	5-volt positive-going pulses at a rate of 2 p.p.s.
Gated clock-pulse	One clock-pulse every 4 seconds when enabled by appropriate input signals
Power requirements	+12 volts +5 volts
Pin connections	33-way ISEP plug

Circuit Description (Fig. 1)

The unit can be considered as a number of separate sections.

(a) Clock-pulse Generator and Gating Circuits

Unijunction transistor TR1 and its associated components form a simple pulse generator. R1 and C5 control the pulse repetition frequency which is set at 4 p.p.s. by selecting R5. The output pulses, which are positive-going and limited in amplitude to 5 volts, are fed to a JK-bistable circuit, IC6a. The output of the bistable, at pin PLA10, is 5-volt positive-going pulses at a rate of 2 p.p.s.

The output from the bistable IC6a is also taken to one input of a two-input NAND gate IC5d. When the other input receives a logic 1 signal an output is produced and passed to a three-stage divide-by-eight circuit comprising JK-bistable elements IC6b and IC7. The gated output, at PLA2, is a train of positive-going pulses at a rate of one pulse every four seconds.

Transistor TR6 is driven from the output of gate IC5d. The collector is taken to pin PLA4 for use in driving an external signal lamp.

(b) Start-up and End of Cycle Reset Circuits

When power is initially switched on a ramp waveform is developed by a Miller-integrator circuit comprising TR4, TR5 and associated components. The waveform is inverted in gate IC9b to produce a negative-going pulse at PLA28 between 3 and 6 seconds long.

Logic 1 signals applied to gate IC4c trigger a monostable multivibrator IC8 to produce a positive-going 1-ms pulse which is inverted in gate IC9a. The output of the gate is connected to PLA28.

(c) Main and Reserve Feed Logic Stores

Gates IC2a, b and c form the main feed logic store and gates IC1a, b and c the reserve feed logic store. The action of each circuit is identical.

Consider the main feed logic store. The input, on pin 13 of gate IC2a, is stored when logic 1 signals are applied to pins 1 and 2. The output of the gate is connected to PLA31. The store is cleared by the application of a logic 1 signal to pin 11 of gate IC2c.

(d) Executive Action Circuit

The signal on PLA20 is transferred to PLA32, without storage, when logic 1 signals are applied to PLA14 and PLA15. The same signal is also stored, by gates IC4a and b, and applied to the base of TR2. The store is cleared by applying a logic 0 signal to PLA29.

(e) Gated Alarm and System Normal Circuits

A logic 1 signal applied to the base of TR2 energises relay RLA, the contacts of which are connected to PLA6, PLA8 and PLA9.

Relay RLB is connected so that a failure of either the +12 or +5 volt supply causes the relay to be de-energised. The relay make contacts are connected to PLA22 and PLA24.

Test Schedule

Apparatus Required

Oscilloscope
Frequency Counter
+12 volt Stabilised Power Supplier
+5 volt Stabilised Power Supplier
Avometer Model 8

Test Procedure

1. Switch on the 5-volt supply and check that a negative-going pulse, with a duration of between 3 and 6 seconds, is present at PLA28. The pulse should be at least 3 volts in amplitude and have a minimum level within 450 mV of chassis potential.
2. Check that RLB is energised.
3. Connect PLA15, PLA17, PLA19, PLA20 and PLA29 to chassis.
4. Check that a logic 0 signal, zero volts, exists at PLA30, PLA31 and PLA32.
5. Connect PLA11 to chassis.
6. Disconnect PLA20 from chassis.
7. Momentarily disconnect PLA19 from chassis.
8. Check that a logic 1 signal, at least 3·5 volts, exists at pin PLA30.
9. Momentarily disconnect PLA11 from chassis.
10. Check that logic 0 signals exist at PLA30 and PLA31.
11. Disconnect PLA15 from chassis.
12. Check that a logic 1 signal exists at PLA32 until PLA15 is reconnected to chassis.

13. Disconnect PLA15 from chassis.
14. Check that RLA is energised.
15. Connect PLA15 and PLA20 to chassis.
16. Momentarily connect PLA13 to chassis.
17. Check that RLA is de-energised.
18. Check the waveform of the pulses at PLA10. The amplitude should be at least 3 volts and the repitition rate 2 p.p.s. ±10 per cent. R1 is selected to obtain the required repitition rate.
19. Connect PLA20 and PLA29 to chassis.
20. Check that PLA2 is at logic 1.
21. Disconnect PLA20 from chassis.
22. Check the waveform at PLA2 comprises logic 1 pulses at a repetition rate of about four seconds.
23. Disconnect PLA20 from chassis and connect PLA29 to chassis.
24. Check that pulses are still present at PLA2.

Reference

Designs Department Specification 11.104(70).

Reference to Typical Associated Equipment

Television Automatic Monitor MN2M/518.

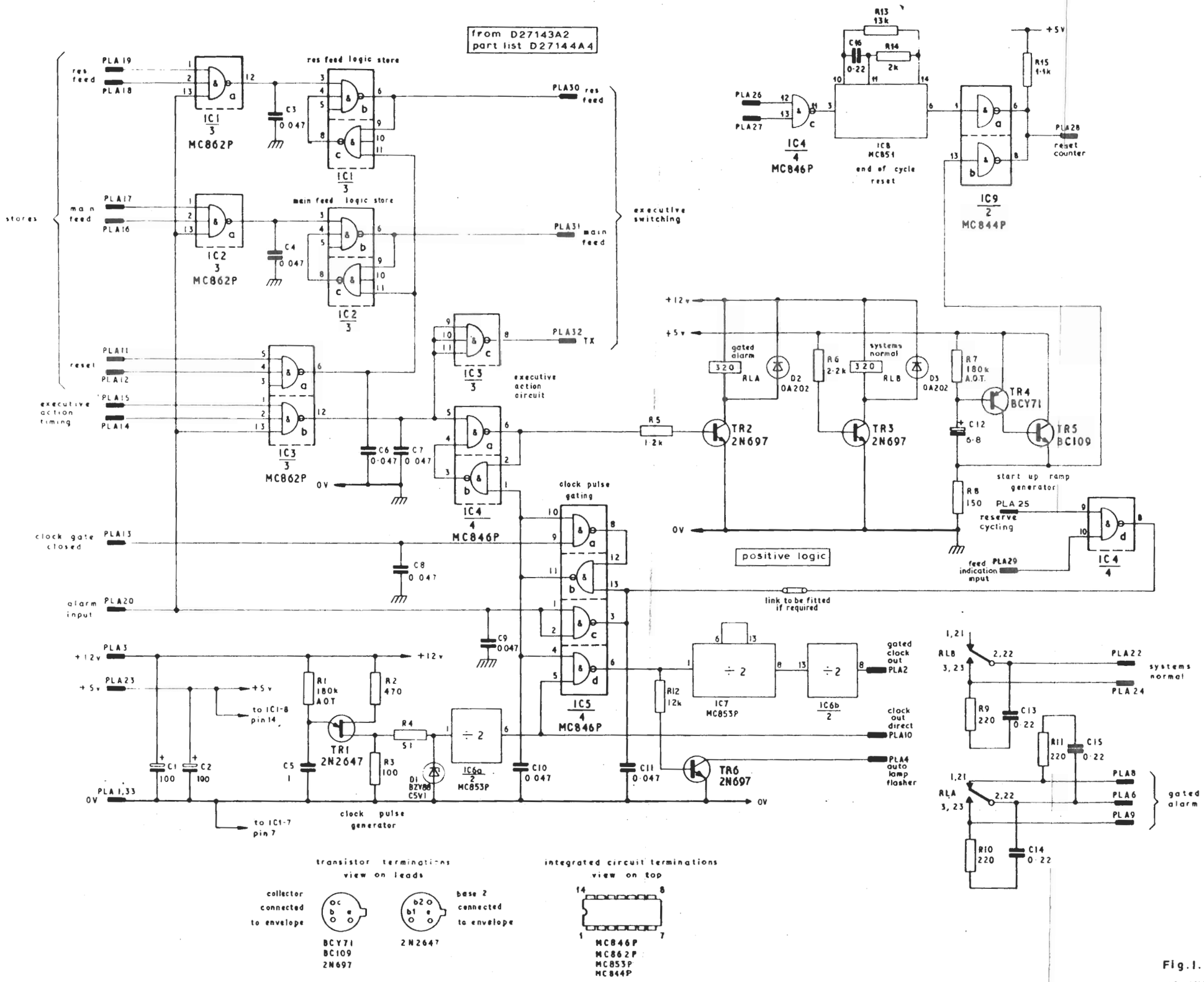

Fig.1. Circuit of UN23/535