SOUND IN SYNCS COUNTER AND CLOCK UNIT UN23/528

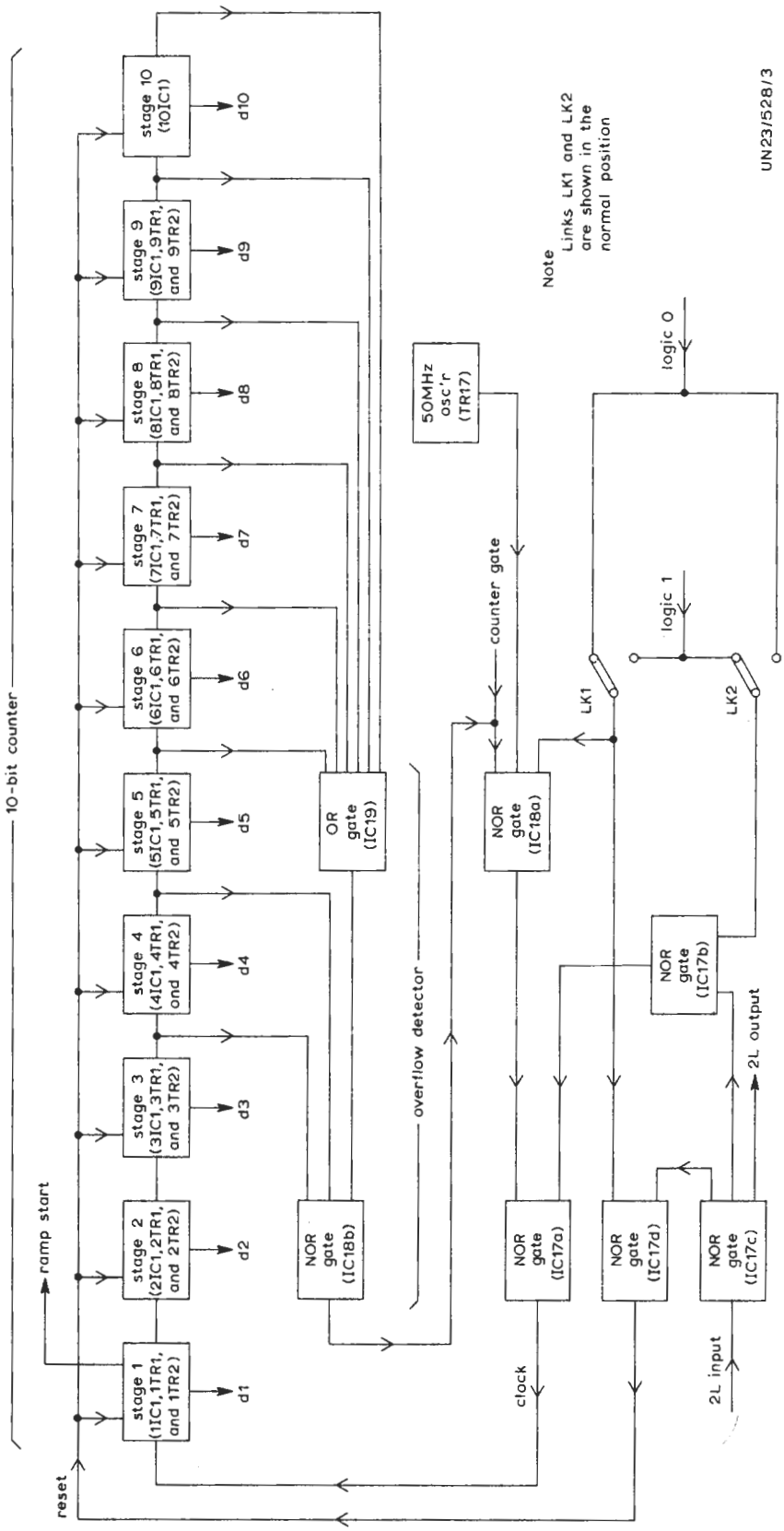

Fig.1. Block Diagram of the Counter & Clock Unit UN23/528

Introduction

The UN23/528 is a ten-stage ripple-through binary up-counter which operates at a clock frequency of 50 MHz and forms part of a sound-in-syncs coder[1].

The counting cycle is repeated at twice line rate, from zero up to a maximum possible count of 2^{10}; circuits are provided to ensure that the counter cannot overflow and repeat a counting cycle. The counter outputs feed a shift register[2] and, at the start of each count, a *Ramp Start* output is provided and fed to a ramp generator in an associated sample-and-hold unit[3].

By means of internal links, a check-counter facility can be provided whereby the counter is clocked by twice line frequency pulses to give a succession of 10-bit words which increase in value by one bit per word. The coded output thus produced represents an audio staircase waveform in which each step is equal to one quantising level.

In conjunction with the associated sample-and-hold and shift-register units, the UN23/528 converts analogue information to digital form.

The UN23/528 is constructed on a printed-wiring card fitted with a 33-way ISEP connector. Index pin positions are 3, 7 and 17. Power supplies at +5 volts, −5 volts and −12 volts are required.

General Specification

Inputs

Counter Gate	twice line frequency pulse, MECL logic, inhibits counter clocking when at logic 1 (obtained from UN23/530)
2L Input	twice-line frequency positive-going pulses, duration 2·35 μs, TTL logic (obtained from UN23/522)

Outputs

Digit Outputs	ten separate outputs, one for each bit of the coded word, labelled *d1* to *d10*, TTL logic
Ramp Start	Twice-line repetitive pulses, MECL logic
2L Output	twice line frequency negative-going pulses, duration 2·35 μs, MECL logic

Power Requirements	20 mA at +5V, 310 mA at −5V, 10 mA at −12V

Logic Levels

TTL Levels	logic level 1, about +3·5V (+5V max.) logic level 0, about 0V (+0·4V max.)
MECL Levels	logic level 1, about −0·75V (−0·7V max.) logic level 0, about −1·75V (−1·7V max.)

Circuit Description

A simplified block diagram of the UN23/528 is shown in Fig.1 and a detailed circuit diagram in Fig.2, on page 5.

The counter consists of ten JK bistable stages (1IC1 to 10IC1) which are connected as a ripple-through up-counter; i.e. a counter which counts upwards and in which each stage is clocked by the preceding stage. The count cycle starts 4·8 μs after the leading edge of syncs and is repeated at twice line rate; this waveform is known as 2L+ 4·8 μs. At the end of each count sequence, the counter outputs are transferred to an associated shift register. The long-tailed pairs in each counter stage (e.g. 1TR1 and 1TR2 in stage 1) act as interface circuits and change the MECL outputs of the bistable elements to TTL logic levels.

Normal Operation

For normal operation the counter is clocked by the output of a 50-MHz crystal oscillator (TR17). Link LK1 is set to apply a logic 0 to an input of gates IC17d and IC18a, link LK2 is set to apply a logic 1 to an input of gate IC17b. A 2L positive-going signal at TTL levels is applied to PLA13 at which point it is translated to MECL levels by a resistor network, which functions as an interface circuit; it is then inverted by gate IC17c. The resulting negative-going pulse is gated together with a logic 0 from LK1 in NOR gate IC17d to provide a positive-going counter-reset pulse which ensures that each stage of the counter is in the Q = 0 condition before the start of a counting sequence.

The output of the 50-MHz oscillator is set to MECL levels by a potential divider consisting of resistors R24 and R25 and is then applied to NOR gate IC18a, together with a *Counter Gate* input and a logic 0 from link LK1. The output from IC18a is inverted by IC17a and fed as clock pulse information to the counter. When the *Counter Gate* input to IC18a is at logic 1 the clock input to the counter is at logic 1 also and the operation of the counter is inhibited, but when the *Counter Gate* input is at logic 0 the 50-MHz clock pulses are fed to the counter. Counting starts when the first positive-going edge of the 50 MHz waveform is applied to 1IC1 and continues (provided that the *Counter Gate* input remains at logic 0) up to a maximum count which is determined by the counter-overflow gates IC18b and IC19. These gates determine when the eight most significant digits are at logic 1; i.e. when the $\overline{Q}$ outputs are at logic 0. When this condition is reached the output of IC18b changes to logic level 1; this change is applied to the *Counter Gate* input of IC18a and thus prevents further counting.

The Q output of the first counter stage is used to start a ramp generator in the associated sample-and-hold unit. Thus the start of counting is synchronised with the start of the ramp.

Check Counter Operation

For this mode of working the counter is clocked by a twice-line-frequency pulse. Link LK1 is set to apply a logic 1 to gates IC18a and IC17d, and link LK2 is set to apply a logic 0 to gate IC17b. The logic 1 applied to IC17d holds the counter-reset line at logic 0 and so prevents reset pulses reaching the counter. The logic 1 applied to IC18a ensures that the output of IC18a is held at logic 0 to inhibit the passage of 50-MHz clock information. The logic 0 applied to IC17b holds this gate in the open condition and permits the passage of twice-line-frequency pulses; these are subsequently inverted by IC17a and are applied to the clock input of the counter as negative-going pulses with the result that the counter is continuously clocked at twice line rate by the positive-going edges of the applied pulses.

Maintenance

The only adjustable component in the UN23/528 is the inductor in the crystal oscillator circuit; this may require adjustment if components associated with the oscillator circuit are changed. To adjust proceed as follows:

1. Monitor the 50-MHz signal at the junction of R24 and R25 with an oscilloscope probe.
2. Adjust the core of the inductor for maximum signal amplitude and check that the waveform obtained conforms to MECL logic levels (see Specification).

To check the performance of the unit:

1. Put links LK1 and LK2 to the *Check* position .
2. Confirm that negative-going twice-line-frequency pulses are present at the clock input (pins 6 and 8) of 1IC1.
3. Check that each stage of the counter is dividing by two and that output transitions occur on positive-going transitions at the input.

References

1. Sound-in-syncs Coder CD2M/505
2. Sound-in-syncs Shift Register UN23/527
3. Sound-in-syncs Sample and Hold Unit UN23/530

TES 4/71

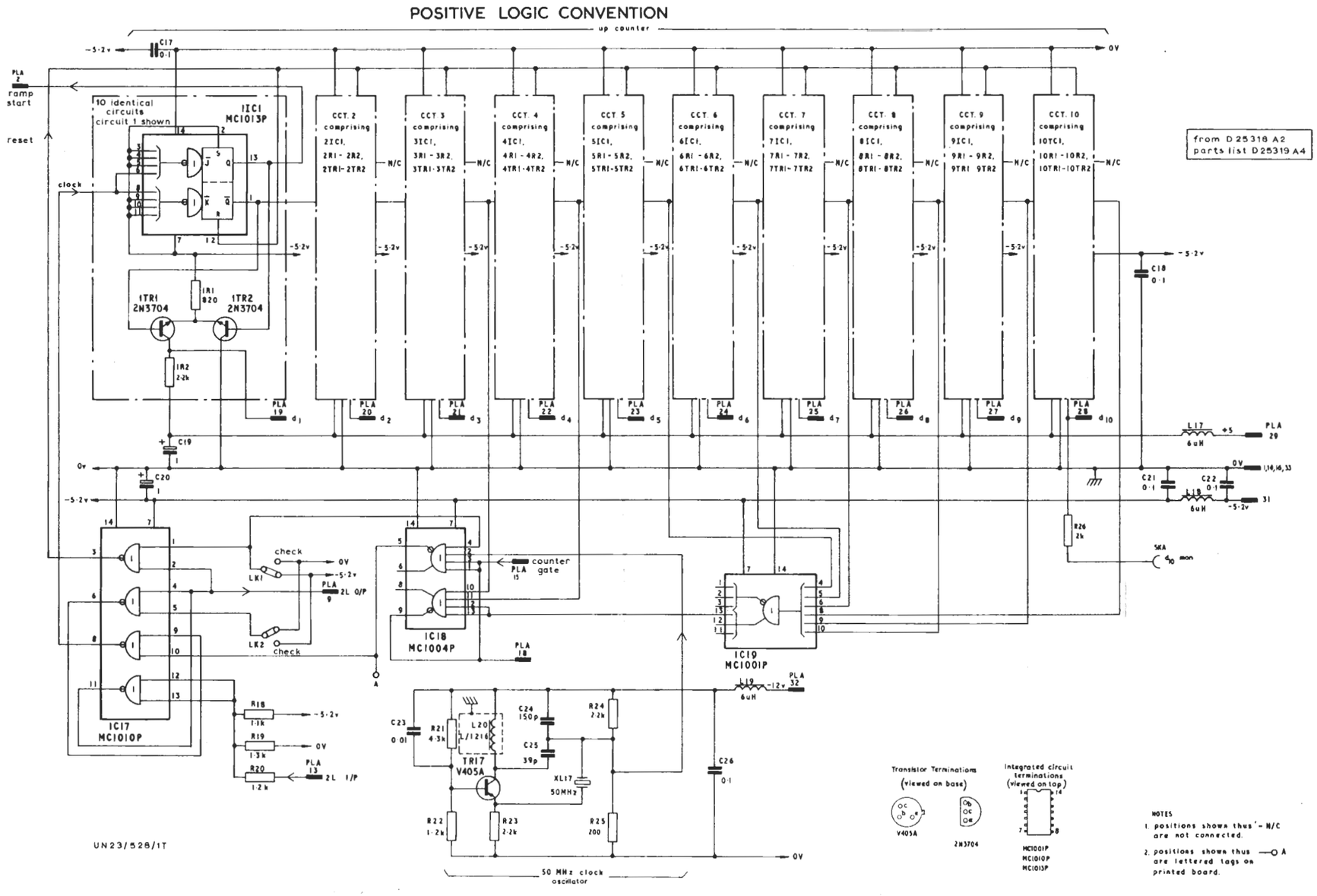

Fig.2 Circuit of the Counter and Clock Unit UN23/528