SOUND IN SYNCS GATED STATICISER UNIT UN23/525

Introduction

The UN23/525 forms part of a sound-in-syncs decoder[1]. It consists, basically, of 10 bistable stages and is used as a temporary store for ten-bit words which are being transferred in parallel form from a shift register[2] to a counter-and-clock unit[3].

Normally words are read into the UN23/525 at twice-line rate. However, before the reading-in takes place each word as inspected in the preceding shift register for faults and, if a fault is detected, an inhibit signal is fed to the UN23/525 to prevent the staticiser being reset and the faulty word read in. Under these conditions the ten-bit word that is currently stored is repeatedly fed to the following counter-and-clock unit.

The UN23/525 is constructed on a printed-wiring board which is fitted with a 33-way ISEP connector. Index-pin positions are 3, 7 and 17. Power supplies at +5V are required.

General Specification

Input Signals

Digit Inputs	ten separate inputs, one for each bit of the ten-bit coded word, labelled *d1 in* to *d10 in* (obtained from UN23/524)
Reset Input	a twice-line rate positive-going pulse delayed by 4·8µs w.r.t. leading edge of syncs (2L +4·8); obtained from UN23/522.
Word Valid Input	a line-repetitive pulse, normally at TTL logic 1 but changing to logic 0 when inhibition required (obtained from UN23/524)
Shift Pulse Input	a twice-line rate positive-going pulse delayed by 5·6µs w.r.t. leading edge of syncs (2L +5·6); obtained from UN23/523
$\overline{LSW}$ Input	a line-frequency square wave (obtained from UN23/522)

Output Signals

Digit Outputs	ten separate outputs, one for each bit of the ten-bit coded word, labelled *d1* to *d10*.
Transfer Odd Output	line-repetitive positive-going pulse, starting 37·6µs after the leading edge of syncs
Transfer Even Output	line-repetitive positive-going pulse, starting 5·6µs after the leading edge of syncs

Power Requirements 140 mA at 5·2V.

Note: All inputs and outputs are TTL logic signals. TTL logic levels are:

logic level 1, about +3·5V (+5V max)
logic level 0, about 0V (+0·4V max)

Circuit Description

A simplified logic diagram of a UN23/525 is shown in Fig.1 and a circuit diagram in Fig.2.

The heart of the unit consists of ten RS bistable stages (see Instruction GP.1) which are formed from cross-coupled NAND gates and contained in integrated circuits IC2, IC3, IC4, IC6 and IC7. As all the bistable stages are similar, only one is described below.
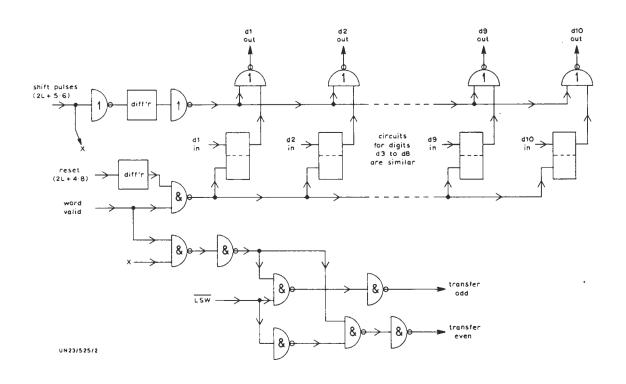

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Fig.1 Simplified Logic Diagram of the UN23/525

The NAND gates connected to pins 1 to 6 of IC2 form the bistable stage which handles digit 1 of the coded word. Normally input-pins 1 and 5 are held at logic 1 and so the output on pin 6 is also at logic 1. A negative-going input signal applied to pin 1 drives it momentarily to logic 0 while pin 5 remains at logic 1; therefore the output changes to logic 0. On the receipt of a reset pulse, the potential on pin 5 changes momentarily to logic 0 while pin 1 remains at logic 1; as a result the device is reset so that the output returns to the logic 1 condition. The reset pulse is derived by gating the differentiated *Reset* input with the *Word Valid* input. The reset pins of all the bistable stages are commoned, and so all bistables are reset simultaneously.

Transfer Odd and *Transfer Even* pulses are developed in the unit for use in the associated shift register. The transfer pulses are derived by first gating the *Word Valid* and *Shift Pulse* inputs, and then gating the resultant pulse with either $\overline{LSW}$ (to produce *Transfer Odd* pulses) or with inverted $\overline{LSW}$ (to produce *Transfer Even* pulses). The transfer-pulse duration is $0.8\,\mu s$.

When a transfer pulse is fed to the associated shift register, the selected 10-bit word is read into the 10 bistable stages contained in the staticiser. The bistable outputs are connected to NOR gates contained in integrated circuits IC8, IC9 and IC10. These gates are opened by negative-going pulses which are derived from the differentiated trailing edges of inverted shift pulses and the information stored in the staticiser is then read out and fed to the associated counter-and-hold unit for subsequent decoding.

Note that the digit information incoming to the staticiser from the shift register is inverted. The output gates of the staticiser provide a further inversion and thus restore the information to the polarity required for the decoding process.

Maintenance

Waveforms at various points in the UN23/525 are given in Fig. 3. To check the performance of the unit:

1. Apply a full-count sound-in-syncs signal to the input of the parent decoder. (This signal can be produced by removing the UN23/528 unit from the associated coder[4]).

2. Check digit inputs *d1* to *d10* in turn. Negative-going pulses at twice-line rate should be present. Check that the pulse timings with respect to the leading edge of syncs are $+5.6\,\mu s$ and $+37.6\,\mu s$. If either the odd or even sets of digit inputs are missing, check the transfer pulse outputs on PLA 17 and PLA 18.

3. Check outputs *d1* to *d10* in turn. These should be twice-line rate positive-going pulses timed at $+6.4\,\mu s$ and $+38.4\,\mu s$ with respect to the leading edge of syncs and with a duration of 150 ns. If these pulses are absent, check that negative-going shift pulses with the same timings are present at pin 1 of IC8.

4. Check that the bistable stages are reset to the pin 6 (or pin 8) = 0 condition at twice-line rate. The reset pulses developed at pin 3 of IC1 should be negative-going with a duration of about 200 ns and timed at $4.8\,\mu s$ and $36.8\,\mu s$ with respect to the leading edge of syncs.

References to Typical Associated Equipment

1. Sound-in-syncs Decoder CD3M/504
2. Sound-in-syncs Shift Register UN23/524
3. Counter and Clock Unit UN23/526
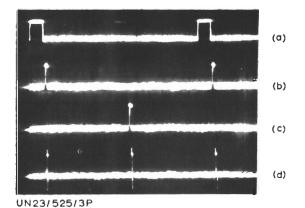4. Sound-in-syncs Coder CD2M/505

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Fig. 3 Waveforms in the UN23/525
(a) sep. syncs from UN16/515 (given as timing reference)
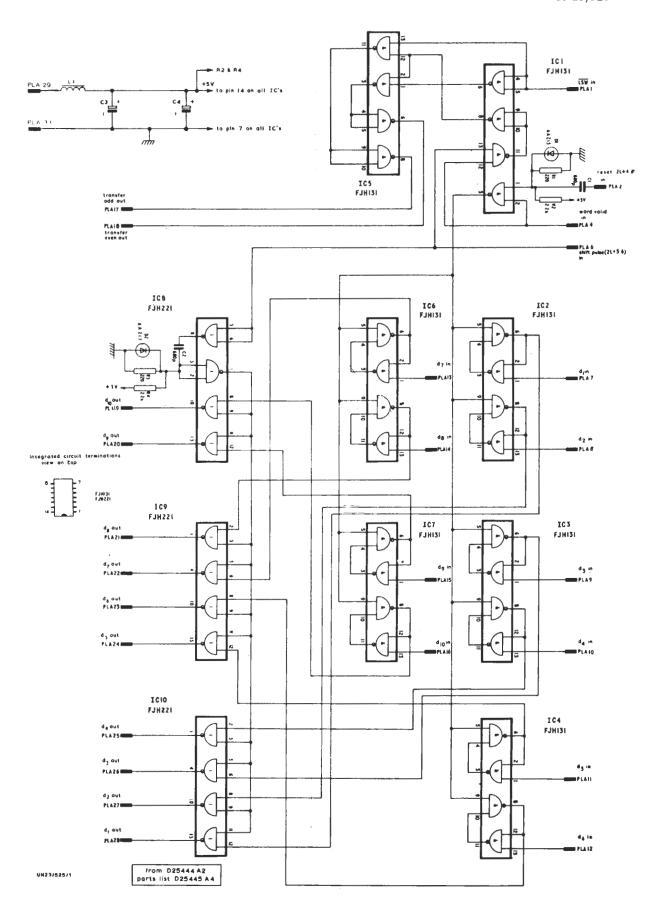(b) transfer even
(c) transfer odd   } 4 V p-p
(d) d1 output; d2 to d10   } 10 µs/div
     are similar

Fig.2 Circuit of the UN23/525