GATING UNIT UN23/510

Introduction

The UN23/510 accepts clock-pulse and other d.c. inputs and provides 16 outputs derived from the clock-pulse input.

The unit is built on an ISEP card with standard index pegs in positions 27, 29 and 31.

General Specification

Clock pulse input level	positive going, maximum value between 2·4 and 5·25 volts
Clock pulse input frequency	d.c. to 5 MHz.
Clock pulse input loading	two logic loads, 6·4 mA max.
Other inputs loading	one logic load, 3·2 mA max.
Fan-out from each output terminal	10 logic loads each of 1·6 mA.
Logic levels	
Logic 1	2·6 volts minimum
Logic 0	0·4 volt maximum
Power requirement	+6 volts at 170 mA.
Pin connections	33-way ISEP plugs.

Circuit Description (Figs. 1 to 3)

Fig. 1 is a circuit diagram of the UN23/510.

The main part of the gating unit is a six-stage divide-by-64 ripple-through counter. Each stage, circuits IC1 to IC6, comprises a master-slave JK-bistable. Outputs from the various stages of the divider chain are taken to 16 gates and 16 inverting gates which feed the 16 output points. The outputs are divided into two groups of eight. One group produces pulses known as Bits and the other group pulses eight times as long known as Channels. The Bit and Channel waveforms, and their component waveforms, are shown in Fig. 2.

Each stage of the divider chain can be cleared simultaneously by applying a negative-going pulse to pin PLA12. An indirect method of clearing the divider chain is to apply logic 1 signals to both pins PLA10 and PLA11. A logic 0 signal from circuit IC19a is inverted in gate IC9b and used to trigger a one-shot monostable circuit IC18. A positive pulse from the monostable is inverted in gate IC9c and applied to the clear inputs of the bistable circuits. This action can be inhibited by applying a logic 0 signal to pin PLA26.

Gates IC19b and IC19c form a bistable latch circuit. When clock pulses are applied to IC19b a logic 1 signal is developed at the output of the latch, IC19b pin 8, until the circuit is cleared by applying a logic 0 signal to gate IC19c.

The six-volt power supply is connected by a silicon diode which reduces the working voltage to about 5·2 volts. To prevent the maximum rating of the integrated circuits from being exceeded the power supplier used should incorporate over-voltage protection operating at about 7·5 volts.

Fig. 3 shows the relationship of Bit and Channel information. By using a two-input gate any one Bit of the 64 Bits available can be selected. Each Bit has the width of a single clock pulse.

Test Schedule

Apparatus Required

Source of clock pulses
Oscilloscope
6-volt power supplier
Avometer Model 8

Test Procedure

1. Check that the current consumption of the unit is 170 ±30 mA.
2. Check that the voltage across capacitors C2 and C3 is 5·2 ±0·2 volts.
3. Connect pins PLA10 and PLA11 to chassis.
4. Apply clock pulses to pins PLA14 and PLA15.
5. Check, by reference to Figs. 2 and 3, that the correct outputs are produced.
6. Connect pin PLA12 to chassis and check that the output is cleared.
7. Connect pin PLA26 to chassis and check that the outputs return.
8. Disconnect pins PLA12 and 26 from chassis.
9. Disconnect pins PLA10 and PLA11 from chassis and check that the outputs are cleared.

Reference

Designs Department Specification 5.156(69).

References to Typical Associated Equipment

Insertion Communication Equipment (Sending) EP1M/514.

Insertion Communication Equipment (Receiving) EP1M/515.

Television Automatic Monitor MN2M/518.

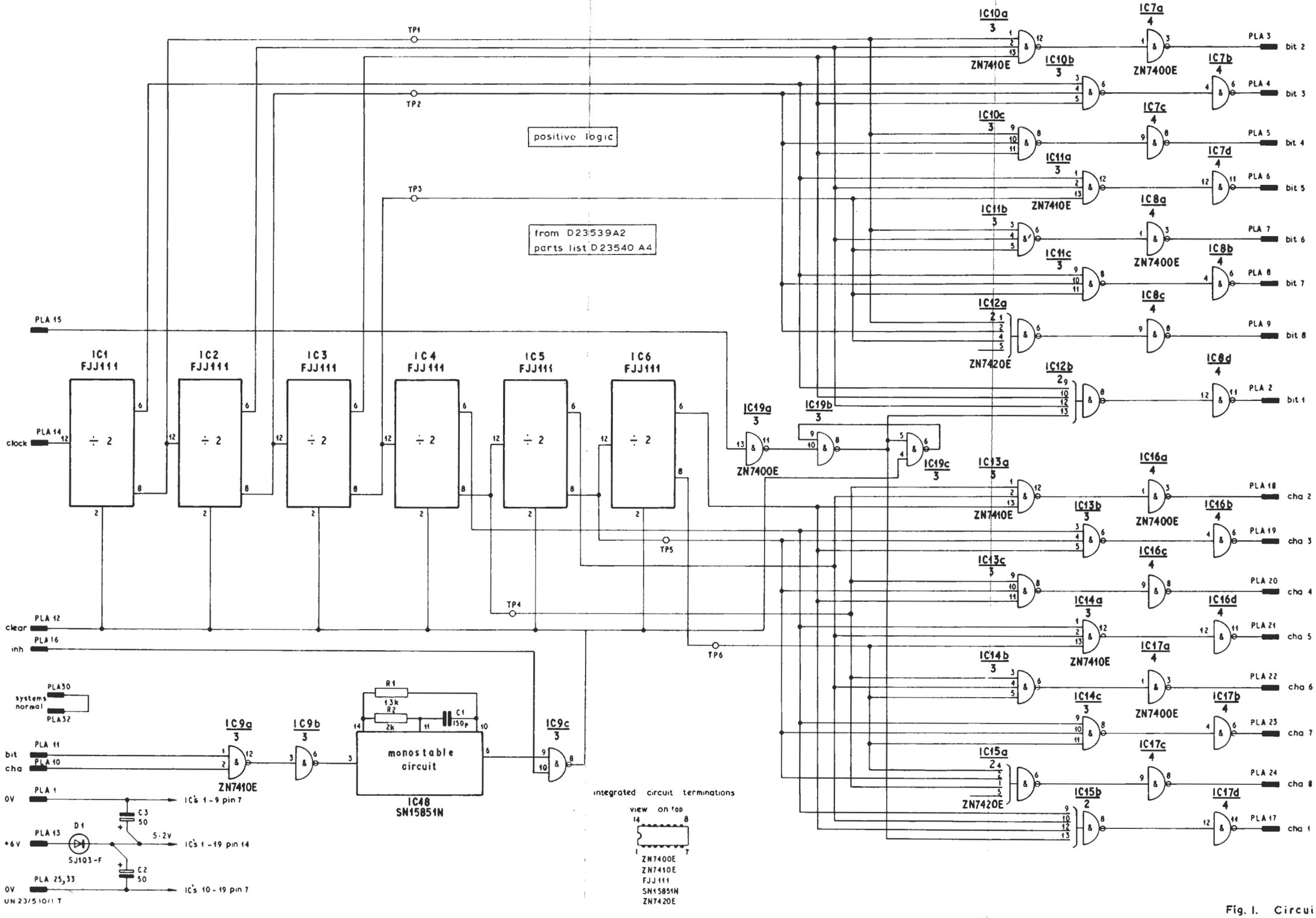
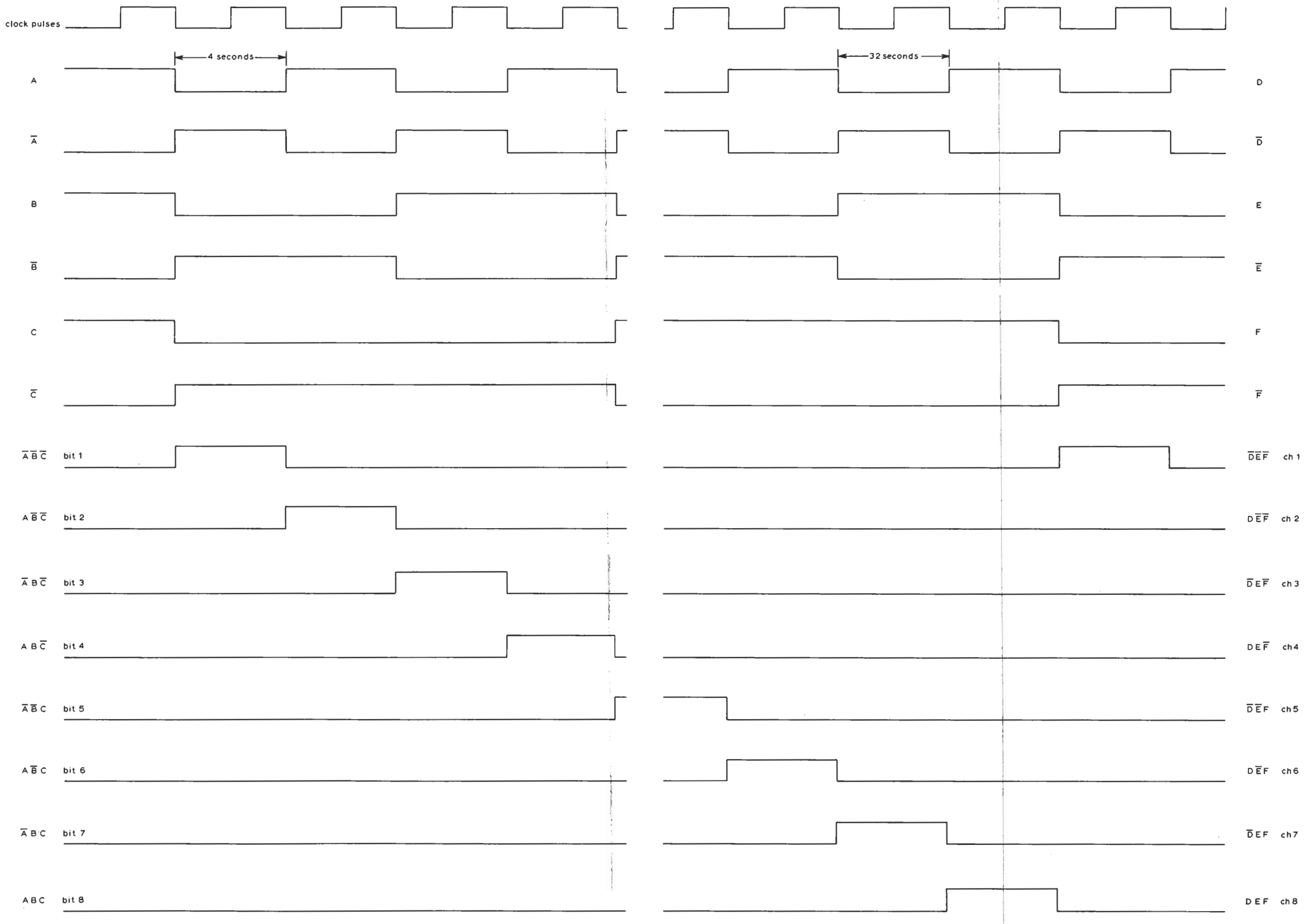


Fig. 1. Circuit of UN23/510



UN23/510/2T

Fig. 2. Waveforms of Bit and Channel Information

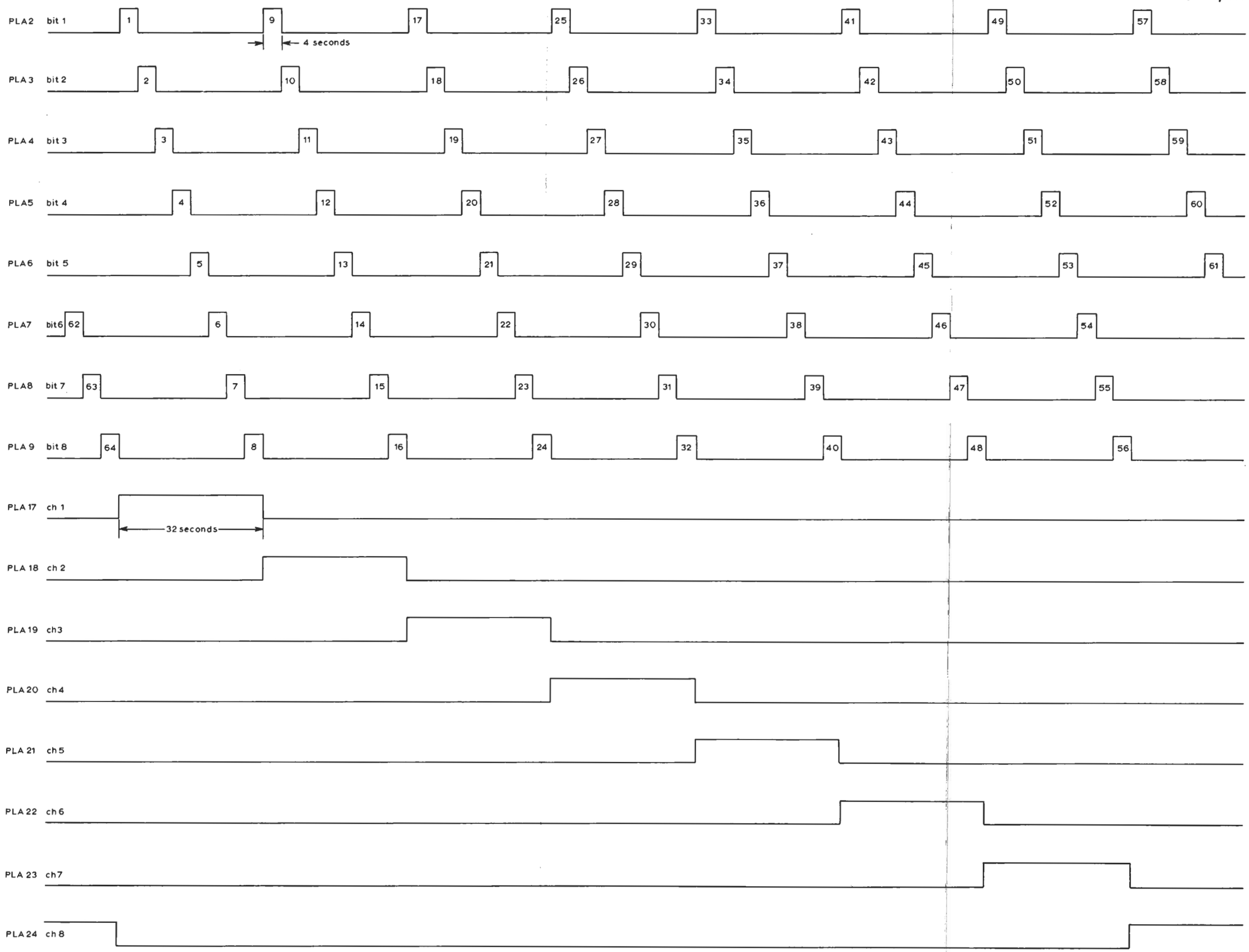


Fig. 3.
Relationship Between 'Bit' and 'Channel' Information