SECTION 6

NOISE DETECTOR UN20/506

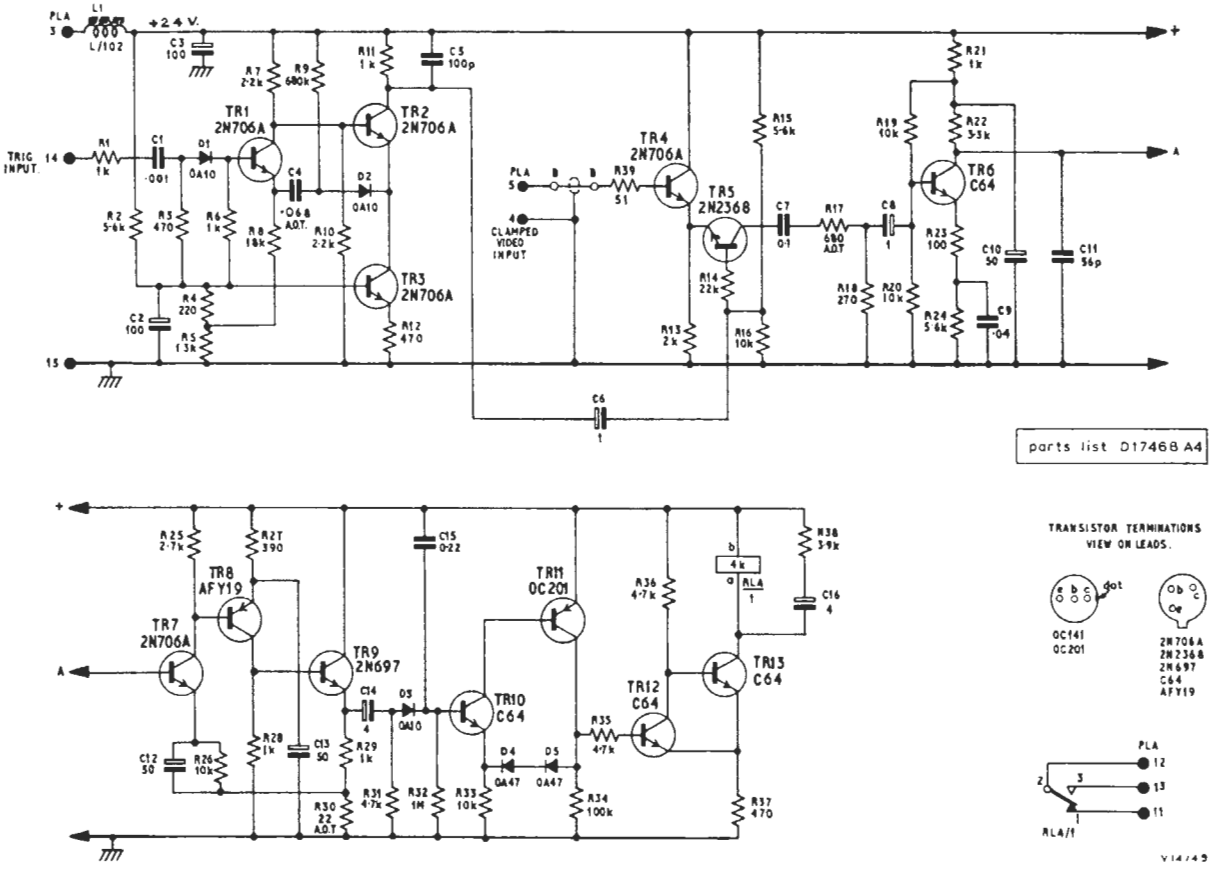

Fig. 6.1 Circuit of the UN20/506

Introduction

The UN20/506, accepts a clamped video signal and a noise-line trigger pulse as inputs: a relay is released if the noise level in a preselected line during field blanking is higher than —30 dB with respect to 0·7 volts p-p.

The UN20/506 is constructed on a CH1/12A chassis with index peg positions 19 and 27.

Circuit Description

The circuit of the UN20/506 is given in Fig. 6.1. Transistors TR1 to TR3 form part of an emitter-coupled monostable multivibrator[1] triggered at the start of the noise line. The output pulse of the multivibrator, used to gate out this line, is fed to the base of a switching transistor TR5.

The clamped video signal is fed to the emitter of the switching transistor via an emitter follower TR4. The gated noise signal is fed via an A.O.T. voltage-divider chain (*Sensitivity*) to the first stage of a four-stage amplifier. This stage, which includes transistor TR6, has a limited frequency response (—3 dB at 40 kHz and 860 kHz) and acts as a weighting network. The remaining three stages TR7—TR9 form a negative-feedback amplifier with a voltage gain of 42 dB.

The noise signal pulses are rectified by diode D3 discharging capacitor C15. During the remainder of the field period the capacitor charges through resistor R32 giving a sawtooth waveform whose amplitude at the base of transistor TR10 is related to the random amplitude of the noise in the video input signal. Transistors TR10 and TR11 form part of an amplifier which drives a Schmitt trigger circuit[2,3]. The Schmitt circuit has a backlash of about 3·5 volts and capacitor C16 is in parallel with relay RLA to accommodate the sawtooth input without too frequent switching of the relay.

Test Procedure

The UN20/506 is tested as part of an Automatic Monitor Major.

Bibliography

1. *Emitter-timed Monostable Circuit:* Mullard Technical Communications, Vol. 5, No. 49, July 1961.
2. Towers, T. D.; *Pumps and Schmitts:* Wireless World, August 1964.
3. Newell, A. F. and Tourtel, P. A.; *Transistor Backlash Circuits:* Mullard Technical Communications, Vol. 6, No. 51.

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