SECTION 5

NON-LINEARITY DETECTOR UN20/505

Introduction

The UN20/505, as used in Automatic Monitor Major MN2M/506 (see Instruction V.11), releases a relay if the non-linearity of the input waveform exceeds 20 per cent. The waveform consists of the staircase portion of a test-line signal and the subsequent sync-pulse. The sync-pulse is attenuated to have the same amplitude as the steps in the staircase under normal conditions.

The UN20/505 is constructed on a CH1/12A chassis with index peg positions 19 and 28.

Circuit Description

The circuit of the UN20/505 is given in Fig. 5.1. Transistors TR1 to TR3 form part of a negative-feedback amplifier with a voltage gain of 30 dB. This feeds a heavily-damped tuned circuit, the output of which consists of pulses whose amplitudes are proportional to the amplitudes of the transitions in the input waveform. These pulses are amplified in a second amplifier TR4 to TR6 with a gain of 26 dB.

The output of the second amplifier is passed through a peak rectifier D3. This is designed to give a d.c. bias at the negative end of diode D2 equal to 80 per cent of the amplitude of the largest positive-going pulse. Diode D2 conducts only during pulses which have an amplitude greater than this bias. These pulses are fed via a Schmitt trigger circuit[1,2] (TR9 and TR10) to a three-stage counter. The counter is reset immediately before each count by a positive-going reset pulse on pin 4. The outputs of the counter stages are gated by diodes D7, D13 and D15 to operate relay RLA if six pulses occur during each count.

Test Procedure

The UN20/505 is tested as part of an Automatic Monitor Major.

Bibliography

1. Towers, T. D.; *Pumps and Schmitts:* Wireless World, August 1964.
2. Newell, A. F. and Tourtel, P. A.; *Transistor Backlash Circuits:* Mullard Technical Communications, Vol. 6, No. 51.

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See page 5.3 for Fig. 5.1.

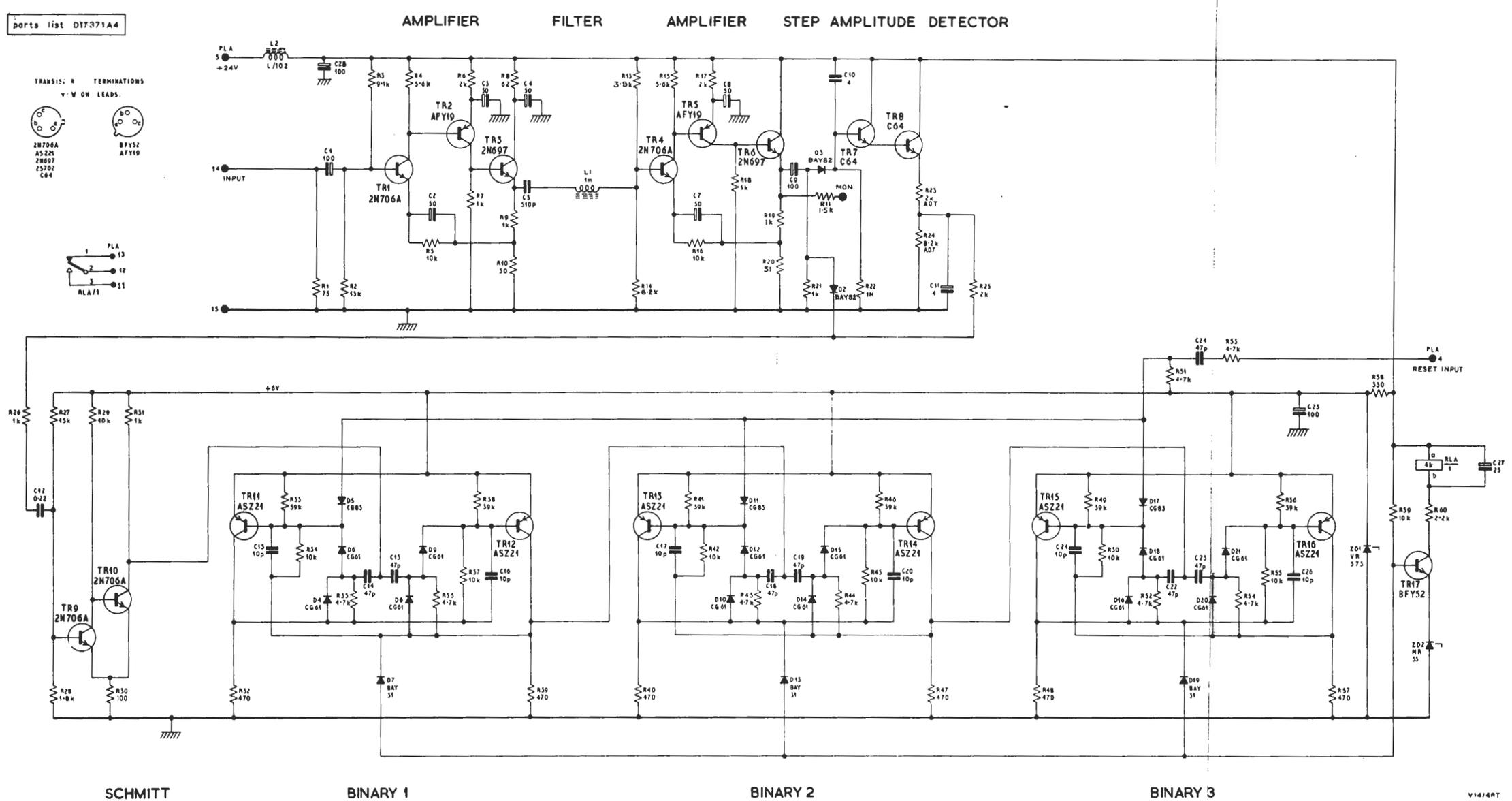

Fig. 5.1 Circuit of the UN20'505