SOUND IN SYNCS DIGIT BLANKERS UN1/614 AND UN1/614A

Introduction

Both the UN1/614 and the UN1/614A accept 625-line video signals which normally contain sound-in-syncs information. The UN1/614 provides a video output signal and a mixed-syncs output signal both with the sound-in-syncs information removed. The UN1/614A provides the same facilities as the UN1/614 and, additionally, contains a relay circuit which indicates whether or not sound-in-syncs information is present in the input signal.

The outputs of both units contain non-standard equalising pulses with a duration of 4·7 μs.

The units are described in blocked-text form in Fig. 1A, a circuit diagram is given in Fig. 1B and waveforms at various points in the circuit are given in Fig. 2. The layouts of the printed-wiring boards are given in Figs. 3, 4 and 5 *(Handbooks only)*. Power supplies are provided by an integral mains-fed PS2/91C Power Supplier. Input and output monitor sockets are mounted on the front panel of the unit, together with a mains-indicator lamp.

General Specification

Input Signal	composite video at 1 V p-p (with or without sound-in-syncs)
Permitted Signal Variation (for correct sync separation)	+3 dB to −6 dB
Input Impedance	more than 3 kilohms
Video Output	composite video with any sound-in-sync information removed, picture component at input level (±0·2 dB) sync component within ±20% of input level
Sync Output	1·5 V to 2 V p-p (non-standard equalising pulses)
Output Impedances	75 ohms
Digit Attenuation	greater than 30 dB
Blanking Transitions	±50 mV typical
Video performance	k-rating not more than 0·5%
Picture signal distortion factor	not more than 0·2%
Differential gain distortion	not more than 0·2%
Differential phase distortion	not more than 0·3°
Chassis	CH1/26A
Weight	1.25 kg (2·71 lb)
Coding pins	67 and 68
Power consumption	55 mA at 240 V, 50 Hz

NOTES

Encircled letters refer to waveforms in fig 2

*Replaced by PS2/120C on later units

TR1 TR2 SYNC DETECTOR

During sync pulses TR1 and TR2 conduct, C1 charges to a potential proportional to peak sync amplitude. R4 and C2 provide smoothing

TR3 TR4 COMPLEMENTARY EMITTER FOLLOWER

TR5 TR6 TR7 SYNC GATING STAGE

+ve-going switch-drive pulses turn on FET TR5 via TR7. When a switch-drive pulse ceases, TR5 cuts off. TR6 and D1 allow -ve going input signals to modify the switch-drive pulses so that TR5 functions correctly for a wide range of signal levels

TR8 TR9 LONG-TAILED PAIR SWITCH DRIVE STAGE

Accepts +ve going blanking pulses from X or Y. Feeds +ve-going pulses to sync gating stage and -ve-going pulses to picture-gating stage

TR10 TR11 TR12 PICTURE GATING STAGE

-ve-going switch-drive pulses cut off TR12 via TR10. When a switch-drive pulse ceases. TR12 conducts and passes the picture component of the signal. TR11 and D4 allow -ve-going input signals to modify the drive pulses so that TR12 functions correctly for a wide range of signal levels

SKB O/P mon

TR13 TR14 OUTPUT AMPLIFIER

Accepts the outputs of the sync and picture-gating stages. Provides a composite output with the same amplitude as the video input signal but with sound-in-syncs information removed

PLA 10 — video output

transistor terminations (view on leads)

TIS75 — 2N3702, 2N3704, 2N3711 — BCY71, BCY72, BC108, BC109, V405A, 2N697, 2N2219A, BFX88

integrated circuits (view on top)

MC851, MC846P, µL9601

integrated circuit (view on leads)

µA710

PLA 4, 6, 11, 15

X Y BLANKING PULSE LINK

4-µs pulse if X connected, 4·7-µs pulse if Y connected

IC2D NAND GATE

-ve-going output when digits are present and during field-blanking periods

IC5 RETRIGGERABLE MONOSTABLE

0V output when triggered by a -ve-going input, +5V output otherwise. Pulse duration 36 µs for picture lines, 800-900 µs for field blanking

TR26 RELAY DRIVER

When fed with a continuous train of 0V pulses (i.e. when sound-in-syncs digits are present on the input signal) TR26 is cut off. When fed with a +5V signal, TR26 conducts and RLA is energised

IC3 MONOSTABLE

Triggered by leading edge of syncs. Provides a 'clean' 20-µs pulse

IC4 MONOSTABLE

Pulse duration 4 µs, +ve-going output feeds X, -ve-going output feeds IC2B

PLA 1 — L — FS1 150mA — 1LP1 — 2 N — 3 E

PS2/91C POWER SUPPLIER

24V

TR28 TR29 POWER SUPPLY STAGE

Derives power supplies of +12V, -12V (with respect to earth) from the 'floating' 24V output of the PS2/91C

TR20 TR21 SYNC DETECTOR

TR20 conducts during syncs and charges C25 to a potential proportional to peak sync amplitude. R51 and C26 smooth the signal, TR21 removes the offset voltage due to TR20. The output is fed via divider network R52-R70 to pin 3 (ref. input) of IC1

PLA 5 — video input

TR16 TR17 INPUT AMPLIFIER

A two-stage feedback amplifier. R77 is adjusted to give 0 dB gain between *Video Input* and *Video Output*

SKA I/P mon

TR17 EMITTER FOLLOWER

L7 C21 C23 SUBCARRIER REJECTOR

Filters out any colour subcarrier components in the video signal

TR18 TR19 INVERTER AND EMITTER FOLLOWER

IC1 SYNC SEPARATOR

When the sync component of the video signal (pin 2) is more +ve than the reference potential (pin 3), +ve-going sync pulses are developed at pin 7. Overload protection is provided by D1

IC2A INVERTER

Produces -ve going syncs

IC2B NAND GATE

+ve-going output during sync pulse periods

IC2C INVERTER

Produces -ve going sync pulses

TR27 SYNC OUTPUT STAGE

Conventional emitter-follower

PLA 13 — m sync output

TR22 TR23 CLAMP

Clamps the output of TR19 at 0V during back-porch periods

TR24 TR25 CLAMP PULSE GENERATOR

TR24 generates +ve going clamp pulses from the differentiated output of TR25

+12V(A), -12V(A), +12V(B), -12V(B), +12V(C), -12V(C), -5·8V, +12V(D), -12V(D), +12V(E), -12V(E), +5·8V

UN1/614/1B

UN1/614/1A

Fig. 1A Blocked Text Diagram of the UN1/614

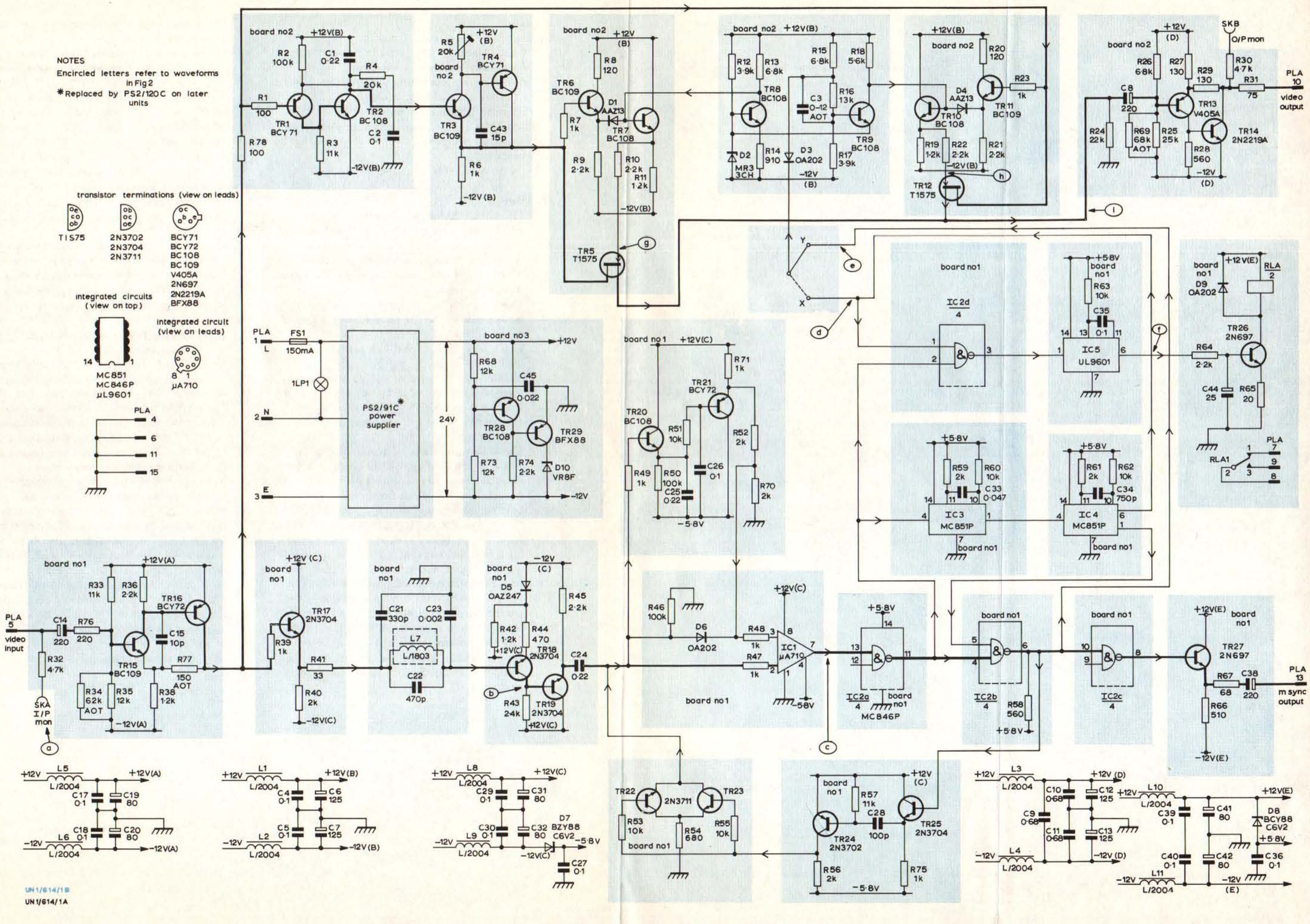

Fig. 1B Functional Circuit Diagram of the UN1/614

Alignment

Equipment and Test Signals Required

C.C.I.R. Linearity Test Waveform with 5-step staircase and field-sync component
Video waveform containing sound-in-syncs signal (or simulated sound-in-syncs digits)
Augmented pulse-and-bar waveform
Mixed syncs, synchronous with linearity waveform
Dual-trace oscilloscope
Avometer
0 - 10 dB Attenuator, adjustable in 1-dB steps.

Procedure

1. Check that Board No. 3 provides output of +12 V and −12 V (within ±0·1 V) with respect to earth.
2. Apply the linearity waveform at a level of +3 dB to the video input. Terminate the video input in 75 ohms.
   Monitor at TR18 collector. Check that with the input signal in the *Bar On* condition the sync component is not clipped.
3. Check that the d.c. level and gain of the two oscilloscope inputs are the same.
   Monitor pins 2 and 3 of IC1. Check that the inverted signal at pin 2 is clamped to 0 V during back-porch periods and that the d.c. at pin 3 corresponds to the half-amplitude level of the syncs on pin 2.
   Check that positive-going syncs, see Fig. 2(c), appear at pin 7 of IC1. If the input to IC1 is not clamped or the d.c. level at pin 3 is incorrect, then the output from pin 7 of IC1 will be either missing or distorted.
   Note: For the correct operation of IC1 the clamp circuit (TR22, TR23) which derives its input from the output of IC1, must be functioning correctly. For test purposes the clamp can be made to function independently of IC1 by applying mixed syncs with an amplitude of 4 V p-p (i.e. unterminated) to TR25 emitter. Ideally inverted mixed syncs should be used but these may not be readily available. Mixed syncs of normal polarity enable the operation of the clamp to be checked, but cause clamp-timing errors.
4. Check that negative-going syncs are present at pins 11 and 8 of IC2.
5. Check that IC3 produces 20-μs pulses (+2 μs) which are timed from the leading edges of the pulses present at pin 11 of IC2.
6. Check that the pulses appearing at the output of IC4 have a duration of 4 μs. If necessary, adjust the value of resistor R62 to obtain the correct duration.
7. Terminate the *Mixed Sync Output* (PLA 13) in 75 ohms. Check that mixed syncs with an amplitude of between 1·5 V and 2 V are present.
8. Terminate the *Video Output* in 75 ohms. Monitor at this point and adjust R77 for 0 dB gain through the unit.
   Check that the blanked sync level of the output signal is within +20% of the sync level of the input signal. Select C3 for minimum blanking transitions. (Note that C3 delays the blanking pulses and hence is limited in value by the need to blank the first digit.)
9. Apply an augmented pulse-and-bar signal to the input of the unit. Monitor at TR18 collector, see Fig. 2(b), and check that all chrominance information has been removed from the signal. Monitor at the *Video Output* and check that the k-rating and the luminance/chrominance ratio of the signal are within the specification.
10. Apply a signal containing sound-in-syncs digits to the unit. Monitor at the *Video Output* and check that the digits have been removed.
    Note: Sound-in-syncs digits are contained in the sync pulses which appear at IC1 pin 7 and IC2 pins 2, 4, 11. All other parts of the sync chain should be free of sound-in-syncs digits.
11. On the UN1/614A only, check that IC5 pin 6 is at 0 V and relay RLA is de-energised. Remove the input signal. Check that IC5 pin 6 is now at +5 V and RLA energised. Apply a video signal which does *not* contain sound-in-syncs information to the input of the unit. Check that a negative-going field-rate pulse with a duration of 800 to 900 μs appears at IC5 pin 6 and that relay RLA remains energised.

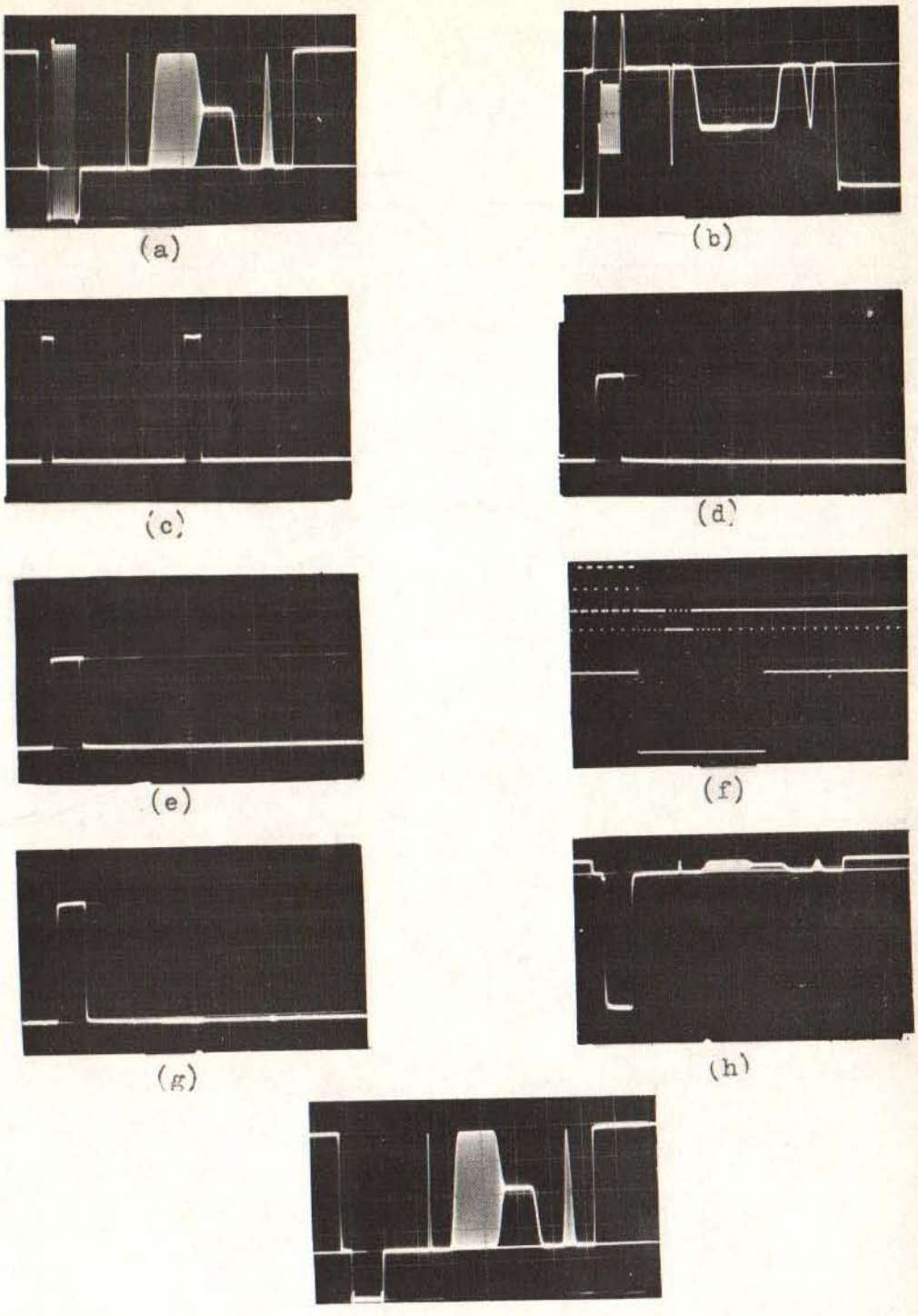

Fig. 2. Waveforms in the UN1/614

(a)	Input:	augmented pulse-and-bar with S.I.S. digits; amplitude 1 V p-p, timebase set to 5 μs/cm
(b)	TR18c:	augmented pulse-and-bar with S.I.S. digits; amplitude about 3·5 V p-p, (excluding transients) timebase set to 5 μs/cm
(c)	IC1 pin 7:	half-amplitude sync sample; amplitude about 4 V p-p, timebase set to 1 μs/cm
(d)	Point X:	blanking pulses; amplitude about 5 V p-p, timebase set to 5 μs/cm
(e)	Point Y:	blanking pulse; amplitude about 5 V p-p, timebase set to 5 μs/cm
(f)	Top trace:	video output (augmented pulse-and-bar without digits); amplitude 1 V p-p, timebase set to 0·2 ms/cm
	Bottom Trace:	IC5 pin 6, digit detector drive (no digits on input); amplitude about 5 V p-p, timebase set to 0·2 ms/cm
(g)	TR5 gate:	switch-drive pulses; amplitude about 3·5 V p-p, timebase set to 5 μs/cm
(h)	TR12 gate:	switch-drive pulses; amplitude about 4 V p-p, timebase set to 5 μs/cm
(i)	TR12 source:	video waveform with digits removed; amplitude 1 V p-p, timebase set to 5 μs/cm