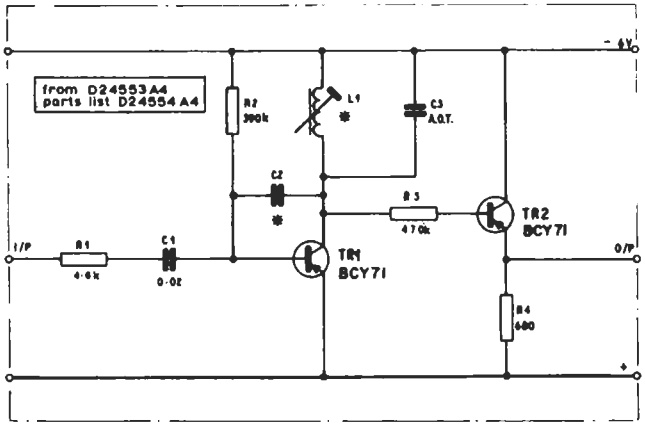
PARAMETRIC DIVIDER UN1/605A - C

Introduction

The UN1/605 is a parametric divider with a division ratio of 2. It is built on a printed card $1^3/_4$in x $4^5/_8$in and forms part of the UN15/503 Discriminator. The three versions are identical except for the frequency of the input signal: Type A, 41·66 kHz; Type B, 20·83 kHz; Type C, 10·415 kHz. The circuit diagram of Fig. 1 indicates component differences.

Parametric division depends on the availability of sufficient power at frequency 2f to drive a circuit containing a non-linear element and tuned to frequency f. Under these conditions continuous oscillations at frequency f will be generated. With low input levels, a parametric divider operates as an amplifier; it amplifies the input frequency and gives useful gain at frequencies where other methods fail or are difficult.



transistor termination
view on leads

BCY71

	L1	Inductance	C2
UN1/605 A	21A/116	56 mH	82p
UN1/605 B	21A/115	100mH	220p
UN1/605 C	21A/114	20 mH	390p

UN1/605/1

Fig. 1 Circuit of the UN1/605 Series of Parametric Dividers

Circuit Description

TR1, with its associated components, is the divider stage; TR2 provides a low-impedance output. The non-linear element is the effective value of C2 which depends on the gain of the stage. TR1 is cut off by the positive-going swing of the 2f input drive and energy is stored in C2 and in the capacitance of the base/collector junction of TR1. On the negative-going input swing TR1 is fully conductive and the stored energy is released into the tuned circuit and starts a train of damped oscillations at frequency f. On the next negative half cycle of the 2f input the energy stored in the previous posivite half cycle is released but, because it occurs at the wrong time, it merely limits the amplitude of the damped oscillation at this point of its swing. The next negative half cycle of the input releases energy again, this time augmenting the oscillation in the tuned circuit. Thus the oscillation is boosted once per two input cycles and the output signal, which is not sinusoidal, has a marked component at frequency f. There is no output if the drive is removed. The process is illustrated diagrammatically in Fig. 2.

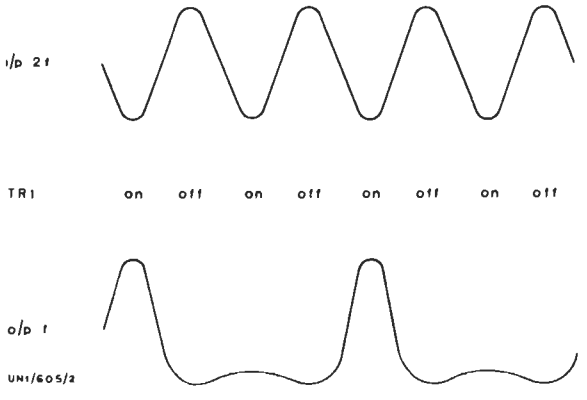


Fig. 2 Waveforms Illustrating Division Process

Maintenance

Routine maintenance is not required but the following points can be noted.

1. The frequency range of the divider should be approximately centred about the input frequency. This can be checked by connecting a source of frequency 41·66 kHz, 20·83 kHz or 10·415 kHz, as appropriate, and of about 5 volts p-p amplitude, to the input. Use an oscilloscope with probe connected to the output terminal as an indicator. The limits of the division range are indicated by the points at which the fundamental frequency just appears. The nominal value for the AOT capacitor C3 is 560pF for the A version and 1500pF and 4000pF for the B and C versions.

References

1. Designs Department Specification No.4.56(69)
2. "Wireless World" January 1964

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