

SECTION 69

GATING UNIT UN1/569 AND UN1/569A

Introduction

The UN1/569 accepts a 625-line composite video signal, mixed sync pulses and a field sync pulse together with an 800-kHz tone and produces two output signals. These signals are a clamped composite video signal and series of bursts of tone mixed with noise. These bursts correspond to the line sync pulses of the input video signal over most of each field. The UN1/569A is a 405-line version. These units are used in a Television Automatic Monitor Minor (see Instruction V.11).

The UN1/569 is constructed on a CH1/12A chassis with index peg positions 25 and 26.

General Description

A block diagram of the UN1/569 is given in Fig. 69.1. The video input signal is clamped to form one of the outputs. This output is also fed to a sync separator in which the 800-kHz tone is also inserted. The output of the sync separator, comprising bursts of tone sitting on sync pulses, is fed via a second clamp to a gate circuit which removes the pulse component of the waveform leaving bursts of noise and tone.

Circuit Description

The circuit of the UN1/569 is shown on page 69.3. The base of transistor TR1 is fed with pulses from the first clamp pulse generator thereby connecting the base of transistor TR2 to a source of fixed voltage (zener diode D1). Transistors TR2 and TR3 are connected as a Darlington-pair emitter follower. The clamped sync pulse voltage at the base of transistor TR4 is negative with respect to the emitter and so this transistor conducts during sync pulses. Potential divider R79 acts as a clipping level control and should be set to clip at about half the amplitude of the sync pulses. The 800-kHz tone is fed to the emitter of transistor TR4 where it is mixed with the sync pulses.

Transistors TR5 to TR7 form part of an amplifier feeding a similar clamp circuit.

The output of the second clamp circuit is fed to the base of transistor TR12 via the series gate transistor TR11. This transistor is switched on only in the sync pulses that occur during the output pulse of the gating pulse generator. During the time the transistor TR11 is switched off the voltage at the base of transistor TR12 is set by a potential

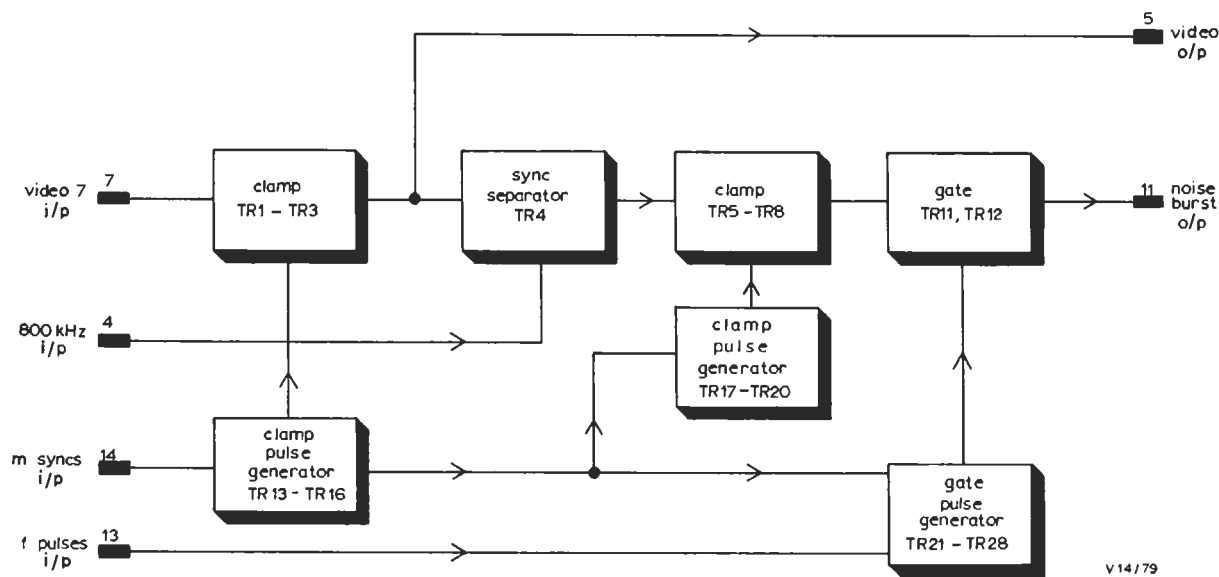


Fig. 69.1 Block Diagram of the UN1/569

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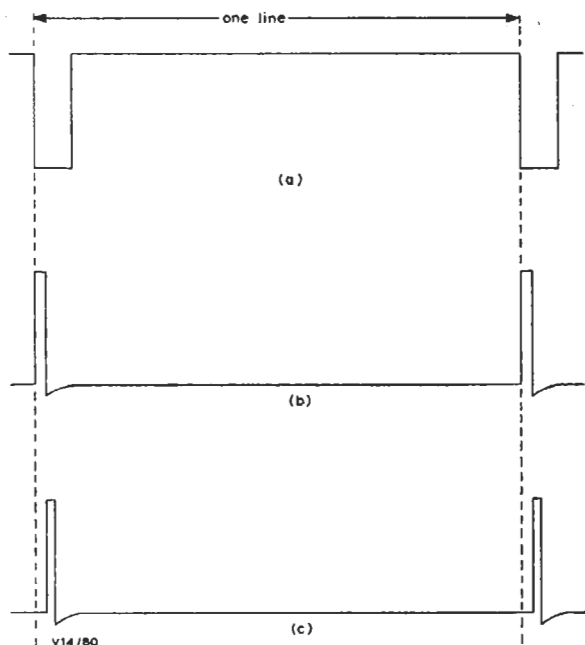


Fig. 69.3. Line Waveforms in the UN1/569

- (a) pin 14
- (b) TR16 emitter
- (c) TR20 emitter

Fig. 69.3 Line Waveforms in the UN1/569

divider R80. By means of this control the pulse component in the output waveform of transistor TR12 can be reduced to a minimum.

The mixed sync pulse input, Fig. 69.3(a), is differentiated (capacitor C16 and resistor R33) to generate the first clamp pulse, Fig. 69.3(b), at the emitter of transistor TR16. A second clamp pulse, Fig. 69.3(c) is triggered from the trailing edge of the first. This is fed to the clamp from the emitter of transistor TR20.

The field pulse input is differentiated and fed to a 1-6-ms monostable multivibrator which includes transistors TR21 and TR22. The trailing edge of the output pulse from this multivibrator is fed to a second monostable multivibrator which is set to

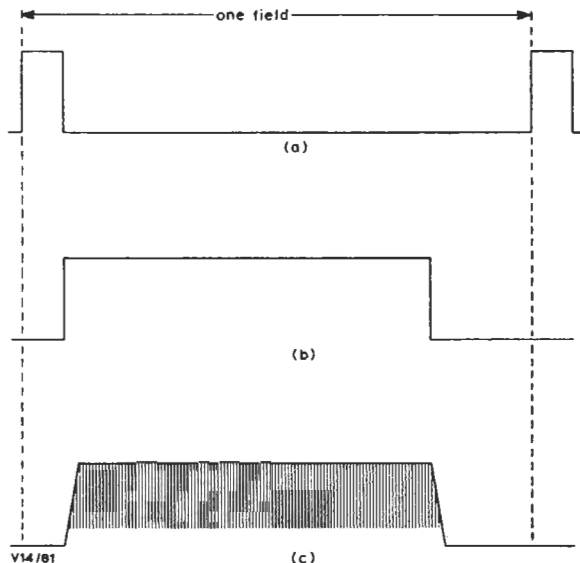


Fig. 69.4. Field Waveforms in the UN1/569

- (a) TR21 collector
- (b) TR23 collector
- (c) junction of D8 and R63

Fig. 69.4 Field Waveforms in the UN1/569

give a pulse that lasts for most of the field. The output of the second multivibrator is mixed with inverted pulses from the first clamp pulse generator to give a waveform as shown in Fig. 69.4. The field component in this mixed waveform is slowed down to avoid mistripping the gate-pulse emitter-coupled monostable multivibrator (transistors TR26 to TR28) which is of the type described in *Emitter-timed Monostable Circuit* published in Mullard Technical Communications, Vol. 5, No. 49, July 1961.

Test Procedure

The UN1/569 is tested as part of an MN2M/508 (see Instruction V.11).

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