

ATTENUATION AND DELAY UNIT UN1/565

Introduction

The UN1/565 is a two-channel device which amplifies two separate but nominally-identical signals, known as the compared signal and the reference signal. A delay line included in the reference channel partly offsets a timing difference between the signals.

Provision is made for preset control of level on one channel.

A U link on the front panel enables a common input to be applied to both channels.

The unit forms part of the Television Automatic Monitor (Transmitter) MN2M/505. It is housed in a CH1/26A chassis with index peg positions 16 and 20.

General Specification

Input Signal Level	550 mV p-p
Output Signal Level	3 V p-p
Max Excursion of Output Level	6 V p-p
Input Impedance	3.2 kilohms
Output Impedance	less than 50 ohms
Nominal Source Impedance	75 ohms (max)
Response	-3dB at 5 MHz relative to 1 MHz
Time Delay in the cable	$1.3 \pm 0.2 \mu\text{s}$
Supply	60 mA at + 24 V

Circuit Description

The circuit of the unit is given in Fig. 1. Both channels are identical apart from the delay line included in the reference channel. The input resistors provide correct termination for the delay line. A low-impedance source, not greater than 75 ohms, is essential; the sum of source impedance and R1 must be 1600 ± 200 ohms. The delay line feeds an emitter-follower impedance converter via a preset level control.

R7/C8 and R37/C18 form weighting networks with an attenuation of 6 dB per octave. Following the networks the signals are amplified to give an output of about 3 volts p-p but, because of the loss of the d.c. component in the interstage couplings, the total swing is about twice this. Considerable negative feedback is used in the amplifiers and, to ease stability problems, a dominant phase-correcting network is used in the collector circuit of TR3 and TR13.

The U link allows a common input to be applied to both channels for test purposes and enables any unbalance to be detected. This test facility is not used earlier in the circuit because the delay line introduces timing differences and the level control introduces amplitude differences.

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See overleaf for Fig. 1

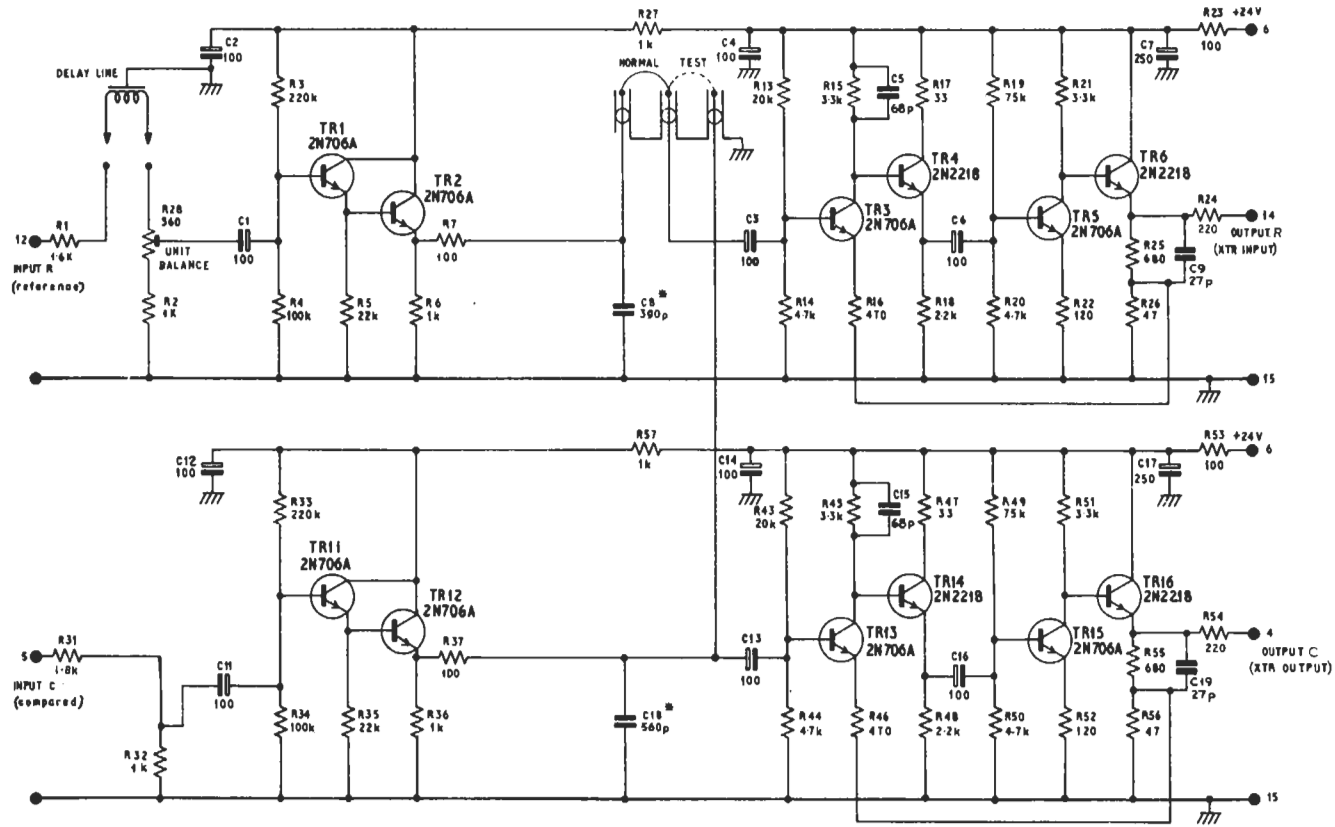


Fig.1 Circuit of the UNI/565

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TRANSISTOR TERMINATIONS.
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*Values adjusted on test