SECTION 18

MAINS DISCRIMINATOR UN1/518

Introduction

The UN1/518 has inputs at picture frequency, field frequency and mains frequency; it produces a d.c. output signal for frequency control of an external oscillator and two other d.c. signals which are used to inhibit external sampling circuits.

The UN1/518 contains a pulse-detector circuit, similar to that of the UN1/542, and a sampling circuit. When picture-frequency pulses are not fed to the pulse-detector circuit, the mains-frequency input is sampled by the field-frequency input to produce the d.c. control voltage. The inhibiting signals are produced by the pulse-detector circuit.

The UN1/518 is constructed on a CH1/12A chassis with index peg positions 7 and 16.

Circuit Description

Fig. 18.1 shows the circuit of the UN1/518. The behaviour of the pulse detector in response to a positive-going picture-frequency input pulse on pin 14 is given in Table 1.

TABLE 1

Circuit Reference	*Input to Pin 14*	*No Input*
Relay S	Released	Operated
Pins 6 and 7	Open Circuit	—6 volts
Pin 5	—6 volts	Positive-going field-frequency pulses from slaved sync separator
TR4 and TR5	Cut off	Cut off except during field pulses

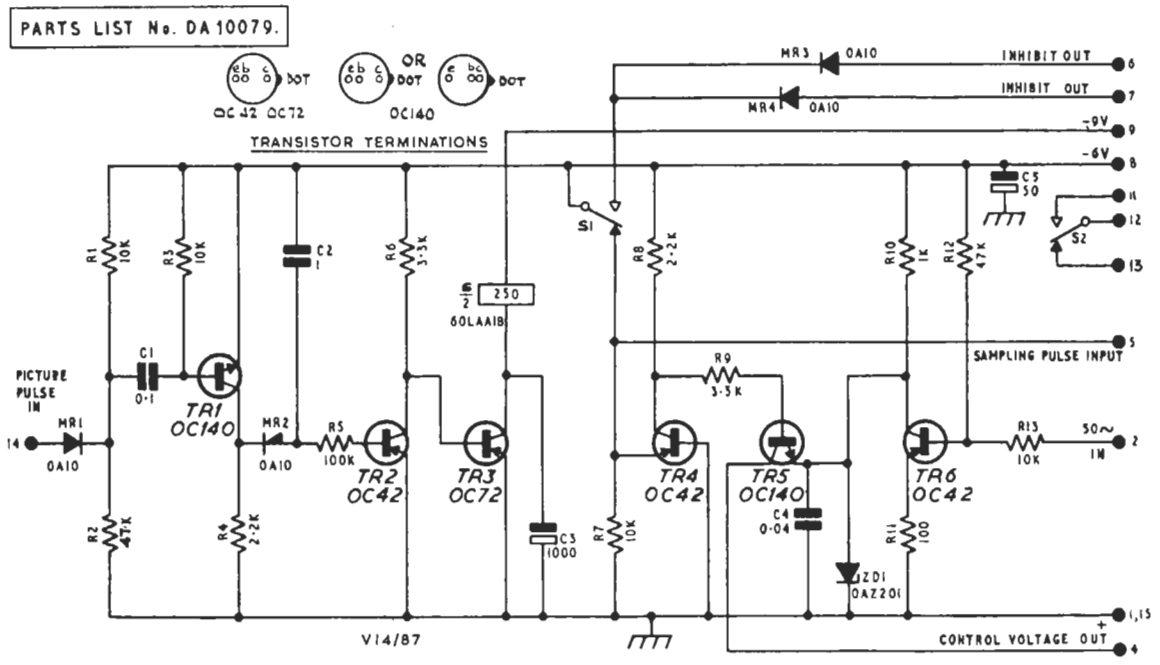

Fig. 18.1 Circuit of the UN1/518

The UN1/518 is fed with a 50-Hz signal on pin 2. This signal is clipped at the collector of transistor TR6 by the zener diode (—5·1 volts) and by the bottoming of the transistor (about —0·5 volts). This ensures that transistor TR5 is cut off except during the field pulses fed in on pin 5; i.e. provided there is not an input on pin 14 (relay S operated). Capacitor C4 provides a source of charge for the 1 μF capacitor at the collector of transistor TR5 (capacitor C3 in a UN1/517).

Test Procedure

The UN1/518 is tested as part of a Picture Synchroniser UN1/528.

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