SYNCHRONISING PULSE SEPARATOR UN1/510 SERIES

Introduction

The UN1/510 accepts a composite video signal or a feed of mixed-sync pulses and provides a feed of positive-going mixed-sync pulses and two feeds of negative pulses which have durations of 2·4 μs and 2·8 μs.

The UN1/510A is intended for colour working and provides, in addition to the outputs listed above, an amplified version of the input signal.

Both units are constructed on CH1/12A chassis with index-peg positions 3 and 16. Power supplies at +12, +4 and −4 volts are required.

General Specification

Input Signal Amplitude	0·25 V p-p
Input Impedance	high w.r.t. 75 ohms
Output Signal Amplitudes	
Inverted sync pulses	11 V p-p
Delayed pulses	1·8 V p-p
Amplified input signal (UN1/510A only)	0·9 V p-p

Circuit Description

The circuit diagram of the UN1/510 is given in Fig. 1 and that of the UN1/510A is given in Fig. 2. The following description applies specifically to the UN1/510 but is largely applicable to the UN1/510A also. The UN1/510A variations are dealt with at the end of this description.

The input signal is applied to an amplifier comprising transistors TR1 to TR6 which increases the signal amplitude to 5 volts peak-to-peak. The signal is then clamped at the bottom of syncs by the action of diode D1 which is driven into conduction by positive-going pulses derived from TR11. The clamping time-constant is very short and this causes low-frequency loss in the broad pulses. Suitable correction is applied in the following stage by the circuit comprising R23, R24 and C8; an undistorted signal is applied via emitter-followers TR8 and TR9 to the sync-separator stage TR10.

Positive-going sync pulses are produced at the collector of TR10. A feed of these pulses forms the inverted sync-pulse output of the unit[1] and a further feed is applied to the diode clipper D2 which operates at a level of +8·5 volts. Two feeds of clipped pulses are taken from the anode of D2. One feed is applied via emitter-follower TR11 to the clamp diode D1, as mentioned earlier, the other feed is applied to transistor TR12.

Emitter-follower TR12 drives the series-connected delay lines X1 and X2. The far end of X2 is connected to the 4-volt line which acts as a signal earth so that pulses fed into the delay lines are inverted and reflected back by the short-circuit at its far end. Thus the waveform at the emitter of TR12 consists of a 4-μs positive-going pulse followed after a short delay by a 4-μs negative-going pulse. A signal is taken from a tap on delay line X1 and applied to TR14; this signal starts 0·6 μs later and finishes 0·6 μs earlier than the signal developed at the emitter of TR12. Thus pulses with a duration of 2·8 μs are produced at the emitter of TR14. Only the negative-going pulse is used, the residual positive-going pulse is removed in the subsequent unit. A second signal taken from a tap 0·2 μs further along delay line X1 is applied to TR13, the pulses at this point have a duration of 2·4 μs. As before, the residual positive-going portion of the output waveform is removed in the subsequent unit.

UN1/510A Variations

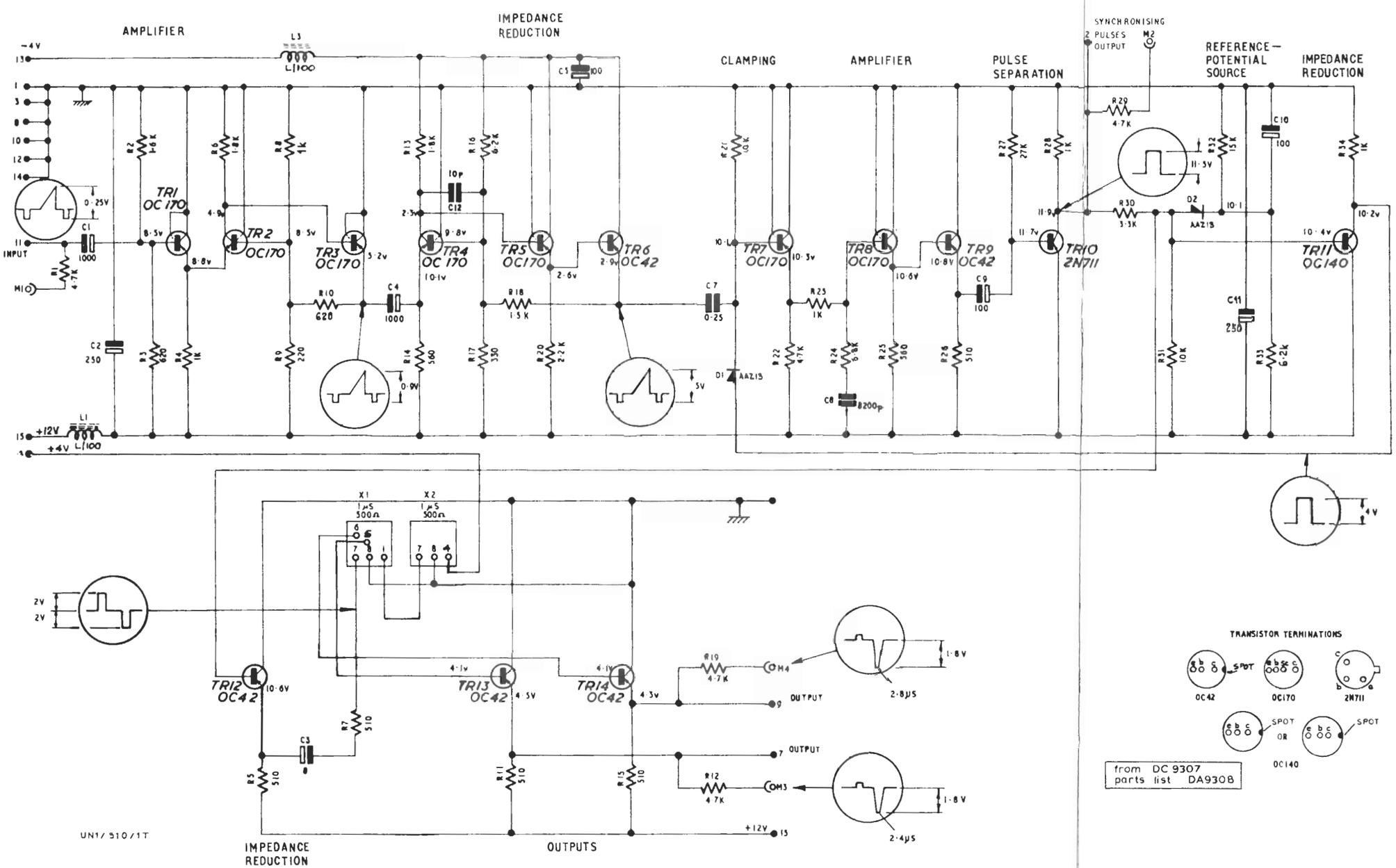
In the UN1/510A (see Fig. 2) the signal developed at the emitter of TR3 is applied to TR4 via a subcarrier filter which removes any chrominance information from the signal. The output from TR3 is applied also to an associated burst error amplifier[3] for use as a phase reference for colour-burst stabilisation.

Alignment and Maintenance

See parent unit [1,2].

References

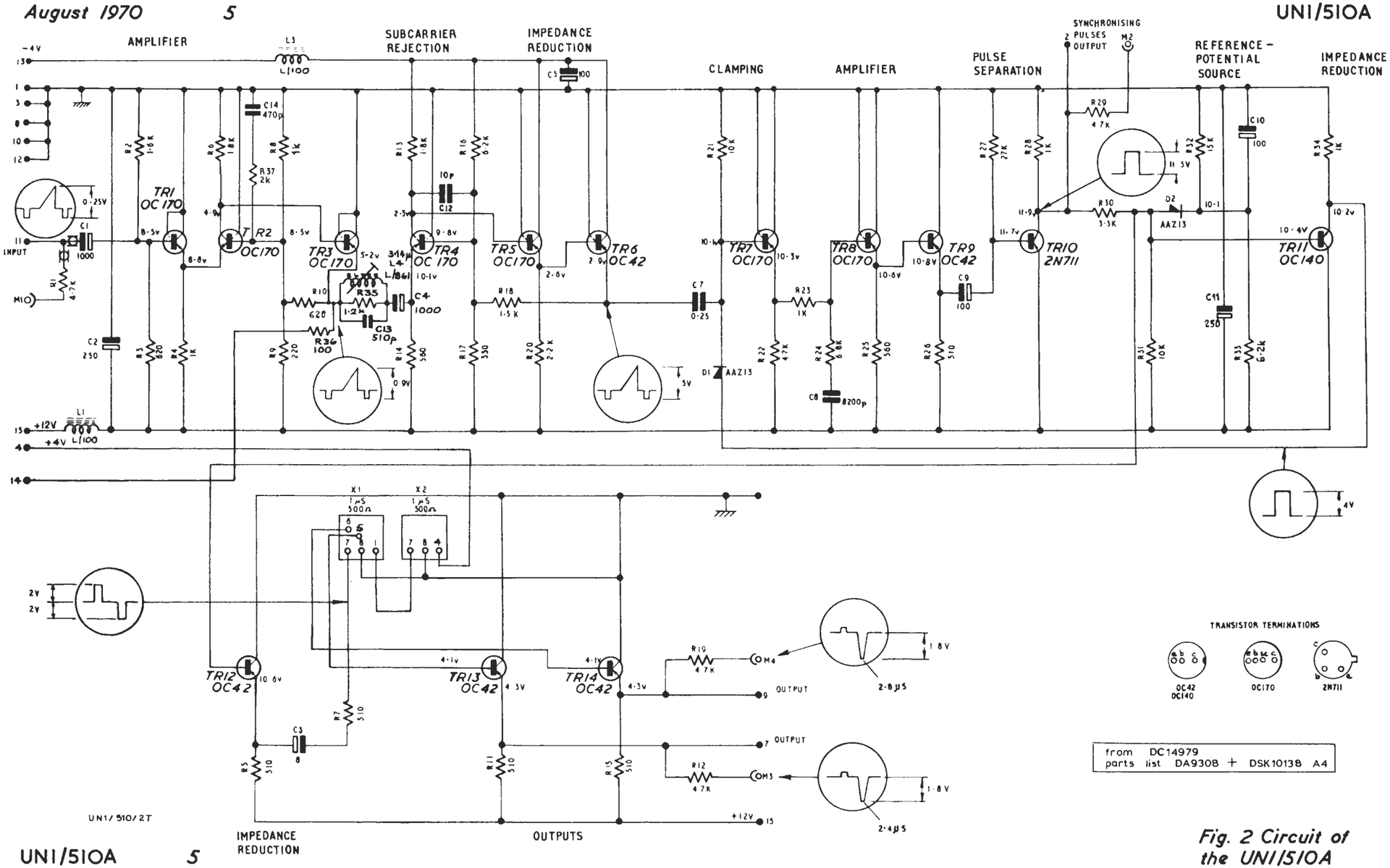
1. Line-store Standards Converter CO6/501A
2. Sync Pulse Stabilising Amplifier AM18/503,A
3. Burst-error Amplifier AM1/558
4. Designs Department Technical Memorandum No. 8.129(62)
5. Designs Department Technical Memorandum No. 8.240(67)
6. Designs Department Specification No. 8.70(62) TES 11/68



TRANSISTOR TERMINATIONS

from DC 9307
parts list DA9308

Fig. 1 Circuit of the UN1/510



TRANSISTOR TERMINATIONS

from DC14979
parts list DA9308 + DSK10138 A4

Fig. 2 Circuit of the UNI/510A