# GENLOCK COMPARATOR UNIT UN17/523

## Introduction

The UN17/523 forms part of the sync-pulse timing comparator[1] used in the BBC fast-genlock system[2].

The unit accepts pulses used in the associated comparator unit[3] and operates on the *Advance, Retard* and *Fast* outputs of the comparator by reducing the dead-spaces to generate *Retard, Advance, Fast* and *Extrafast* error control signals for use in the fast-genlock mode. All error signal outputs are inhibited until a d.c. *Genlock* control signal is received and the *Fast* and *Extrafast* signals are not sent until the required input conditions have existed for one second. The genlock error control signals are listed in Table 1; voltage tolerances are given in Table 2.

The UN17/523 is constructed on a CH1/43B (A-size) chassis with a 25-pole ISEP connector using coding pegs 1, 6 and 9. A chassis extender CH1A/8 may be required for maintenance.

## General Specification

*Pulse Inputs*

| | |
|---|---|
| Remote line | 6 V p-p |
| Remote picture | 6 V p-p 0 V |
| Local line | 6 V p-p maximum |
| Local picture | 6 V p-p amplitude |
| Local field | 4 V p-p |

*Control Inputs*

| | |
|---|---|
| Error control signals $A', R', F'$, | Error: −5 V nominal |
| | No error: 0 V nominal |
| GENLOCK | −5 V nominal |

*Control Outputs*

| | |
|---|---|
| Genlock error control signals | Error: −5 V nominal |
| $A'_g$, $R'_g$, $F'_g$, $XF'_g$, | No error: 0 V nominal |
| ENABLE | 0 V nominal |

TABLE 2

| *nominal voltage* | *actual voltage* |
|---|---|
| 0 | 0 to −1·5 |
| −6 | −4·5 to −6·0 |

*Power*

| | |
|---|---|
| Input | −12 V d.c., 210 mA |
| Output | −5 V d.c. (for *Genlock* control) |

*Temperature Range* 0°C to 45°C ambient

*Weight* 0·4 kg (14 oz)

## Circuit Description

Fig. 1 shows the logic diagram of the UN17/523, annotated to describe the operation. The full circuit diagram of the unit is given in Fig. 2.

## Maintenance

The UN17/523 is tested as part of the parent unit[1]. Routine maintenance is not possible.

## References

1. Error Signal Generator (Genlock) GE1M/568
2. *Picture Source Synchronising;* Instruction P.1, Section 4
3. Comparator Unit UN17/506

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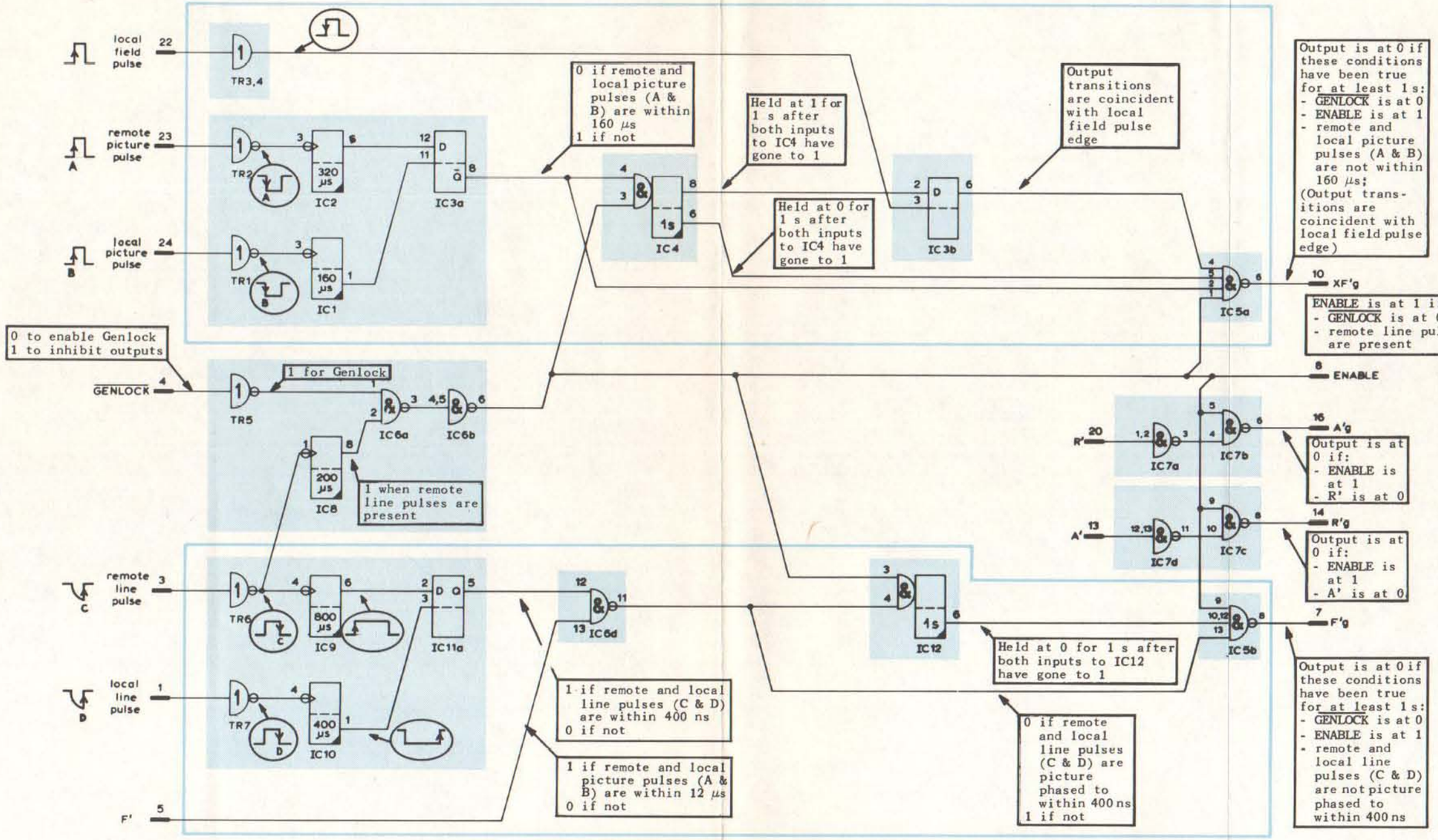
**Table 1**

| *Correction Mode* | *Remote Timing (w.r.t. local pulses)* | *Error control signals (V)* | | | |
|---|---|---|---|---|---|
| | | $A'_g$ | $A'_g$ | $F'_g$ | $XF'_g$ |
| Extrafast Retard | more than 160 μs late | 0 | −6 | −6 | −6 |
| Fast Retard | between 160 μs and 400 ns late | 0 | −6 | −6 | 0 |
| Retard | between 400 ns and 50 ns late | 0 | −6 | 0 | 0 |
| Normal | less than 50 ns | 0 | 0 | 0 | 0 |
| Advance | between 50 ns and 400 ns early | −6 | 0 | 0 | 0 |
| Fast Advance | between 400 ns and 160 μs early | −6 | 0 | −6 | 0 |
| Extrafast Advance | more than 160 μs early | −6 | 0 | −6 | −6 |



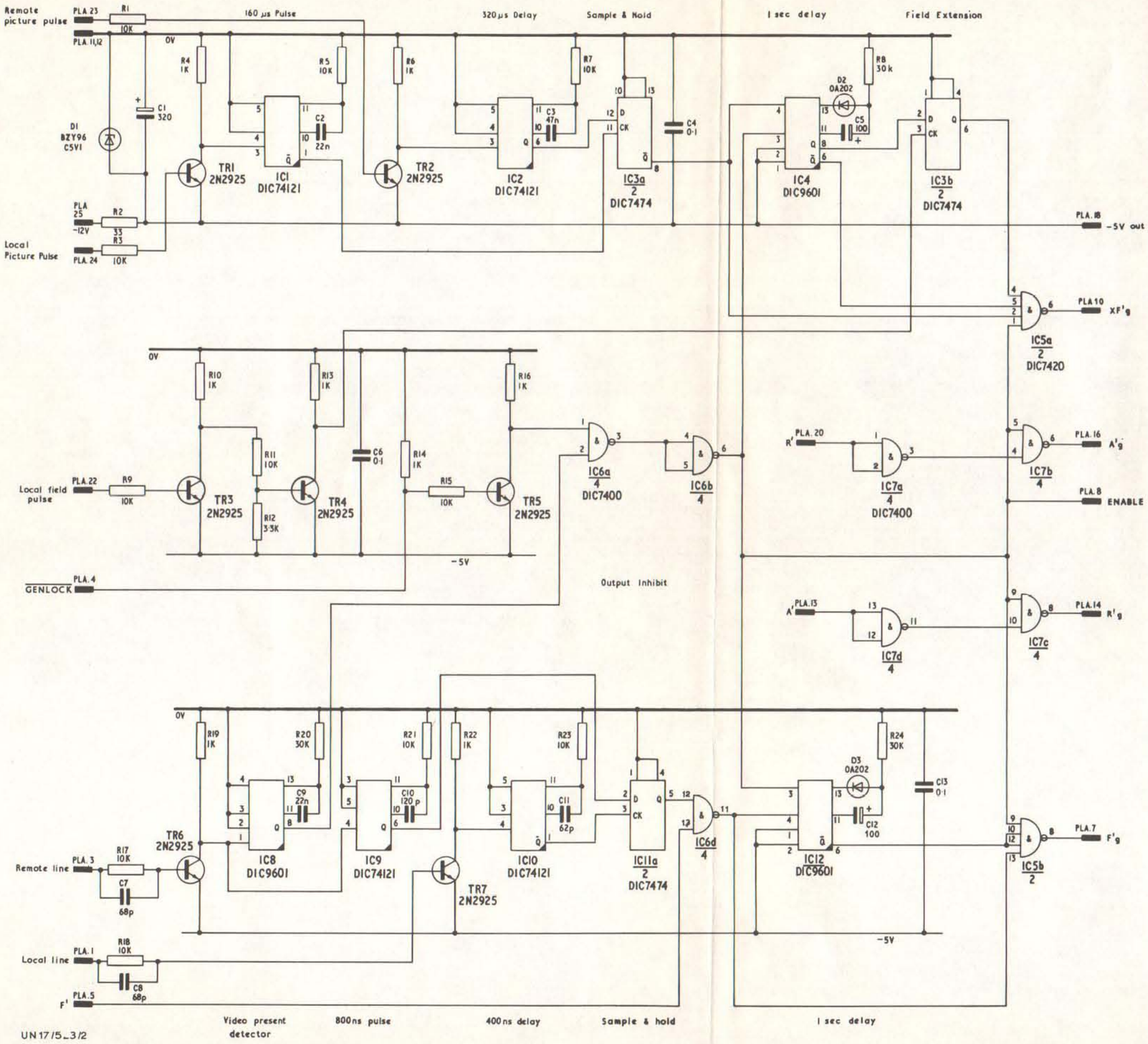

UN17/523/1A
UN17/523/1B
UN17/523/1C

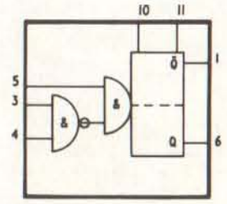


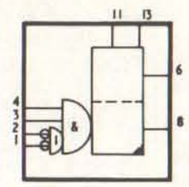
*Fig. 1. Logic Diagram of UN17/523*

from D 30513 A2 iss 2
parts list D 30514 A4

NOTE:-
1. Section Ic11b, Ic6c not used.
2. Ic1 - Ic12 incl - pin 14 (0V)
pin 7 (-5V)





DIC74121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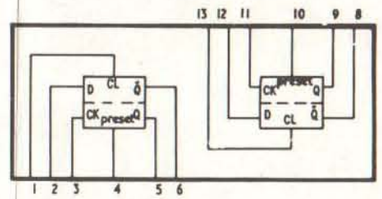
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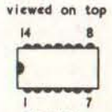
transistor terminations view on leads

2N2925

integrated circuit terminations viewed on top



DIC74121
DIC9601
DIC7474

*Fig. 2. Circuit Diagram of the UN17/523*