INPUT LOGIC DELAY UNIT UN14/4

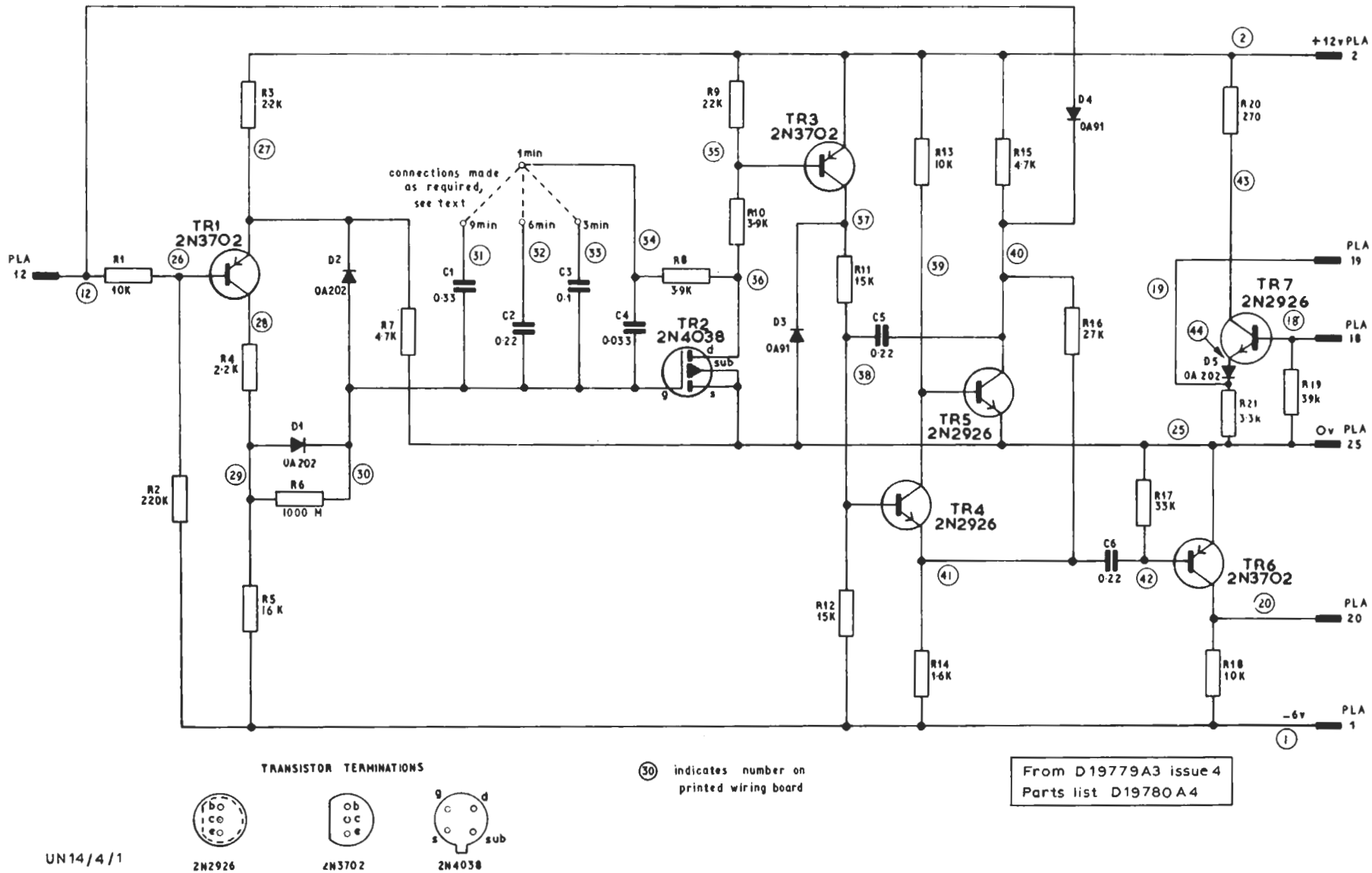

Fig. 1. Circuit of the UN14/4

Introduction

The UN14/4 is designed as part of the Automatic Fault Reporter PA2M/7A. The unit accepts two inputs. One input is normally held at a potential of three volts positive with respect to earth; if the input rises to about nine volts positive a preset timing sequence begins. Provided that this input is held at the nine-volt level for the duration of the timing sequence of between one and 19 minutes, a 1-ms positive-going 6-volt output pulse is generated and the input is momentarily earthed. The other input is either an earth or 12 volts positive and is taken via an emitter-follower stage direct to an output pin on the unit.

The unit is built on a BBC/I.S.E.P. printed wiring board which is fitted with a 25-way connector. Sections 3, 5 and 7 are removed from the coding device on the connector.

Circuit Description (Fig. 1)

Main Input

Normally the input on PLA12 is held at about three volts positive, and transistors TR1 and TR2 are saturated. When TR2 is conducting, its drain is at roughly earth potential and transistor TR3 is saturated. The collector of TR3 is held at earth potential by diode D3; TR4 is saturated and TR5 is cut off.

Transistor TR2 is an insulated-gate f.e.t. which is connected in a timing circuit. Feedback is applied betwen drain and gate via R8 and C4. The timing period can be increased by connecting one or more of the capacitors C1, C2 and C3 in parallel with C4. The range of potentials that can be applied to the gate is limited by diodes D1 and D2.

If the input is raised to nine volts positive, transistor TR1 is cut off, diode D1 is reverse-biased and the selected timing capacitors begin to charge through resistor R6, which has a value of 1000 megohms. When the timing capacitors are charged, transistors TR2, TR3 and TR4 are cut off and TR5 begins to conduct. Feedback through capacitor C5 increases the speed at which TR4 cuts off and at which TR5 starts conducting. When capacitor C5 is discharged, feedback via resistor R16 causes TR4 to saturate and TR5 to cut off; C5 at once begins to charge again and transistor TR4 to cut off. This cycle repeats during the time that transistor TR3 is cut off and generates a rectangular waveform at the emitter of TR4.

When transistor TR3 conducts again, the output from TR4 is a single negative-going pulse of one millisecond duration. This is applied to a common-emitter amplifier TR6 and to the output of the unit on PLA20.

When transistor TR5 is conducting its collector is effectively at earth potential, and this earth is connected to the input via diode D4, thus inhibiting the action of an associated unit[1]. Normally this causes the positive nine-volt potential at the input to be removed and transistor TR1 to saturate. TR2 and TR3 therefore conduct and prevent further pulses from being generated and passed to the output.

Secondary Input

Transistor TR7 is an emitter-follower. An input to PLA18 is presented at PLA19. This stage is used solely to produce a low output impedance.

WARNING

TR2 is an insulated-gate field effect transistor; its input resistance is of the order of 10^{15} ohms. On no account should the gate be allowed to become open-circuited. If it does, static charges are almost certain to destroy the transistor.

Test Procedure

The UN14/4 is tested as part of its parent equipment.

Continued overleaf

TABLE 1

Node	*Voltage*	*Node*	*Voltage*	*Node*	*Voltage*
1	−6·0	26	+4·0	37	+12·0
2	+12·0	27	+4·6	38	−1·5
12	+4·0	28	+4·5	39	−2·1
18	+3·0	29	+2·6	40	+9·9
19	+1·7	34	+0·57	41	−2·2
20	−6·0	35	+11·7	42	0
25	0	36	+0·57	43	+11·9
				44	+2·3

Maintenance

The voltages given in Table 1 relate to points designated by so-called 'node numbers' on the printed wiring board. The voltages were measured on an Avometer Model 8 and are with respect to PLA25.

Fault Conditions

If the timer does not work with any combination of timing capacitors the possibility is that f.e.t. TR2 is faulty. The method of checking this is:

(a) Check the voltage at node 36, the drain of TR2. This should be +0·57 volt with respect to PLA25

(b) Connect a 10-kilohm resistor between node 30, the gate of TR2, and node 1, PLA1. Measure the voltage at node 36. This should be +11·3 volts with respect to PLA25.

If the timer works correctly for short periods but does not time over longer periods of say 15 minutes, check the leakage of the timing capacitors and the reverse resistance of diodes D1 and D2. These diodes should have a maximum reverse current of 0·1 microampere with an applied voltage of 150 at an ambient temperature of 25 degrees C.

References to Typical Associated Equipment

1. Input Change Detector Unit UN20/5.

LPB9/72