Instruction V.14
Part 13

SECTION 4

BLACK LEVEL CLAMP UN13/504

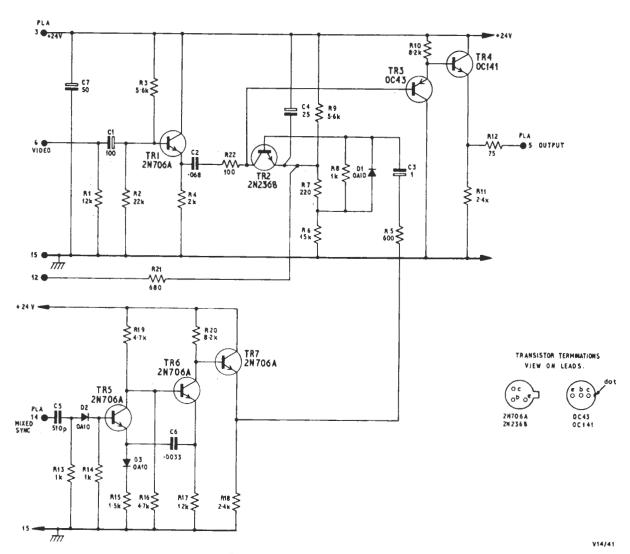


Fig. 4.1 Circuit of the UN13/504

Introduction

The UN13/504 accepts a video signal, mixed sync pulses and a d.c. signal; it clamps the video signal during the back porch and provides for periodic changes in the clamping level effected by the d.c. input.

The UN13/504 is constructed on a CH1/12A chassis with index peg positions 19 and 26.

Circuit Description

The circuit of the UN13/504 is given in Fig. 4.1. The sync pulses are differentiated by R13 and C5 and the trailing-edge pulses are applied to the base of transistor TR5 via diode D2. Transistors TR5 and TR6 form a part of an emitter-coupled monostable multivibrator¹. Transistor TR7 is an emitter follower for the output pulses of the multivibrator

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(duration $3.5 \mu s$) fed to the base of the switching transistor TR2.

The input video signal is fed via an emitter follower TR1 to the collector of the switching transistor. The emitter of transistor TR2 is at a potential of +17.5 volts, except when a potential of +24 volts is periodically applied to pin 12. Diode D1 prevents the reverse bias on the base of transistor TR2 from being excessive.

Complementary transistors TR4 and TR5 are connected as a cascaded emitter-follower output stage.

Test Procedure

The UN13/504 is tested as part of an Automatic Monitor Major; see Instruction V.11.

Bibliography

1. Emitter-timed Monostable Circuit: Mullard Technical Communications, Volume 5, No. 49, July 1961.

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