SECTION 2

TELEVISION TEST GENERATOR TV/TG/1

Introduction

The Television Test Generator TV/TG/1 produces a composite television signal for test purposes, of 1 volt d.a.p. from an output impedance of 75 ohms. The sync-pulse waveforms are similar to those employed in the television service, but the frame-sync signal can be suppressed when required. If desired, the frequency of the sync signals can be locked to the supply mains frequency, or to that of an external source. Satisfactory locking occurs over the range of frequencies 47·5–51 c/s. The picture signal can comprise a sawtooth, one of six available pulse signals, or an external signal. To all of these picture signals, a continuously-variable d.c. component can be added.

The unit is mounted on a 19 × 24 $\frac{15}{32}$ in. panel, suitable for bay mounting; when so mounted the unit projects through the bay. The signal output is fed to two *Musa* plugs at the front panel and two similar plugs are provided to receive the external signal input. When the sync-signal frequency is to be locked to that of an external source, the signal from the source is applied to a standard audio-frequency jack at the front panel.

Power supplies are normally obtained from a Stabilised Power-supply Unit Type SPS/3. The connections on the generator are made by an eight-pin plug situated at the rear of the unit.

Circuit Description

A circuit diagram of the complete unit is shown in Fig. 5. The unit includes a number of stages, the principles of operation which are described in Volume 3 of Television Engineering: Principles and Practice. The operation of such circuits will thus not be described here, and the interested reader is referred to the above textbook for details. Similarly, for a description of the television waveform, and the names of the various sections of the waveform, reference should be made to Volume 1

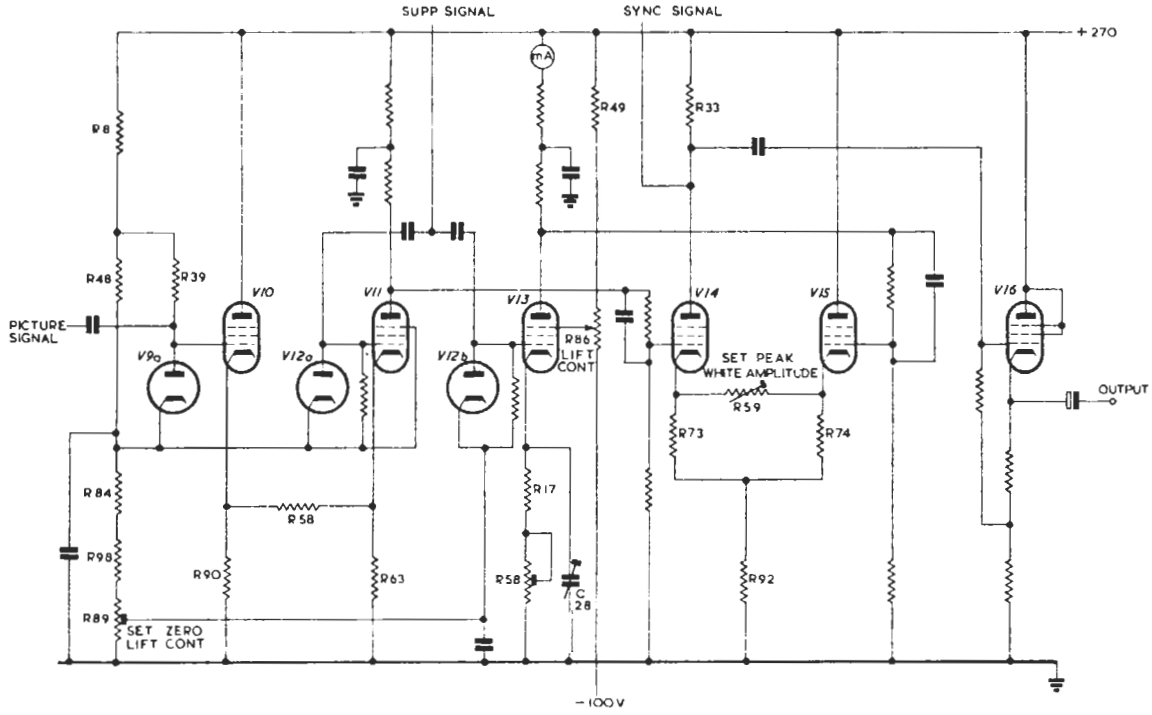


Fig. 2.1. Simplified Circuit Diagram of Mixing Stages and Output Stage

of *Television Engineering: Principles and Practice.*

For the purpose of description, the most convenient starting point of the circuit is the mixing section to which waveforms are applied to generate the complete signal. The waveforms employed will thus be referred to before the description of the means whereby they are generated.

Mixing and Output Stages

Fig. 2.1 shows a simplified circuit diagram of the mixing stages V9–V15, together with the output cathode-follower stage, V16. The latter is of conventional design, having an output impedance of 75 ohms approximately. It is fed from the anode of V14, which is connected in parallel with the anode of the sync-pulse generator output valve. This latter valve is cut off except in the intervals when sync pulses occur. The consequent change of current in the common anode load produces a sync-pulse output, the amplitude of which is independent of conditions in V14.

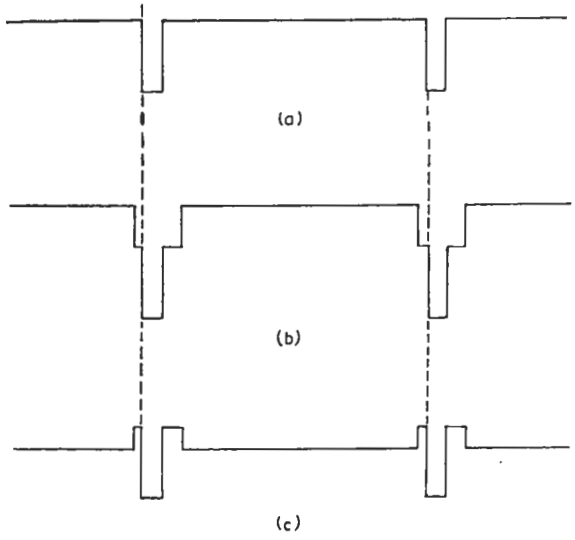


Fig. 2.2 Suppression Waveforms at the Anode of V14, showing (a) Zero Lift, (b) Positive Lift, (c) Negative Lift

The input to V14 comprises two signals; one at the grid from the anode of V11, and one at the cathode from V15, which is in turn fed from V13. We shall assume initially that the anode current in V11 is equal to that in V13. Thus, when suppression pulses are applied to the grids of V11 and V13 in parallel of sufficient amplitude to cut off current in both valves, equal positive-going pulses are generated at the anodes of V11 and V13 and fed to V14 and V15. Since these inputs are of the same polarity, each valve of this latter pair behaves as though its cathode load comprised its individual cathode resistor (R73 or R74) and a resistor equal to twice the value of the common load resistor R92. With this very large amount of negative feedback, the change in output voltage is scarcely perceptible. If the anode current in V11 exceeds that of V13, the condition of balance no longer exists, and the ' unbalance ' voltage, i.e. that by which the suppression-pulse voltage at the anode of V11 differs from that at V13, produces an output at the anode of V14 in the same way as if this ' unbalance ' voltage were applied alone to V14. By appropriate choice of electrode operating potentials, the suppression pulse in the output can be made positive-going, zero, or negative-going. Since it is usual to relate the remainder of the output waveform to the ' black ' level assumed to exist at the pre-sync and post-sync suppression periods, the effect is precisely similar to adding a variable d.c. component in the picture signal period, and is termed ' lift '. This is shown in Fig. 2.2.

Variation of the anode current of V13 is accomplished by means of the *Lift* control R86, which together with the series resistor R49 is connected between the 270-volt positive and the 100-volt negative supplies. The suppressor-grid bias of V13 can thus be varied between 0 and −100 volts with respect to earth. Anode current is cut off at a bias in the region of −60 volts, and thus the control enables the current of V13 to be varied between zero and maximum value. At the maximum value, it is usually desired that there should be zero lift in the output signal; the pre-set control R89 is normally set to achieve this. Because of the dissimilarity of the cathode circuits of V11 and V13, and the effect of the cathode follower V15 between V13 and V14, the suppression pulses applied to V14 tend to be dissimilar. In order to achieve the similarity necessary for cancellation, the variable components R85 and C28 in the cathode circuit of V13 are provided. Of necessity, R85 controls the anode current of V13, and hence the settings of R85 and R89 are interdependent. However, the former should only require adjustment at long intervals, or when a valve is changed. With correct adjustment, the amount of lift is proportional to the amount by which the anode current of V13 is below its maximum value, and the degree of lift is indicated directly by the meter in the anode circuit of V13. This meter has a right-hand electrical zero, i.e. it reads ' 0 ' when the anode

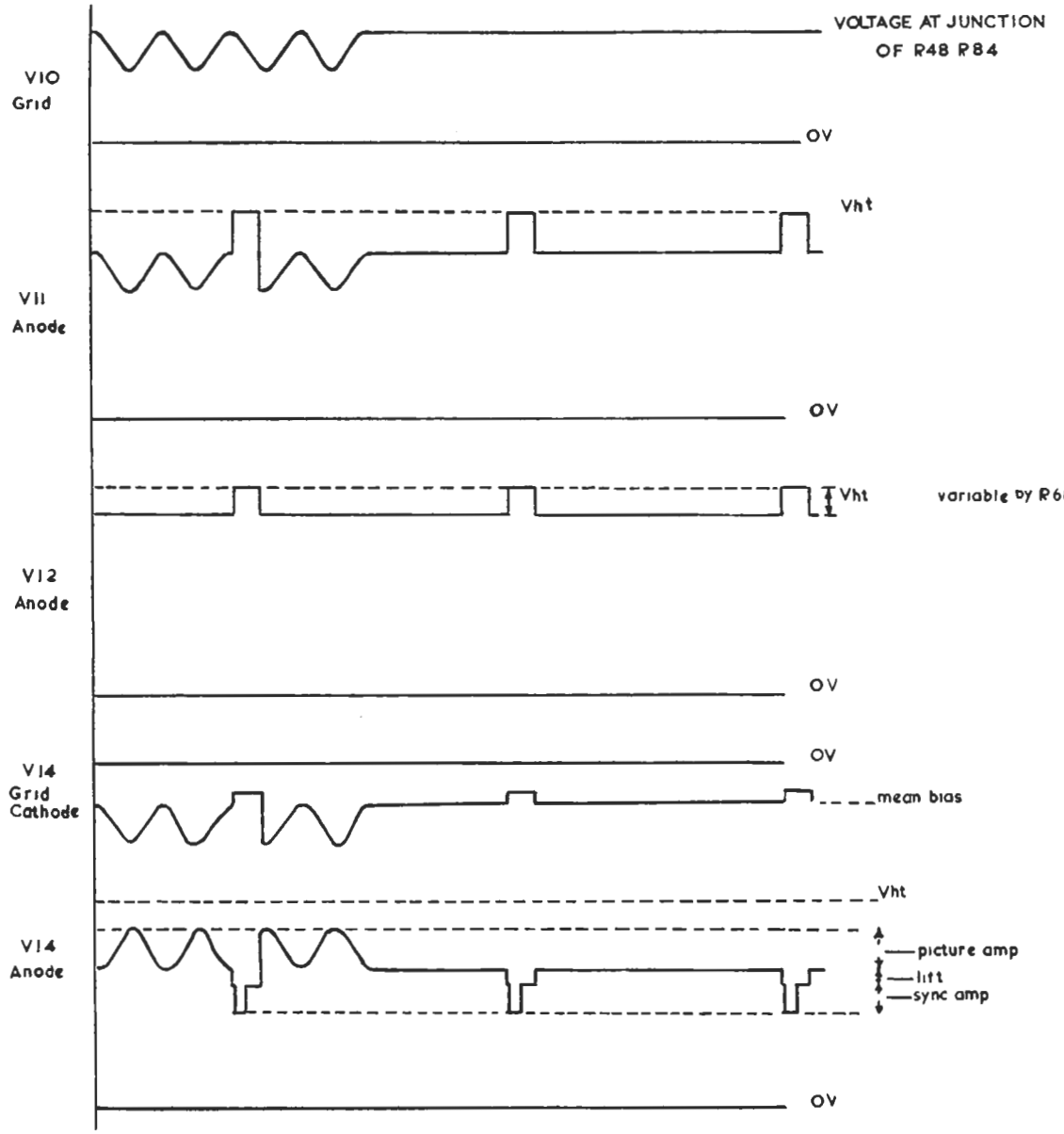


Fig. 2.3. Development of Signal Waveform in Mixing Stages

current is at maximum. The meter is scaled 0–100, its reading indicating the lift as a percentage of the peak-white value. A shunt-resistor chain R11, R12, enables the meter maximum deflection to be made to coincide with the scale zero.

When there is no standing current in V13, the lift is maximum and should correspond to peak-white signal amplitude, 0·7V. To enable this value to be set accurately, R59 is provided. This control varies within narrow limits the individual feedback applied to V14 and V15, and hence provides a fine control of the gain of the former. The control also varies the picture-signal amplitude, since this is transmitted via V10, as discussed later. The control does not, however, affect the sync-pulse amplitude, since these pulses are introduced subsequently, at the anode of V14.

is considered replaced by its equivalent T-network. The equivalent common cathode-load resistor effects the transfer of the picture signal to V11, and thence to the grid of V14. When a suppression pulse is applied to the grid of V11, this latter valve is cut-off; the picture signal is thus interrupted for the duration of the suppression pulse. The waveforms at successive stages in the chain V10–V16 are shown in Fig. 2.3; in this figure, the picture signal is assumed to comprise a sinusoidal waveform, followed by black level.

Master Oscillator and Automatic Frequency-Control Circuit

A master oscillator is employed to provide control of the line frequency and, by means of an automatic frequency-control circuit, can be syn-

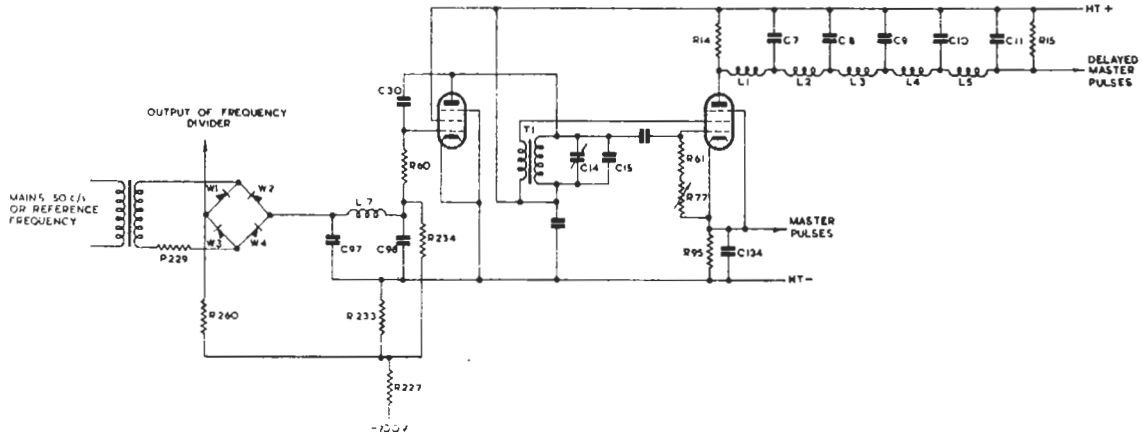


Fig. 2.4. Simplified Circuit Diagram of Master Oscillator and Reactance Valve

As stated above, the picture signal is fed via V11. In the arrangement employed the picture signal is fed to the grid of V10, and the positive-going excursions of the signal are clamped at the potential existing at the junction of R48 and R84 by the action of the diode V9(a). As it is desired that this clamping should be effective despitc changes of picture-signal amplitude, the recovery after a period of high picture-signal amplitude is assisted by returning the load resistor R39 to a point at a potential some 100 volts above that of V9(a) cathode.

The cathode of V10 is coupled to that of V11 by the π-section network R90, R58 and R69. This arrangement applies individual feedback to each valve, and a load common to both; this may perhaps be more easily visualised if the π-section

chronised with the mains-supply frequency, or an external signal source. The oscillator and a.f.c. circuit are shown in simplified form in Fig. 2.4.

The oscillator V2, is of the tuned-grid type employing the cathode, grid and screen-grid of V2 and operates at a frequency of 20,250 c/s. Outputs are taken at both anode and cathode. The current through the output loads is pulsed, as V2 operates in Class C, and two sets of short-duration pulses of opposite polarity are obtained. These pulses are designated *Master* pulses. The output at the anode is fed via an 0·5-microsecond delay network L1–L5, C9–C11. The pulse output across R15 is thus 0·5 microseconds delayed with respect to the pulse output across R95, and this delay is used to establish the correct time relationship between the line-suppression and line-synchronising pulses.

The width of the output pulses can be varied within narrow limits by R77, which alters the damping of the tuned circuit. As the damping is increased, the oscillator amplitude falls, and hence the width of the anode-current pulses increases. The width of these pulses determines the duration of the positive-going pulses at twice-line frequency occurring during the frame-sync signal. As the sum of the durations of a broad pulse and a twice-line-frequency pulse is constant, variation of the duration of the latter automatically alters the duration of the former, and hence R77 is designated *Set Broad Pulse Width.*

The variable-reactance valve V1 is connected in parallel with the oscillatory circuit comprising T1, C14 and C15. A small fraction of the voltage at the anode is fed back via C30 to the grid of V1, and since R60 is of low resistance, the voltage at the grid leads the voltage at the anode by almost 90 degrees. Consequently, the anode current in V1 leads the anode voltage by the same angle, and hence V1 behaves like a capacitor. The equivalent capacitance of V1 is directly proportional to the mutual conductance of the valve, and hence the frequency of oscillation can be altered by varying the mutual conductance of V1. The quiescent bias of V1 is derived from the potential divider R277, R233, connected across the 100-volt negative supply and is about 2·5 volts; to this is added a control voltage developed across C98. The value of the quiescent bias is such that V1 is operating in the region where substantial changes of mutual conductance occur with changes of bias, and hence the oscillator frequency varies in sympathy with the polarity and magnitude of the control voltage.

The control voltage is developed by the bridge phase-comparator circuit, W1–W4. To one pair of bridge terminals (the junction of W1, W2 and earth) is applied a pulse output from the frame-frequency divider chain; the pulse frequency is 50 c/s. To the other pair of bridge terminals is applied the reference-frequency signal, either at mains frequency or that of an external standard. Provided that the two signals are at the same frequency, there is no output from the comparator. If, however, the frequency of one changes, then the relative phasing of the two waveforms will alter, and an output will be developed. This output is smoothed and fed to the reactance valve, to alter the oscillator frequency tending to restore the previous phase relationship. If the change of frequency persists, there must of necessity be an output from the comparator to maintain the oscillator at its new frequency, and hence the previous phase relationship is not restored, but a new equilibrium relationship is established. Without the a.f.c. circuit, the phase difference would increase indefinitely.

Master Pulse ' Window ' Stage

The delayed master pulses from the anode of V2 are used directly to generate the pulses at twice-line frequency occurring in the frame-sync pulse. They are also used for triggering purposes, and for this reason the pulse shape is improved by the ' window ' stage V3 before being used for these applications.

The ' window ' stage comprises a cathode-coupled pair of triodes, V3(a) and V3(b). The input signal is applied to the grid of V3(a), whilst the grid of V3(b) is decoupled to earth. The signal at the grid of V3(a) is transmitted via the cathode load to V3(b) and hence the anode current in V3(b) tends to change in such a manner as to oppose the input cathode-voltage change. With a high-value cathode load, the anode-current changes are very nearly equal, the difference, flowing in the cathode load, supplying the input to V3(b). Since this input must be substantially equal to the grid-cathode voltage, V3(a) has the equivalent of 6 db of negative feedback.

With a small-amplitude input signal, this type of stage behaves as a phase-splitter, giving a push-pull output at its anodes. If, however, V3(a) is driven sufficiently positive that anode current in V3(b) is cut-off, then the current-compensating action of V3(b) ceases and the degree of feedback applied to V3(a) rises abruptly, limiting the output sharply. Conversely, if V3(a) is driven to cut-off there can be no further change of current in either valve. Thus, limiting occurs on both peaks of a symmetrical input.

The input to V3(a) comprises negative-going pulses of short duration (10 microseconds approximately). These pulses are of sufficient amplitude (about 40 volts), to cut off V3(a), and hence the output pulses at the anodes of V3(a) and V3(b) tend to be flat-topped with short rise times.

The output from V3(a) is used to trigger the sync generator, the frame-suppression generator and the picture-signal ' spike ' generator. The output from V3(a) is fed to the frame-frequency divider chain, and provides the reference pulses for the frame-suppression and frame-sync generators.

Frame-frequency Divider

The frame-frequency divider comprises stages V17–V26. These together form five similar division stages, dividing by 3, 3, 3, 3 and 5 respectively, a total division ratio of 405. The final outputs, which comprise one set of positive-going and one set of negative-going pulses, have a frequency of 50 c/s, and durations of some 18 milliseconds.

Each divider stage is of the cathode-coupled phantastron type described in *Television Engineering:* Volume 3. Each one is actually a pulse generator, the circuit being such that the generator is triggered by every third input pulse (or fifth in the case of the final divider). The operation of the first divider stage is described briefly below; the operation of the others is similar.

Under quiescent conditions, with no input signal applied, valve V22 is conducting, with its grid held at the potential of the junction of R162 and R178 by the action of the diode V17(b). Current flows through the diode from the h.t. supply via R106. The cathode of V22 is at a potential somewhat higher than its grid, and the suppressor grid is at the potential of the junction R178, R198. The suppressor-grid/cathode bias is then sufficient to cut off anode current in the valve, so that the total cathode current flows to the screen grid.

When a negative-going pulse is applied to the anode of V22 via the diode V17(a), the grid potential is carried negative since C58 cannot discharge immediately. Diode V17(b) ceases to conduct, and the cathode potential is driven negatively by cathode-follower action. If the pulse amplitude is sufficient, the suppressor-grid/cathode bias falls to a value where anode current starts to flow. The anode potential then tends to fall still further. A rapid fall of anode and control-grid potentials is thus initiated, which ceases when current is nearly cut off by the bias at the control grid. When this happens, the anode potential then commences a linear run-down whilst the control-grid potential slowly rises; the run-down rate is controlled by the magnitudes of R131, C58 and R106. When the anode voltage falls to the value at the knee of the i_a–V_a characteristic, the anode potential tends to fall more slowly and the grid potential commences to rise more rapidly. The cathode potential rises similarly, and the suppressor-grid/cathode bias increases, reducing the proportion of the total current in the valve flowing to the anode. This action slows down still further the rate of fall of anode potential, and after a short interval, the anode potential commences to rise. The control-grid potential is then driven positively by the action of C58, and the process is cumulative, the circuit returning rapidly to the quiescent condition.

The outputs available are (a) sawtooths at the anode (b) negative-going pulses at grid and cathode and (c) positive-going pulses at the screen grid.

In the quiescent condition, the anode and cathode of V17(a) are at the same voltage, and when a triggering pulse is applied, the action described above is initiated. When subsequent trigger pulses are applied, whilst the anode potential run-down is occurring, these pulses will not be transmitted since their amplitude is less than the anode-cathode voltage of V17(a). Thus after the application of the initial pulse, the circuit is insensitive to following pulses until it has returned to its quiescent state. If then the run-down period exceeds that of two complete pulse-repetition periods, the stage will respond only to every third pulse, i.e. the output pulse-repetition frequency is one third of that of the input. The output from the cathode, being negative-going, can be used to trigger a similar stage following.

The later divider stages are similar to V22, and differ only in that the run-down times are proportionately increased as the pulse input repetition frequency progressively decreases.

The output from the screen grid of the final divider, V28, is fed to the phase-comparator circuit and to the picture-signal generator; it is used in the latter as one of the picture signals, providing a frame bar. Its duration is some 18 milliseconds and its start is coincident with the start of a frame; the duration of the frame bar thus generated is thus between 80 and 90 per cent of the frame period.

The output from the cathode of V26 is used to trigger the frame-keying and frame-suppression generators.

Sync-pulse Generator

The generation of the complete sync signal is accomplished by mixing the appropriate individual sections of the sync signal in valve V8. This stage is followed by a 'window' stage (V32, V33) to improve the waveform. The circuit is shown in simplified form in Fig. 2.5. As explained previously sync pulses are produced in the output by current taken through R33 by V33. R33 is the common load resistor of V33 and V14. V33 is normally cut off; its grid is returned to the junction of R177,

R197 which is about 3·5 volts negative with respect to the junction of R177, R174 to which the grid resistor of V32 is returned. The complete sync signal is applied negative-going to the grid of V32, and is of sufficient amplitude to cut off V32 during sync pulses. During such periods, therefore, V33 conducts. The magnitude of the anode current, and hence the magnitude of the output pulses, is determined by R196 (*Set Sync Amplitude*) which controls the total cathode resistance of V33. The lower this resistance, the greater is the magnitude of the anode current pulses in V33.

The mixing stage V8 comprises a double triode, with a common cathode load resistor R67. The grid resistor of V8(a) is returned to earth, whilst

The input to the grid of V8(a) comprises a mixture of two sets of pulses. The first, at line frequency, is of 10·5-microseconds duration. The leading edges of these pulses are synchronised with the trailing edges of the undelayed master pulses. Hence the first 0·5 microsecond of each such pulse is suppressed by the action of the pulses at the grid of V8(b), as shown in Fig. 2.6. The resultant 10-microsecond pulse is the line-sync pulse; the reference time for the leading edge of the line-sync pulses is thus that of the trailing edge of the delayed master pulses. The other waveform at the input of V8(a) is the frame-keying waveform. This is a pulse of duration equal to four complete line periods. The timing of the leading and trailing

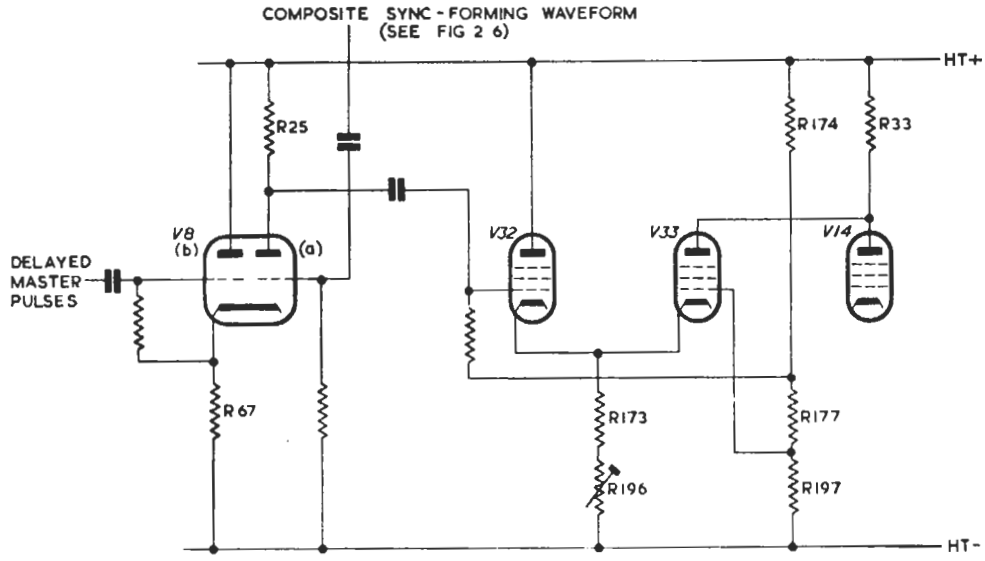


Fig. 2.5. Simplified Circuit Diagram of Sync-pulse Generator Stages

that of V8(b) is returned to cathode. The input to V8(a) comprises a composite waveform providing the basis of the line- and frame-sync pulses; these pulses are positive-going. The input to V8(b) comprises positive-going master pulses derived from the oscillator V2, with 0·5-microsecond delay; grid-current biassing occurs, and the amplitude of the pulses is such that V8(b) does not conduct between pulses. In the intermediate periods, V8(a) has a small anode current sufficient to maintain its bias near the cut-off value. At the occurrence of each of the master pulses, V8(b) conducts and the common cathode potential rises to a value where V8(a) is cut-off irrespective of the magnitude of the signal at its grid.

edges is synchronised by the leading edges of the delayed master pulses. The 10·5-microsecond pulses at line frequency are suppressed for the period of this waveform. The resultant output at the anode of V8(a) is derived as shown in Fig. 2.6, which shows the conditions at the ends of both odd and even frames. The lines and master pulses have been arbitrarily numbered to assist the understanding of the waveform generation. The 0·5-microsecond delay between the two sets of master pulses has been exaggerated in the figure for greater clarity.

10·5-microsecond Pulse Generator

The composite signal fed to the grid of valve V8(a), described above and shown in Fig. 2.6,

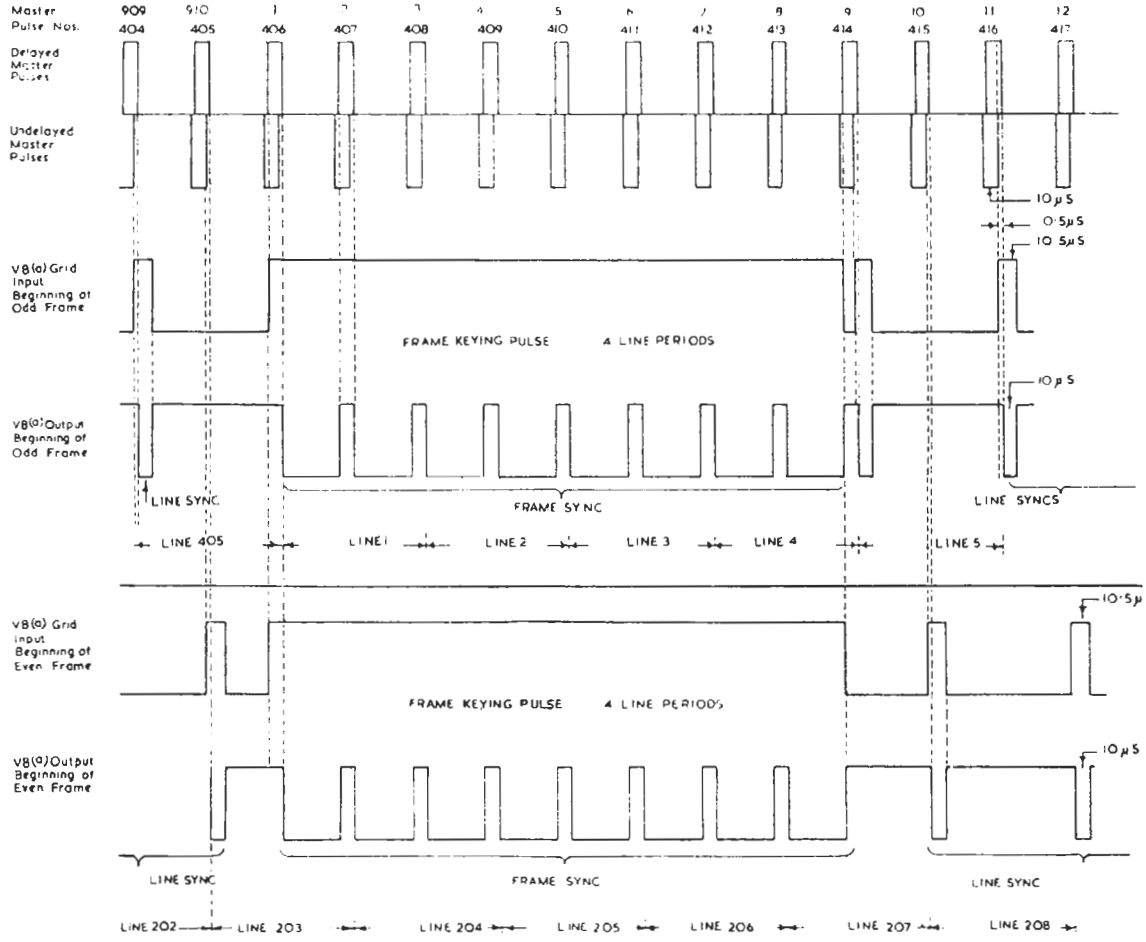


Fig. 2.6. Development of Sync-pulse Waveform

is generated in the stage comprising V6 and V7. These two valves are connected as a monostable cathode-coupled multivibrator, shown in simplified form in Fig. 2.7. With no input to the control grid or suppressor grid of V6, current flows in V6. V7 is cut-off, since its grid is at a potential substantially lower than that of V6, and the cathode load (R65) is common to both valves.

When a negative-going pulse of large amplitude is applied to the suppressor grid of V6, anode current is cut off, and the anode potential rises to that of the h.t. supply. The positive-going pulse

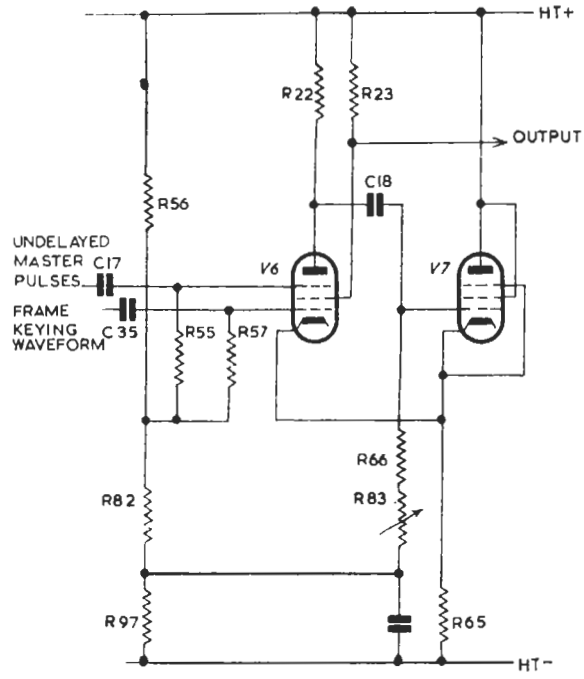


Fig. 2.7. Simplified Circuit Diagram of 10.5-microsecond Pulse Generator

at the grid of V7 is then sufficient to drive V7 to zero bias, which in turn causes the cathode potential to rise. This rise in cathode potential is sufficient to cut off current in V6. The circuit then remains in this state until C18 has charged sufficiently for the current in V7 to fall; when this happens, current re-commences in V6, accentuating the rate of transition to the initial state. There is thus a positive-going short-duration pulse developed at the anode and screen of V6; the latter pulse is that fed to V8(a). The duration of the pulse can be set accurately to 10·5 microseconds by means of R83. The duration of the pulse is 0·5 microseconds longer than that of a line-sync pulse, and hence R83 is designated *Set Line Sync Width*.

The input pulses to the suppressor grid of V6 are differentiated by the short time-constant network comprising C17, R55. This arrangement ensures that the input pulse controls only the timing of the leading edge of the 10·5-microsecond pulse, and not the duration; the leading edge is co-incident with the trailing edge of alternate undelayed master pulses.

The input to the control grid of V6 comprises the frame-keying waveform. This waveform is negative-going, and comprises a pulse of some 400 microseconds duration (4 line periods). Its magnitude is sufficient to cut-off current in V6,

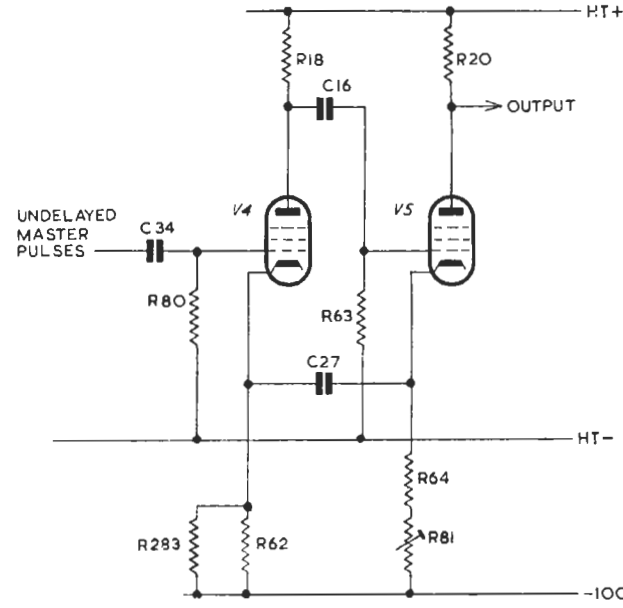


Fig. 2.8. Simplified Circuit Diagram of Line Divider and Suppression Generator Stages

and hence the 10·5-microsecond pulses are not generated during the period of the frame-keying waveform. The leading and trailing edges of this waveform are co-incident with the leading edges of delayed master pulses.

Line Divider and Suppression Generator

The input signal to the 10·5-microsecond pulse generator, and the line suppression pulses are generated in the stage comprising V4, V5. The valves are arranged in an astable cathode-coupled multivibrator circuit, shown in simplified form in Fig. 2.8.

The multivibrator has a mark/space ratio of some 4 : 1. In the free running condition, this ratio is determined by the magnitudes of the cathode-load resistors, each cathode resistor determining the period during which its associated valve is cut-off. The natural period of the multivibrator is somewhat greater than one line; under driven conditions, it is triggered by the leading edges of alternate master pulses. These pulses are positive-going, and are the undelayed pulses derived from the cathode of V2. The pulses are differentiated by the short time-constant combination C34, R80 at the grid of V5, and the positive 'spike' at the leading edge of each alternate pulse drives V5 into conduction. After a short interval, V5 is again cut-off; the cathode bias carries the valve substantially beyond cut-off, so that the amplitude of the next positive 'spike' at the grid is insufficient to cause current to flow in V5. The output-pulse frequency is thus half that of the input.

The duration of the conduction period of V5 can be altered by means of R81; since the pulse developed in this period is the line-suppression pulse, R81 is designated *Set Line Suppn. Width.*

The output employed is taken from the anode of V6; the line-suppression pulse is here negative-going as required to drive the suppressor grid of V6. An output from the screen of V5 is taken to the suppression mixer stage V29, and to the picture-signal pulse generator.

Frame-keying Pulse Generator

The frame-keying waveform fed to the 10·5-microsecond pulse generator is generated in the frame-keying pulse generator stage, V27. A simplified circuit of this stage is shown in Fig. 2.9. V27 is a monostable cathode-coupled multivibrator. The grid of V27(a) is returned to a point of positive potential (+10 volts approximately), whilst the grid of V27(b) is returned to earth. The common cathode-load resistor is returned to the negative 100-volt supply, and hence in the stable condition, V27(a) is conducting whilst V27(b) is cut off.

The output from the final stage of the frame-frequency divider V26 is fed to the grid of V27 via the short time-constant network C77, R169. The output from the cathode of V26 comprises a negative-going pulse of approximately 18 milliseconds duration. These pulses occur at frame frequency, and the leading edge of the pulse is coincident with the leading edge of a delayed master pulse. This leading edge provides a negative-going 'spike' at the grid of V27(a), which cuts off anode current in V27(a). The anode potential consequently rises, and V27(b) is driven into conduction by the positive pulse at its grid (see Fig. 2.10). The cathode potential rises, and maintains V27(a) in the non-conducting state. V27(b) remains conducting until C66 charges to sufficiently for the cathode potential to fall the point where V27(a) recommences to conduct.

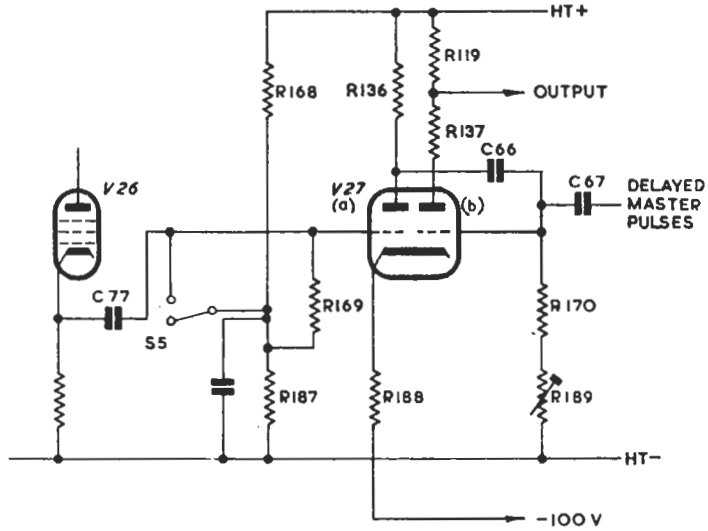


Fig. 2.9. Simplified Circuit Diagram of the Frame Keying-pulse Generator

There is then a rapid transition to the initial state.

Delayed master pulses are fed to the grid of V27(b) via the short time-constant network C67, R170, R189. The ' spikes ' appearing at the grid of V27(b) are of small amplitude, and do not appreciably affect the operation of the circuit except when a negative-going ' spike ' occurs when V27(a) is about to commence conduction. The occurrence of such a ' spike ' at this time initiates a transition to this conducting state. The negative-going spikes at the grid of V27(b) are coincident with the leading edges of the delayed master pulses, and hence the duration of the pulse at the anode of V27(b) is an integral multiple of the master pulse-repetition period. A control of this number is provided by R189, which varies the period continuously over a limited range when the ' spikes ' are not applied. Since the frame-keying waveform duration determines the number of broad pulses in the frame-sync signal, R189 is designated *Set No. of Broad Pulses*.

For the purposes of certain tests, it is desirable to have no frame signals in the output waveform. The removal of the frame-sync signal is accomplished by throwing the switch S5 from *Complete W/F* to *Line W/F*. When this is done, the grid of V27(a) is connected to a point at a.c. earth potential, and hence the stage cannot be triggered.

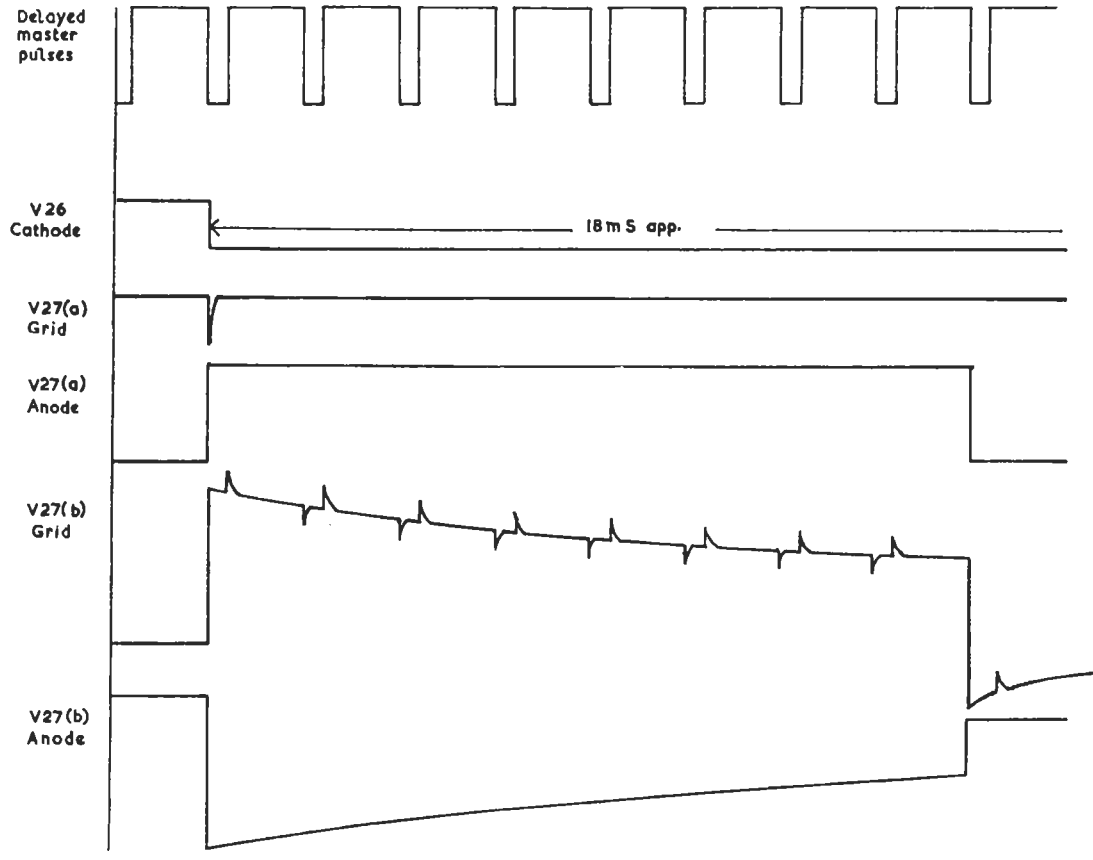


Fig. 2.10. Development of Frame-keying Waveform

Suppression-pulse Generator

The generator of the line-suppression pulse is achieved in the stage comprising V4 and V5, which also functions as a line-frequency divider. These pulses are mixed with the frame-suppression pulses to form the composite suppression signal. The generator of the frame-suppression pulse is described below.

Frame-Suppression Pulse Generator

The frame-suppression pulse is generated in the stage V28. This stage is almost identical with that of the frame-keying-pulse generator described earlier. The timing resistors R171, R191 are, however, somewhat larger, because of the greater duration of the frame-suppression pulse. Unlike the frame-keying-pulse generator, the end of the pulse is determined by the timing of the *trailing* edge of a delayed master pulse, obtained from the anode of V3(a) to have the correct polarity for this purpose. Adjustment of R191 (*Set Frame Suppression Width*) alters the pulse duration in discrete steps; the normal duration is 14 lines *plus* the duration of one master pulse, since the leading and trailing edges of the suppression pulse are timed by the leading and trailing edges, respectively, of master pulses.

Suppression-Pulse Mixer and Limiter

The line- and frame-suppression pulses are mixed to form a composite signal in valve V29, and this signal is then passed through the limiter stage V30.

The mixer stage comprises the pentode V29, which has a suppressor grid requiring a relatively small input to cut off anode current. To this suppressor grid is applied the negative-going frame-suppression pulses from the anode of V27(b). To the suppressor grid is connected the anode of an internal diode of V29, and, by the action of this diode, the positive peaks of the signal are clamped at cathode potential. The suppressor pulses are of sufficient amplitude to cut off anode current in V29.

The line-suppression pulses from V5 are fed to the control grid of V29 and grid-current biassing is used. When a line-suppression pulse occurs, anode current is cut off, and hence the pulses are trans-

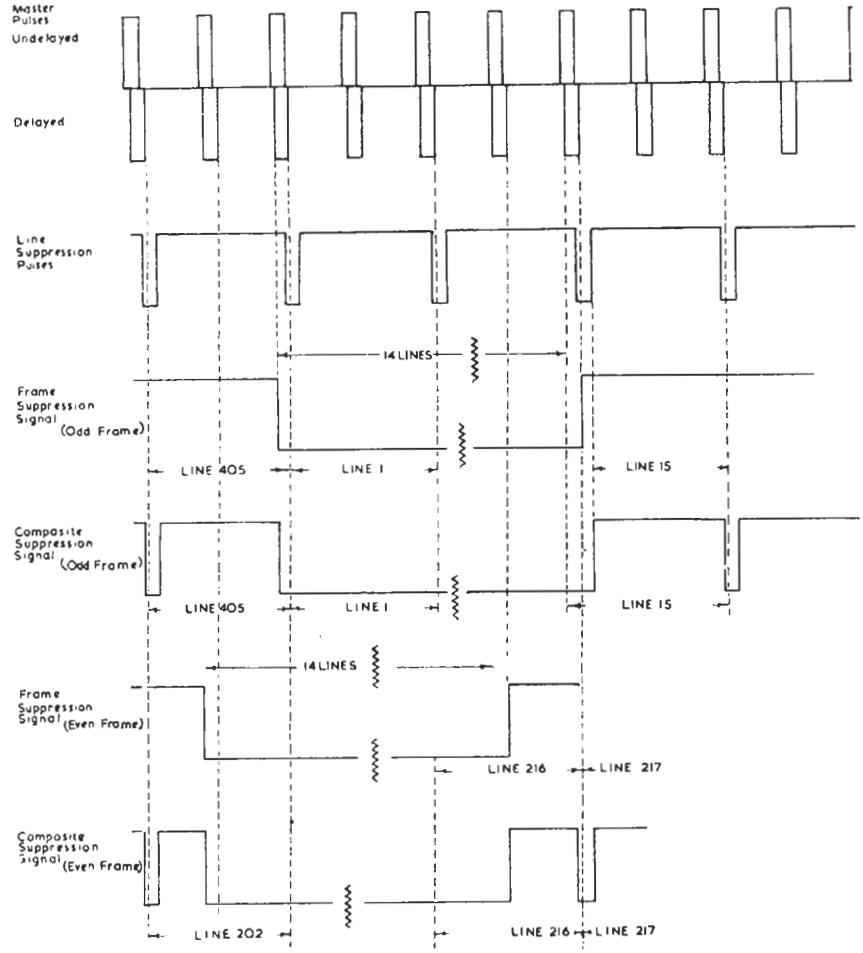


Fig. 2.11. Development of Composite Suppression Signal

mitted positive-going to the output. The composite suppression waveform is shown in Fig. 2.11.

V30 is the suppression-pulse limiter stage. The valve is grid-current biassed, and the input suppression signals from the anode of V29 are positive-going. These input pulses are of sufficient amplitude to drive the grid of V30 to a value well beyond cut-off in the intervals between pulses. The output pulses at the anode are consequently 'cleaned'. From the anode of V30, the suppression pulses are fed to the grid of V11 and V13 in parallel, as described earlier.

Picture Signal Generation

The picture signal may belong to one of four main categories. These are (a) Lift, (b) External, (c) Sawtooth and (d) Pulse signal. The picture category is selected by means of switch S1. Wafer S1(a) selects the input to V10 of the mixing stages. Wafer S1(b) serves to switch the h.t. supply to the appropriate picture-generating section. The picture-generating stages can thus be discussed individually.

The first category of picture, comprising lift only, can be dealt with immediately. At this position of the selector switch (designated *Sync and Lift*), there is no signal fed to V10; the picture-signal lift is generated in V13 as described previously. It is of interest to note that the coupling capacitor C33 to the grid of V10 is connected to the resistor R176, which is returned to the h.t. line. A similar arrangement is adopted at all positions of the switch, to ensure that large surge voltages are not fed to V10 when switching occurs.

External Signal Amplifier

Provision is made for the application of a picture signal from an external source. The amplitude of the input signal is metered, and the amplitude of the picture signal can be varied in discrete steps.

The external signal is fed to one of two co-axial plugs at the front panel. A 75-ohm resistive termination is provided by R245. The signal is then amplified in the two-stage shunt-inductance amplifier comprising V34 and V35. From the anode of V35 the signal is fed to the cathode follower V36. The cathode load of this stage comprises ten equal resistors, the junctions of which are connected to the contacts of the switch S3 (*Ext. Signal Level*). The switch positions are designated 0, 10, 20 etc. up to 100, corresponding to the percentage of the total output selected. By this arrangement the picture amplitude can be varied in 10 per cent steps from zero to peak white.

A peak-reading diode-voltmeter V9(b) is connected in parallel with the resistor chain. The overall gain of the stages V34 and V35 is 25 db, whilst the cathode follower introduces a loss of 3 db. With this overall gain of 22 db from input to voltmeter, the voltmeter reads mid-scale for an input signal of approximately 0·7 volt d.a.p.

Sawtooth Generator

A sawtooth at line frequency is generated by V31. This stage comprises a free-running Miller-transitron circuit, of the conventional type described in detail in *Television Engineering:* Volume 3. The generator is synchronised by 'spikes' at its suppressor grid, derived from the leading and trailing edges of the line-suppression pulses at the screen grid of V5. These pulses are negative-going, and the effect of the short time-constant network at the suppressor grid of V31 is to produce a negative-going 'spike' co-incident with the leading edge of the suppression pulse, and a positive-going 'spike' co-incident with the trailing edge of the suppression pulse. The first of these 'spikes' cuts off anode current in V31, and hence initiates the flyback period. The second initiates anode current flow in V31 before it would otherwise occur, and hence the beginning and end of each sawtooth is co-incident with that of the line during which it is displayed.

The sawtooth has the initial 'step' occurring with this type of generator, as shown in Fig. 7 (V31 anode). This step is equivalent to the addition of 'lift' to the picture and the *Set Zero Lift* control must be adjusted to eliminate this spurious lift component when the sawtooth waveform is employed. A pre-set control of the peak sawtooth output is provided by R128, *Set Sawtooth Amplitude.*

Picture Pulse Generator

The pulse generator comprises a cathode-coupled multivibrator, together with a 'window' stage; the latter also functions as a mixer stage for the production of one of the pulse waveforms. The pulse signals are selected by means of switch S2 (*Pulse Signal*), and comprise

Frame 1: Pulses having a natural repetition frequency somewhat less than twice frame frequency. The leading edges of alternate pulses are synchronised with the trailing edges of frame-suppression pulses.

Frame 2: Pulses with a mark/space ratio of approximately unity and a repetition period equal to that of 4½ lines.

Line 1: Pulses with a mark/space ratio of approximately unity and a repetition period of about one-third of that of one line.

Line 2: Pulses with a mark/space ratio of unity and a repetition period equal to one twenty-fifth of a line.

Spike 1: Pulses of approximately 2 microseconds duration occurring at the middle of each line.

V38 and V39 share a common load resistor R26; in this position, the circuit behaves as a free-running multivibrator, of unity mark/space ratio, the periods of conduction being determined by the magnitude of C93, R125 and R226. The natural repetition period is about 12 milliseconds. The multivibrator is synchronised by the application of frame-suppression pulses from V28. These pulses are negative-going and are differentiated by the short time-constant network C217, R213 at the grid of V38. The resultant positive-going ' spike ' at the end of the frame-suppression period initiates anode current in V38, and hence cuts-off anode

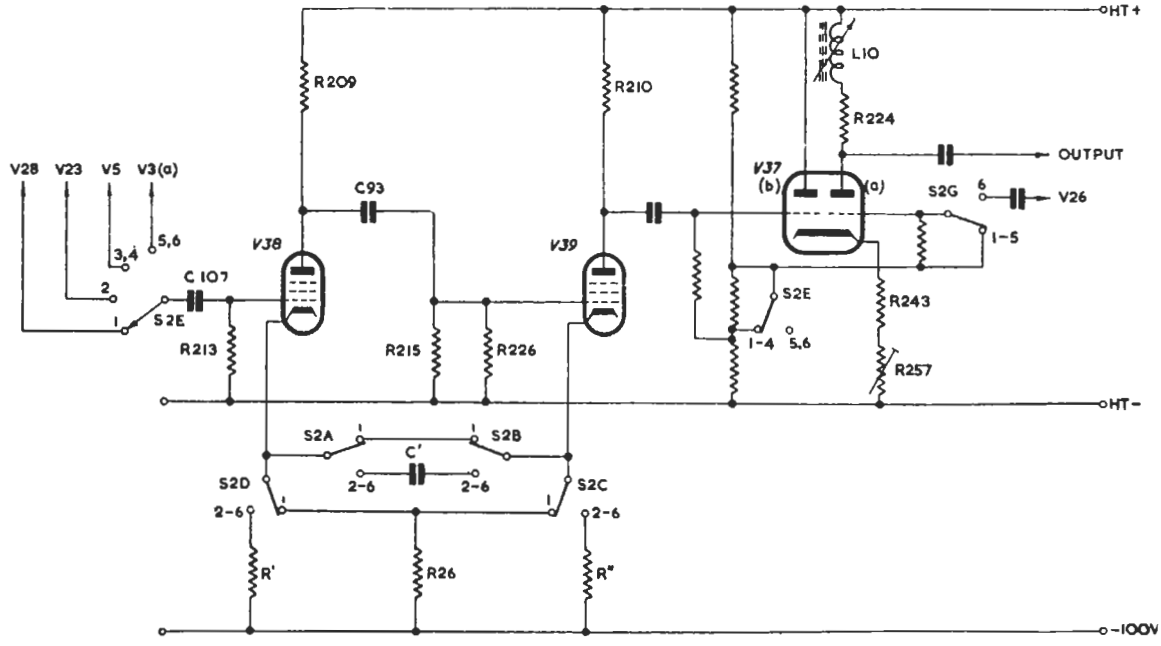


Fig. 2.12. Simplified Circuit Diagram of Picture Pulse Generator and ' Window ' Stage

Spike 2: Pulses of approximately 20 microseconds duration, occurring at the middle of each line, together with a pulse of some 2 microseconds at the beginning of each line. The picture signal is removed for a period of some 2 milliseconds prior to the end of each frame period.

A simplified circuit diagram of the pulse generator and ' window ' stage is shown in Fig. 2.12. In this figure certain contacts of switch S2 have been grouped and shown as one contact to clarify the circuit drawing.

When switch S2 is set to *Frame* 1 (position 1), current in V39. Thus at the anode of V39, alternate positive-going leading edges of the output pulses are co-incident with the start of the frame-suppression period. The resultant waveform thus has alternate pulses of unequal durations. The display on a picture monitor comprises a white bar near the centre of the frame, occupying somewhat more than a quarter of the frame period, and a smaller white bar at the foot of the frame.

In the *Frame* 2 position of S2, the multivibrator is transformed to the cathode-coupled type by the introduction of capacitor C105 (C′ of Fig. 2.12). The network C93, R125, R225 now acts merely as a coupling network, and the period of the relaxation

oscillation is determined by C110, R261 and R264 (C′, R′ and R″ respectively of Fig. 2.12). Since R261 and R264 are equal, the oscillation has a unity mark/space ratio. The natural oscillation period is some 500 microseconds; the oscillator is, however, synchronised by the application of pulses to the grid of V38 from V23. These latter pulses are positive-going, and are repeated at intervals of one-ninth of the master-oscillator frequency, i.e. at $4\frac{1}{2}$ line intervals. The network C107, R213 has a short time-constant, and hence differentiates the input pulses from V23 to produce positive-going and negative-going 'spikes' at the grid of V38. The positive 'spike' which is co-incident with the trailing edge of the pulse from V23, initiates anode current in V38, and thereby provides the synchronising action.

In the *Line* 1 position of S2, conditions in V38 and V39 are generally similar to those described above, except that the natural repetition frequency is increased by the employment of a smaller timing capacitor, C110. The natural period is some 34 microseconds. Synchronisation is achieved by the application of line-suppression pulses from the screen grid of V5. The positive-going 'spike' generated by C107, R213 at the beginning of each suppression pulse initiates anode current in V38, and provides the synchronising action. Viewed on a picture monitor, the signal comprises two vertical white bars.

In the *Line* 2 position of S2, the free-running period is still further reduced to some four microseconds. Synchronisation is effected by line-suppression pulses; as however, the circuit is triggered only at every twenty-fifth pulse, its free-running frequency must be closely adjusted. For this reason, a trimmer capacitor, C111, *Line 2 Pulse Lock*, is provided.

In the *Spike* 1 position of S2, the cathode resistors R263 of V38 and R259 of V39 are unequal. Consequently, the multivibrator free-running mark/space ratio is no longer unity, but about 25. The mark period is two microseconds; this is the 'spike' which gives the waveform its title. The spikes are initiated by synchronising pulses from V3(a); these are positive-going pulses at twice line frequency (delayed master pulses). The trailing edges of these pulses produce negative-going spikes at the grid of V38, and these serve to end the conduction period of V38. This is followed by the short conduction period of V39 and the reversion to the state when V38 conducts. Although the generator is triggered at twice line frequency, only the 'spike' occurring at the middle of the line period can be displayed, since the other occurs during the line-suppression period.

In the *Spike* 2 position of S2, unequal cathode resistors of V38 and V39 are again employed, and the mark/space ratio is about 3 : 2. The mark period is some 20 microseconds, and the end of the space period is determined by the negative-going spikes co-incident with the end of the delayed master pulses, as described for the 'Spike 1' waveform. The 'Spike 2' waveform repetition frequency is thus also twice that of line frequency. Because of its relatively long duration, the pulse commencing during the line-suppression period overlaps the beginning of each line picture period, and there is a small portion of the 'mark' pulse in the picture signal. This 'spike' represents the portion of the 'mark' pulse which extends beyond the line-suppression pulse. The duration of this latter pulse is some 18 microseconds, and hence, with a 'mark' period of 20 microseconds, this pulse at the commencement of each line is of some 2 microseconds duration. The pulse at the middle of the line is, of course, that of the full 'mark' period.

This picture signal is suppressed for a period near the end of each frame; this 'blanking' is accomplished in the 'window' stage discussed below.

Picture-pulse Window Stage

The picture-pulse 'window' stage V37, is similar to stages of this type discussed earlier. Control of the output pulse amplitude is provided by R257, *Set Pulse Picture Amp.*, which controls the quiescent currents in the two halves of V37(a). Shunt inductance is employed in the anode of V37(a) to preserve the high-frequency response.

With the pulse signals having approximately unity mark/space ratio, the two halves of V37 have equal d.c. voltages applied to the grids. With the asymmetrical 'spike' waveforms, the bias conditions are unbalanced by the switch wafer S2F by the introduction of additional bias at V37(a) by R251. Under quiescent addition, V37(a) is biassed nearly to cut-off, so that V37(b) anode current is high. The negative-going 'spike' waveforms from the anode of V39 are of sufficient amplitude to cut-off anode current in V37(b), and hence drive V37(a) anode current to a high value. The provision of asymmetrical bias enables a larger double-amplitude peak output to be obtained with the asymmetrical input waveform In the

absence of this biassing arrangement, the double-amplitude peak output would be only about half of that obtainable with the symmetrical waveforms.

In the 'Spike 2' position of S2, a frame-blanking waveform is introduced at the grid of V37(a). This waveform is negative-going and comprises a pulse of some 2 milliseconds duration, the trailing edge of which provides the synchronising edge initiating the frame-suppression period. Thus, during the period of this pulse, anode current in V37(a) is cut-off, and there is no picture output. When displayed on a picture monitor, the effect is to remove the 'Spike 2' waveform from the last period of the frame.

Mechanical Construction

The mechanical construction can be seen in Plates V and VI. The unit is mounted on a 19-in. × 24-$\frac{15}{32}$in. panel. suitable for bay mounting. Behind the front panel, and at a distance of 5 inches from it, is a sub-panel. On this sub-panel are mounted the valves and associated components. At the rear of the unit, at a distance of 9 inches from the front panel, are two vertical panels each $2\frac{1}{2}$ inches wide, supporting components and the pre-set controls. The whole is enclosed by a cover, which is detached from the rear; when in place spring clips press against the inside of the cover, to retain it in position, and ensure that it is earthed. The cover is cut out at the rear to give access to the power-supply plug.

Access to the valves from the front of the unit is through a detachable plate secured to the front panel. The plate is fitted with handles, and is held in place by the pressure of spring mountings on four fasteners at the top and bottom centre of the plate, and at the mid points of the sides. Additionally, handles are attached to the front panel to assist removal and replacement of the unit.

Power Supplies

Power supplies are normally obtained from a Stabilised Power-Supply Unit, Type SPS/3, which is described in Technical Instruction V4, Section D. Connections to the power-supply unit are by means of an eight-way plug at the rear of the unit. Connections to the plug are as follows:

Tag No.	
1	HT— and EARTH
2	+270V
3	−100V
4	—
5, 6	6·3V: tag 6 earthed
7, 8	6·3V: tag 8 earthed

Valve Data

All readings measured with AVO Model 7 or 40, with the exception of the readings indicated by *; these latter readings measured with a high-impedance waveform monitor or valve voltmeter.

Tolerance on all readings ±10 per cent.

Valve	*Anode Volts*	*Screen Volts*	*Suppressor-grid Volts*	*Control-grid Volts*	*Cathode Volts*	*Remarks*
V1 EF50	208	210	—	−2·5	—	No a.f.c. voltage
V2 EF50	—	210	—	—	—	
V3 (a)	—	—	—	—	—	
ECC91 (b)	—	—	—	—	—	
V4 EF50	240	243	—	—	2·3	

Valve	*Anode Volts*	*Screen Volts*	*Suppressor-grid Volts*	*Control-grid Volts*	*Cathode Volts*	*Remarks*
V5 EF50	252	260	—	—	16·2	
V6 EF50	215	235	—	—	61	
V7 EF50	254	254	—	—	61	
V8 (a)	275	—	—	—	26	
ECC91 (b)	125	—	—	—	26	
V9 (a)	—	—	—	—	40	
EB91 (b)	—	—	—	—	—	
V10 EF50	259	261	—		62	
V11 EF50	263	261	—	—	62	
V12 (a)	—	—	—	—	40	
EB91 (b)	—	—	—	—	0–9	
V13 EF50	263	261		—	7·5	
V14 EF50	132	264	—	—	58	
V15 EF50	262	223	—	—	60	
V16 EF55	274	274	274	—	14	
V17 (a)	—	—	—	—	90	No input
EB91 (b)	—	—	—	—	16	
V18 (a)	—	—	—	—	90	No input
EB91 (b)	—	—	—	—	16	,,
V19 (a)	—	—	—	—	90	,,
EB91 (b)	—	—	—	—	16	,,
V20 (a)	—	—	—	—	90	No input
EB91 (b)	—	—	—	—	16	,,

Valve	*Anode Volts*	*Screen Volts*	*Suppressor-grid Volts*	*Control-grid Volts*	*Cathode Volts*	*Remarks*
V21 (a)	—	—	—	—	90	No input
EB91 (b)	—	—	—	—	16	,,
V22 6F33	130*	150*	9	—	22	,,
V23 6F33	130*	150*	9	—	22	,,
V24 6F33	130*	150*	9	—	22	,,
V25 6F33	130*	150*	9	—	22	,,
V26 6F33	130*	185*	9	—	22	,,
V27 (a)	122*	—	—	—	18	
ECC91 (b)	190*	—	—	—	18	
V28 (a)	130*	—	—	—	17	
ECC91 (b)	200*	—	—	—	17	
V29 6F33	90	100	—	—	—	
V30 EF50	200	210	—	—	—	
V31 EF50	122	140	—	—	—	
V32 EF50	250*	180*	—	—	30	
V33 EF50	210	180*	—	—	30	
V34 EF50	180	265	—	—	2	
V35 EF50	170	265	—	—	2·1	
V36 EF55	270	270	270	—	38	

Valve	*Anode Volts*	*Screen Volts*	*Suppressor-grid Volts*	*Control-grid Volts*	*Cathode Volts*	*Remarks*
V37 (a) ECC91 (b)	248 252	— —	— —	— —	98 98	
V38 EF50	231	258	—	—	—	
V39 EF50	250	258	—	—	—	

** Measured with high-impedance waveform monitor or valve voltmeter*

Lining-up Instructions

Apparatus required:

Television Waveform Monitor, TV/WM/1
Avometer, Model 7 or 40
Picture Monitor
Video-frequency Oscillator, 10 kc/s–3 Mc/s

1. Switch on power supplies and allow ten minutes to elapse for unit to warm up.
2. Check that the h.t. voltages are +270 (±5 per cent) and −95 (±5 per cent), and that the l.t. voltages are each 6·3 (±5 per cent).
3. Connect the output of the TV/TG/1 to the waveform monitor AC input plug, and connect a 75-ohm resistor to the *Mon* plug. Set TV/TG/1 controls to COMP. W/F, SYNC AND LIFT, set the *Mains Hold* control to INTERN. and the *Lift* control to mid position.
4. Set the waveform monitor to display a frame-sync signal, and adjust the *Set Broad Pulse Width* control until the duration of the broad pulses is 40 microseconds.
5. Adjust the *Set No. of Broad Pulses* control to give eight broad pulses in the frame-sync signal.
6. Adjust the *Set Frame Suppn. Width* control until the duration of the suppression period is that of 14 lines; adjustment of the control should alter the suppression period in discrete half-line steps.
7. Set the waveform monitor to display a complete line. Adjust the *Set Line Sync Width* control until the duration of the line-sync pulse is 10 microseconds.
8. Adjust the *Set Line Suppn. Width* control until the duration of the line suppression period is 16·5 microseconds.
9. Set *Lift* control to zero. Adjust *Set Zero Lift* to give the correct black level. Adjust the *Set Meter Zero* control so that the lift meter reads zero.
10. Adjust the *Set Sync Amplitude* control so that the output sync-pulse amplitude is 0·3V.
11. Set the *Lift* control so that the meter reads 100 and adjust the *Set Peak White Amplitude* control so that the peak-white signal amplitude is 0·7V. Check that the sync-pulse crushing does not exceed 3 per cent.
12. Reduce the *Lift* control setting until the meter reads 75, 50 and 25, successively. Check that the actual percentage lift as measured on the waveform monitor agrees within 1 per cent with the reading of the meter at each setting. Set *Lift* control to zero.
13. Set the signal selector to EXT. SIG. AMP. and inject a signal at 10 kc/s at an amplitude of 0·7V d.a.p. to the *Ext. Sig. Amp.* socket. Check that the external signal-level meter reads mid-scale. A small adjustment of R231, R285 should be made if necessary.
14. Vary the oscillator frequency over the range 10 kc/s to 3 Mc/s. The frequency response as measured by both the external signal meter and the waveform monitor should not vary by more than 0·25 db.
15. Set the signal selector to SAWTOOTH and adjust the *Set Sawtooth Amplitude* control so that the output sawtooth signal amplitude is 0·7V.
16. Set the signal selector to PULSE SIGNALS and the pulse signal selector to SPIKE 1. Adjust the *Set Pulse Picture Amp.* control so that the pulse amplitude is 0·7V. Measure the time of rise, time of fall and overshoot of the pulse.

The rise and fall times should be not greater than 0·12 microseconds and the overshoot not greater than 5 per cent.

17. Set the pulse signal selector to each of the other positions in turn and check that the output pulse amplitude is 0·7V.
18. Apply the output of the generator to the picture monitor, and observe each of the pulse signals in turn. These should produce stationary patterns locked at both line and frame frequencies.

Test Specification

Apparatus required:

Television Waveform Monitor TV/WM/1
Avometer, Model 7 or 40
Video-frequency Oscillator 10 kc/s–5 Mc/s
Double-beam Oscilloscope
Valve Voltmeter
Oscillator covering range 47–51 c/s, capable of 16V r.m.s. output.

During all tests the output of the unit should be terminated in a 75-ohm load. In the following tests voltages are given in d.a.p.; the corresponding approximate r.m.s. for sinusoidal waveforms are given in brackets.

1. Switch on power supplies and allow ten minutes to elapse for unit to warm up.
2. The supply voltages at the 8-way plug should be as follows:

Between Tags	
1 and 2	270V ±5%
1 and 3	95V ±5%
5 and 6	6·3V ±5% r.m.s.
7 and 8	6·3V ±5% r.m.s.

3. Short circuit resistor R234 and throw the *Mains Hold* selector to EXTERN. Apply output from monitoring point M1 to one input of the double-beam oscilloscope and the output from the video-frequency oscillator to the other input. Set the video-frequency oscillator frequency to 20·25 kc/s precisely and adjust C14 until the TV/TG/1 oscillator frequency is also 20·25 kc/s.
4. Connect the output of the TV/TG/1 to the Waveform Monitor AC input plug. Set the TV/TG/1 controls to COMP. W/F, SYNC AND LIFT, and set the Waveform Monitor to display a frame-sync signal. Adjust the *Set Broad Pulse Width* control until the duration of the broad pulses is 40 microseconds.
5. Check the amplitude of the oscillation between the grid of V2 and earth; this should be of the order of 190V (67V). Check that the amplitude of the pulses at the grid of V3(a) and M1 respectively are of the order of 45V and 10V, and that the waveforms at V2 and V3 are as shown in Figs. 6 and 7 (M1, M2).
6. Remove the input to the divider chain and check that the potentials of valves V17 to V26 are as given in the Valve Data section.
7. Restore the input to the divider chain and replace C58 with a variable capacitor having a maximum value of 100 pF. Apply the output from test point M1 to one input of the double-beam oscilloscope and that from M5 to the other. Adjust the variable capacitor to a value midway between the values which cause the circuit to divide by 2 and 4 respectively. The capacitor should then be replaced by a fixed capacitor of the same value; this latter capacitor should be of a high-stability type.
8. Repeat the procedure outlined in 7 above with the next stage, V23; the variable capacitor should have a maximum value of 500 pF and the double-beam oscilloscope inputs should be from M5 and M6 respectively.
9. Repeat 8 for V24, V25 and V26. In the case of the latter, the value of C62 should be midway between the values dividing by 4 and 6.
10. Remove the short circuit from R234 and apply a low-frequency external tone signal of amplitude about 45V (16V) from an impedance of not more than 600 ohms to the *Ext. Hold Sig.* jack. Apply this signal also to one input of the double-beam oscilloscope and that from test point M9 to the other. Check that, as the frequency of the external signal is varied over the range 47·5 to 51 c/s, the two displays remain in synchronism. Set *Mains Hold* control to INTERN. and check by means of the double-beam oscilloscope that the output at test point M9 is synchronised to the mains frequency.
11. Check that the waveforms at V4 and V5 are substantially as shown in Figs. 6 and 7 (M3), and that the electrode potentials are as given in the Valve Data section. Check by means of the double-beam oscilloscope that the frequency of the output at M3 is half that at M1. Check that the *Set Line Suppn. Width* control can be varied over its whole range without affecting the synchronisation or division ratio.

Check that the line-suppression pulses can be varied in duration over the range 14–18 microseconds. Set this period to 16·5 microseconds.

12. Check that the waveforms at V6 and V7 are substantially as shown in Figs. 6 and 8 (M10), and that the electrode potentials are as given in the Valve Data section. Check that with no input the stage is quiescent. Check that the *Set Line Sync Width* control can be adjusted over its whole range without affecting the synchronisation. Check that the line sync period can be varied over the range 8–12 microseconds. Set this period to 10·0 microseconds.
13. Check that the waveforms at V27 are as given in Figs. 7 and 8 (M11) and that the electrode potentials are as given in the Valve Data section. Set the waveform selector switch to LINE W/F and check that the stage is quiescent. Set the waveform selector switch to COMP. W/F and check that the width of the pulse at the test point M11 can be varied in discrete steps by means of the *Set No. of Broad Pulses* control. Observe the TV/TG/1 output waveform and check that the number of broad pulses in the frame-sync waveform can be varied between 6 and 12 by means of the *Set No. of Broad Pulses* control. Set the number of broad pulses to eight.
14. Check that the waveforms at V28 are as given in Figs. 7 and 8 (M14) and that the electrode potentials are as given in the Valve Data section. Set the waveform selector switch to LINE W/F and check that the stage is quiescent. Set the waveform selector switch to COMP. W/F and check that the width of the pulse at the test point M14 can be varied in discrete steps. Observe the TV/TG/1 output waveform and check that the frame-suppression period can be varied between 10 and 18 line periods in half-line steps by means of the *Set Frame Suppn. Width* control. Set the period to 14 lines.
15. Check that the waveforms at V29 and V30 are as shown in Fig. 7 and that the electrode potentials are as given in the Valve Data section. Check that the amplitude of the pulses at the anode of V30 is approximately 40V.
16. Check that the waveforms at V8 are as shown in Fig. 6 and that the electrode potentials are as given in the Valve Data section.
17. Check that the waveforms at V32 and V33 are as shown in Figs. 7 and 8 (M17), and that the electrode potentials are as given in the Valve Data section. Check that the *Set Sync Amplitude* control enables the amplitude of the sync pulses at the TV/TG/1 output to be varied over the range 0·25–0·5V.
18. Check that the electrode potentials of V34, V35 and V36 are as given in the Valve Data section.
19. Connect the video-frequency oscillator to the *Ext. Sig. Amp.* socket. Set the oscillator frequency to 10 kc/s and the output amplitude to 0·7V (0·25V). Connect a valve voltmeter between the anode of V9(b) and earth; the voltage should be 10·5V (3·65V) ±10 per cent. Adjust oscillator output so that the valve voltmeter reads 10·5V, and check that the external signal-level meter reads mid-scale. If necessary a small adjustment to the values of R231, R285 should be made.
20. Vary the input frequency over the range 10 kc/s–5 Mc/s, maintaining the reading of the valve voltmeter constant. The external signal-level meter reading should not vary by more than 1 per cent over this range. Disconnect the valve voltmeter.
21. Transfer the oscillator output to the grid of V35. Terminate the oscillator output in 75 ohms, and set the oscillator output level to + 5·5 db relative to 1V i.e., 1·88V (0·67V). Vary the oscillator frequency over the range 10 kc/s–3 Mc/s and adjust the inductance of L9 to give a maximally-flat response. Reconnect the oscillator to the *Ext. Sig. Amp.* input and reduce input level to 0·7V (0·25V). Vary the oscillator frequency from 10 kc/s–3 Mc/s and adjust L8 to obtain a maximally-flat response as measured on the meter. For a constant input voltage at any frequency between 10 kc/s and 3 Mc/s the reading of the external signal-level meter should be constant to within 1 per cent.
22. Check that the electrode potentials of the valves V10 and V16 are as shown in the Valve Data section.
23. Check that the *Lift* control varies the potential of the suppressor grid of V13 from —100V (maximum) to —2V (minimum). Check that the amplitudes of the suppression pulses at the anodes of V11 and V13 are 3·5V (*Lift* control at minimum).

24. Remove V32. Set the signal selector switch to SYNC AND LIFT and observe the output from the generator with the *Lift* control set at minimum. The amplitude of the line-suppression pulses in the output should be set to zero by means of the *Set Zero Lift* control. If necessary R85, C28 and L11 should be adjusted to give precise cancellation. The settings of the four controls R85, R89 (*Set Zero Lift*), C28 and L11, are interdependent. If adjustment is necessary, a trial setting of R85 should be selected, and R89, C28 and L11 adjusted in turn for best cancellation. This cycle should be repeated until no further improvement is obtained.
25. Set the *Lift* control to maximum and check that the *Set Peak White Amplitude* control permits variation of the lift signal over the range 0·65–0·75V. Set the control so that the lift amplitude is 0·7V.
26. Set the *Lift* control to minimum and adjust the *Set Meter Zero* control to read zero on the meter. Increase the *Lift* control setting to maximum and check that the meter reads full scale (100).
27. With V32 removed, connect the video-frequency oscillator to the *Ext. Sig. Amp.* input and set the oscillator output level so that the external signal-level meter reads mid-scale. Set the signal selector switch to EXT. SIG. AMP. and connect the valve voltmeter to the generator output. Vary the frequency of the oscillator over the range 10 kc/s–4 Mc/s, maintaining the reading of the external signal-level meter constant at all frequencies. The valve voltmeter reading should be constant within 0·2 db from 10 kc/s–3 Mc/s; the response at the higher frequencies may be adjusted by means of the inductor L6 in the anode of V14.
28. Connect the Waveform Monitor DC input to the grid of V11, and using the *Open Grid* condition, observe the frame waveform. Any tilt of the pulse base line should be removed by adjustment of the value of C25. Transfer the waveform monitor to the grid of V10 and adjust C26 if necessary.
29. With V32 removed, set *Lift* control to minimum, connect the waveform monitor to the output of the TV/TG/1 (employing *Direct* condition) and observe frame waveform. With the *Set Zero Lift* control set as in (24), the frame-suppression pulses should not produce any output; if, however, any output is obtained, this should be removed by adjustment of the values of C19 and C13. Replace V32.
30. Check that the waveforms at V37, V38 and V39 are as shown in Fig. 8 and that the electrode potentials are as given in the Valve Data section. Check that in the *Line* 2 position of the pulse signal selector switch the pulses are of 2 microseconds duration, i.e. the circuit is triggered at each 25th cycle. If necessary adjust the *Line* 2 *Pulse Lock* control to obtain this result.
31. Check that the waveforms at V31 are as shown in Fig. 7 and that the electrode potentials are as given in the Valve Data section. Check that the amplitude of the sawtooth at the output is 0·7V and if necessary adjust the *Set Sawtooth Amplitude* control to achieve this. The sawtooth waveform observed at the output should appear completely linear.

COMPONENT TABLE FIG. 5

All capacitors are 350 volt d.c. (working) types, unless otherwise specified

Comp.	Loc.	Type	Tolerance Per cent
C1	B1	T.C.C. 62	± 15
C2	G2	,, CP37N/PVC	± 20
C3	V1	Plessey CE811/1 450V	−20 + 50
C4	W2	,, CE 809/1 450V	,, ,,
C5	R5	Muirhead 233 250V	± 1
C6	S2	,, ,, ,,	,,
C7	D2	T.C.C. CSM 20N	± 5
C8	D2	,, ,, ,,	,,
C9	E2	,, ,, ,,	,,
C10	E2	,, ,, ,,	,,
C11	F2	,, ,, ,,	,,
C12	P2	,, 62	± 15
C13	L12	,, 425 SMP FIN. E	± 1
C14	B2	Wingrove and Rogers C8·03	
C15	B2	T.C.C. 425 SMP	± 5
C16	I2	,, CP32N/PVC	± 25
C17	J2	,, CSM20N	± 5
C18	L2	,, ,,	,,
C19	T2	,, 425 SMP FIN. E	± 1
C20	W2	,, CP35N/PVC	± 20
C21	F3	,, CSM20N	± 5
C22	M3	,, CP32N/PVC	± 25
C23	H3	,, ,,	,,
C24	O3	,, ,,	,,
C25	R3	,, CP33N/PVC	± 20
C26	S3	,, ,,	,,
C27	I4	,, SM3N	± 2
C28	T4	Wingrove and Rogers C8·03	
C29	Y4	T.C.C. CE41C 25V	−20 + 50
C30	B4	,, CSM20N	± 5
C31	C4	,, ,,	,,
C32	H4	,, CP37N/PVC	± 20
C33	P4	,, CP91N/PVC	,,
C34	G4	,, CSM20N	± 5
C35	J4	,, CP35N/PVC	± 20
C36	M4	,, 62	± 15
C37	O4	,, ,,	,,
C39	K5	,, CP37N/PVC	± 20
C40	U5	,, ,,	,,
C41	X5	,, 62	± 15
C42	L5	,, CP37N/PVC	± 20
C43	O5	Plessey CE17078/1 50V	−20 + 100
C44	S5	T.C.C. CP37N/PVC	± 20
C46	N7	Plessey CE809/1 450V	−20 + 50
C47	P7	,, ,, ,,	,, ,,
C48	Y7	,, ,, ,,	,, ,,
C49	Y7	,, CE808/1 ,,	,, ,,
C50	A7	T.C.C. 62	± 15
C51	Q8	T.C.C. CP37N/PVC	± 20
C52	W7	,, ,,	,,
C53	D8	,, 62	± 15
C54	F8	Plessey 808/1 450V	−20 + 50
C55	H8	,, ,, ,,	,, ,,
C56	J8	,, CE809/1	,, ,,
C57	W8	T.C.C. CP37N/PVC	± 20
C58	C8	,, 101 SMP FIN. E	± 1
C59	E8	,, 401 ,, ,,	,,
C60	G8	,, 501 ,, ,,	,,
C61	I8	,, 425 ,, ,,	,,
C62	K8	,, 701 SMB ,,	,,
C63	P8	,, CP37N/PVC	± 20
C64	T8	,, CP33N/PVC	,,
C65	G8	,, 501 SMP FIN. E	± 1
C66	N8	,, 601 SMP ,,	± 5
C67	N8	,, CSM60N	,,
C68	P8	,, 601 SMP FIN. E	,,
C69	P8	,, CSM20N	,,
C70	R8	,, CP32N/PVC	± 25
C71	U8	,, CSM20N	± 5
C72	A9	,, ,,	,,
C73	C9	,, ,,	,,
C74	F9	,, ,,	,,
C75	H9	,, ,,	,,
C76	J9	,, ,,	,,
C77	L9	,, ,,	,,
C78	V9	,, ,,	,,
C79	Y9	,, SM3N	,,
C80	O10	,, CSM20N	,,
C81	V10	,, ,,	,,
C82	S10	Plessey CE809/1 450V	−20 + 50
C83	R10	T.C.C. 62	± 15
C84	M10	,, CP36N/PVC	± 20
C85	T10	,, ,,	,,
C86	U11	Plessey CE809/1 450V	−20 + 50
C87	X11	T.C.C. CP37N/PVC	± 20
C88	Y11	,, ,,	,,
C89	E12	,, CP47S/PVC 500V	,,
C90	E12	,, 62	± 15
C91	H12	,, ,,	,,
C92	P12	,, ,,	,,
C93	U13	,, CP32N/PVC	± 25
C97	E14	,, 62	± 15
C98	E14	,, ,,	,,
C99	G14	,, CP35N/PVC	± 20
C100	I14	,, ,,	,,
C101	L14	,, CP47S/PVC 500V	,,
C102	N13	,, ,,	,,
C103	M14	,, ,,	,,
C104	Q14	,, ,,	,,

Component Table Fig. 5 Continued

Comp.	Loc.	Type	Tolerance Per cent
C105	T14	T.C.C. CP47S/PVC 500V	± 20
C106	I15	,, 62	± 15
C107	R14	,, CSM20N	± 5
C110	T14	,, SM3N	,,
C111	T14	Plessey A.2	
C112	T14	T.C.C. 501 SMP FIN. E	± 5
C113	T15	,, CSM20N	,,
C114	T15	,, ,,	,,
C115	I15	,, 62	± 15
C116	T15	,, SM3N	± 5
C117	N16	,, SCE 76PE/PVC 450V	−20 + 50
C118	P16	,, ,, ,,	,, ,,
C119	R3	,, 101 SMP FIN. E	± 10
C120	N2	,, CSM20N	± 5
C122	V3	,, CP37N/PVC	± 20
C123	G2	Hunts B818 400V	,,
C124	I2	,, ,, ,,	,,
C125	A10	,, ,, ,,	,,
C126	M2	,, ,, ,,	,,
C127	N8	T.C.C. 32N/PVC	± 25
C128	R8	,, ,,	,,
C129	P14	,, ,,	,,
C130	O8	,, ,,	,,
C131	Q2	Hunts B818 400V	± 20
C132	W8	,, ,, ,,	,,
C133	F15	T.C.C. CP37N/PVC	,,
C134	C5	,, 401 SMP FIN. E	± 10
L1	D2	BBC Dwg No. DA486	
L2	D2	,,	
L3	E2	,,	
L4	E2	,,	
L5	F2	,,	
L6	V2	BBC D1/22	
L7	E13	Wearite 214	
L8	G13	BBC D1/23	
L9	H13	,, D1/22	
L10	O13	,, D1/23	
L11	V5	,, ,,	
R1	C1	Dubilier BTB 1W	± 10
R2	G1	Erie 9 0·25	,,
R3	I1	,, ,, ,,	,,
R4	L1	,, ,, ,,	,,
R6	V1	Welwyn A3635	± 5
R7	W1	Erie 9 0·25W	± 10
R8	P1	,, ,, ,,	,,
R10	Q1	,, 108 0·5W	± 1
R11	R1	Colvern CLR 4001/22	
R12	S1	Erie 9 0·25W	± 10
R13	T1	,, 108 0·5W	± 1
R14	C2	,,	± 2

Comp.	Loc.	Type	Tolerance Per cent
R15	F2	Erie 9 0·25W	± 10
R16	G2	,, 9 0·25W	,,
R17	G2	,, ,, ,,	± 10
R18	H2	,, 109 ,,	± 2
R19	I2	,, 9 ,,	± 10
R20	J2	,, ,, ,,	,,
R21	J2	,, ,, ,,	,,
R22	L2	,, 100 1W	± 2
R23	L2	,, 9 0·25W	± 10
R24	M2	,, 109 ,,	± 2
R25	N2	,, 9 ,,	± 10
R26	N2	Dubilier BTB 1W	,,
R27	Q2	Erie 108 0·5W	± 1
R28	T2	,, ,, ,,	,,
R29	G2	,, 9 0·25W	± 10
R30	P2	,, ,, ,,	,,
R31	T2	Welwyn C23 0·5W	± 2
R32	U2	,, ,, ,,	,,
R33	V3	Erie 108 0·5W	± 2
R34	X2	,, 9 0·25W	± 10
R35	H3	,, ,, ,,	,,
R36	I3	,, ,, ,,	,,
R37	K3	,, ,, ,,	,,
R38	L3	,, ,, ,,	,,
R39	P3	,, ,, ,,	,,
R40	P3	,, ,, ,,	,,
R41	Q3	,, ,, ,,	,,
R42	S3	,, ,, ,,	,,
R43	U3	,, ,, ,,	,,
R44	W3	,, ,, ,,	,,
R45	X3	,, ,, ,,	,,
R46	M3	,, ,, ,,	,,
R47	N3	,, 5B 0·1W	,,
R48	P3	,, 9 0·25W	,,
R49	L13	,, ,, ,,	,,
R50	A3	,, ,, ,,	,,
R51	C3	,, ,, ,,	,,
R52	F3	,, ,, ,,	,,
R53	F3	,, 109 ,,	± 2
R54	G3	,, 9 ,,	± 10
R55	J4	,, ,, ,,	,,
R56	K4	,, ,, ,,	,,
R57	K4	,, ,, ,,	,,
R58	Q4	,, ,, ,,	,,
R59	V4	Colvern CLR 1106/95	
R60	A4	Erie 109 0·25W	± 2
R61	C4	,, 9 ,,	± 10
R62	H4	,, 100 1W	± 2
R63	I4	,, 9 0·25W	± 10
R64	I4	,, ,, ,,	,,
R65	K4	Dubilier BTB 1W	,,
R66	L4	Erie 108 0·5W	± 5

Component Table Fig. 5 Continued

Comp.	Loc.	Type	Tolerance Per cent	Comp.	Loc.	Type	Tolerance Per cent
R67	N4	Erie 9 0·25W	± 10	R115	I7	Welwyn C23 0·5W	± 2
R68	Q4	,, ,, ,,	,,	R116	J7	Erie 9 0·25W	± 10
R69	Q4	,, ,, ,,	,,	R117	L7	,, ,, ,,	,,
R70	S4	,, ,, ,,	,,	R118	L7	Welwyn C23 0·5W	± 2
R71	T4	,, ,, ,,	,,	R119	M7	Erie 9 0·25W	± 10
R72	L14	,, 108 0·5W	± 1	R120	P7	,, ,, ,,	,,
R73	V4	,, ,, ,,	± 2	R121	T7	,, ,, ,,	± 5
R74	W4	,, ,, ,,	,,	R122	E8	,, 108 0·5W	± 2
R75	X4	,, 9 0·25W	± 10	R123	G8	,, ,, ,,	,,
R76	X4	,, 109 ,,	± 2	R124	G8	,, ,, ,,	,,
R77	C4	Morganite LHAP/50450/ 20000		R125	K8	,, ,, ,,	,,
				R126	R8	,, 9 0·25W	± 10
R78	E4	Erie 9 0·25W	± 10	R127	S8	,, ,, ,,	,,
R79	G4	,, ,, ,,	,,	R128	V7	Morganite LHAP/50250/ 48000	
R80	H4	,, ,, ,,	,,				
R81	I4	Morganite LHAP/10350/ 20000		R129	W7	Erie 9 0·25W	,,
				R130	A8	,, 108 0·5W	± 2
R82	K4	Erie 9 0·25W	± 10	R131	B8	,, ,, ,,	,,
R83	L4	Morganite LHAP/25350/ 20000		R132	C8	,, ,, ,,	,,
				R133	F8	,, ,, ,,	,,
R84	P4	Erie 9 0·25W	± 10	R134	H8	,, ,, ,,	,,
R85	Q4	Morganite BJ/10250/ 20000		R135	J8	,, ,, ,,	,,
				R136	M8	,, ,, ,,	,,
R86	L14	Morganite LHAP/10450/ 48000		R137	M8	,, 9 0·25W	± 10
				R138	O8	,, 108 0·5W	± 2
R87	X4	Erie 9 0·25W	± 10	R139	P8	,, 9 0·25W	± 10
R88	W10	,, ,, ,,	,,	R140	S8	,, ,, ,,	,,
R89	P5	Morganite LHAP/20350/ 48000		R141	U8	Welwyn A3632 0·5W	± 2
				R142	U8	Erie 9 0·25W	± 10
R90	P4	Erie 9 0·25W	± 10	R143	V8	,, ,, ,,	,,
R91	W4	,, 108 0·5W	± 2	R144	W8	,, ,, ,,	,,
R92	V5	,, 100 1W	± 2	R145	B9	,, ,, ,,	,,
R93	W5	,, 108 0·5W	± 1	R146	D9	,, ,, ,,	,,
R94	X5	,, 9 0·25W	± 10	R147	F9	,, ,, ,,	,,
R95	C5	,, ,, ,,	,,	R148	H9	,, ,, ,,	,,
R97	K5	,, ,, ,,	,,	R149	J9	,, ,, ,,	,,
R98	P5	,, ,, ,,	,,	R150	C9	,, ,, ,,	,,
R100	M7	,, ,, ,,	,,	R151	E9	,, ,, ,,	,,
R101	O7	,, ,, ,,	,,	R152	S9	,, ,, ,,	,,
R102	Q7	Dubilier BTB 1W	,,	R153	I9	,, ,, ,,	,,
R103	S7	,, ,, ,,	,,	R154	K9	,, ,, ,,	,,
R104	A7	Erie 9 0·25W	,,	R155	Q9	,, ,, ,,	,,
R105	C7	,, ,, ,,	,,	R156	R9	,, ,, ,,	,,
R106	C7	Welwyn C23 0·5W	± 2	R157	U9	,, ,, ,,	,,
R107	C7	Erie 9 0·25W	± 10	R158	W9	,, ,, ,,	,,
R108	E7	,, ,, ,,	,,	R159	X9	,, ,, ,,	,,
R109	E7	Welwyn C23 0·5W	,,	R160	Q9	,, ,, ,,	,,
R110	F7	Erie 9 0·25W	,,	R161	Y9	,, ,, ,,	,,
R111	G7	,, ,, ,,	,,	R162	A9	,, 108 0·5W	± 2
R112	G7	Welwyn C23 0·5W	± 2	R163	B10	,, 9 0·25W	± 10
R113	H7	Erie 9 0·25W	± 10	R164	C9	,, 108 0·5W	± 2
R114	I7	,, ,, ,,	,,	R165	F9	,, ,, ,,	,,

Component Table Fig. 5 Continued

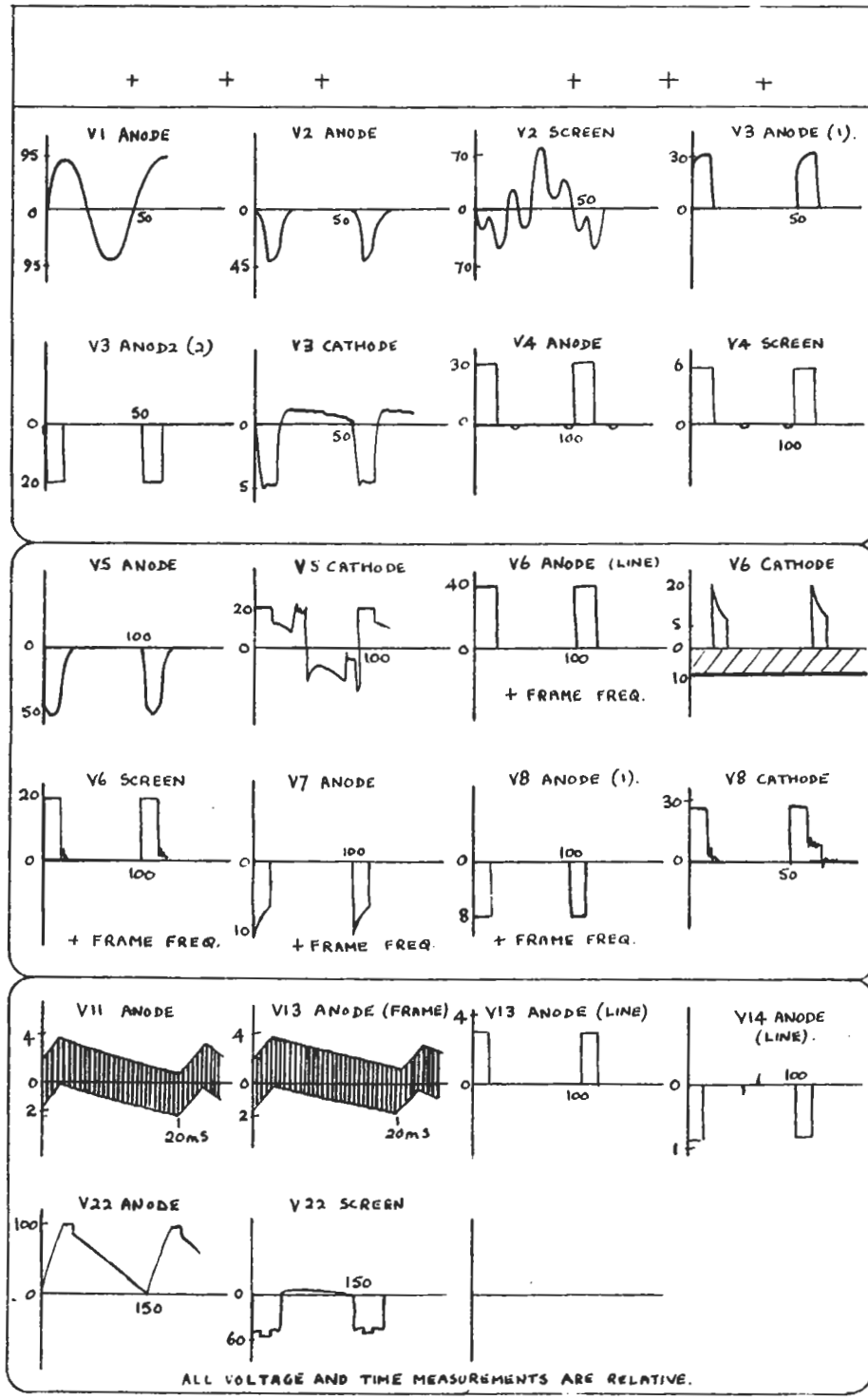
Comp.	Loc.	Type	Tolerance Per cent
R166	H9	Erie 108 0·5W	±2
R167	J9	,, ,, ,,	,,
R168	L10	,, 9 0·25W	± 10
R169	M10	,, ,, ,,	,,
R170	N10	,, 108 0·5W	± 2
R171	P10	,, ,, ,,	,,
R172	V10	,, 109 0·25W	,,
R173	W10	,, 108 0·5W	,,
R174	Y10	,, ,, ,,	,,
R175	O10	,, 9 0·25W	± 10
R176	T10	,, ,, ,,	,,
R177	Y10	,, 108 0·5W	± 2
R178	A10	,, ,, ,,	,,
R179	C10	,, ,, ,,	,,
R180	D10	,, 9 0·25W	± 10
R181	F10	,, 108 0·5W	± 2
R182	F10	,, 9 0·25W	± 10
R183	H10	,, 108 0·5W	± 2
R184	I10	,, 9 0·25W	± 10
R185	J10	,, 108 0·5W	± 2
R186	K10	,, 9 0·25W	± 10
R187	L10	,, ,, ,,	,,
R188	M10	Dubilier BTB 1W	,,
R189	N10	Morganite LHAP/10450/ 20000	
R190	O10	Dubilier BTB 1W	± 10
R191	P10	Morganite LHAP/25450/ 20000	
R192	Q10	Erie 9 0·25W	± 10
R193	R10	,, ,, ,,	,,
R194	S10	,, ,, ,,	,,
R195	T10	,, ,, ,,	,,
R196	W10	Reliance TW	
R197	Y10	Erie 108 0·5W	± 2
R198	A11	,, ,, ,,	,,
R199	C11	,, ,, ,,	,,
R200	F11	,, ,, ,,	,,
R201	H11	,, ,, ,,	,,
R202	J11	,, ,, ,,	,,
R203	F12	,, 9 0·25W	± 10
R205	G12	,, ,, ,,	,,
R206	H12	,, ,, ,,	,,
R207	I13	,, ,, ,,	,,
R208	C12	,, 109 ,,	± 2
R209	S12	,, ,, ,,	,,
R210	V12	,, 9 ,,	± 10
R211	K13	,, ,, ,,	,,
R212	J13	,, ,, ,,	,,
R213	E13	,, ,, ,,	,,
R214	S13	,, ,, ,,	,,
R215	T13	Welwyn C23 0·5W	± 2
R216	U13	Erie 9 0·25W	± 10
R217	X13	Erie 9 0·25W	± 10
R218	J13	,, ,, ,,	,,
R219	M13	,, ,, ,,	,,
R220	H13	,, ,, ,,	,,
R221	I13	,, ,, ,,	,,
R222	J14	,, ,, ,,	,,
R223	J13	,, ,, ,,	,,
R224	O13	,, ,, ,,	,,
R225	O13	,, ,, ,,	
R226	T14	,, 108 0·5W	± 2
R227	F15	,, 9 0·25W	± 10
R228	J14	,, 108 0·5W	± 2
R229	D14	,, 9 0·25W	± 10
R230	J14	,, 108 0·5W	± 2
R231	M14	,, ,, ,,	,,
R232	O14	,, 9 0·25W	± 10
R233	E15	,, ,, ,,	,,
R234	F15	,, ,, ,,	,,
R235	G15	,, ,, ,,	,,
R236	H15	,, ,, ,,	,,
R237	J14	,, 108 0·5W	± 2
R238	J14	,, ,, ,,	,,
R239	J15	,, ,, ,,	,,
R240	J15	,, ,, ,,	,,
R241	N15	,, 9 0·25W	± 10
R242	O15	,, ,, ,,	,,
R243	P15	Welwyn A3635 2W	± 5
R244	P15	Erie 9 0·25W	± 10
R245	F15	,, 109 ,,	± 2
R246	G15	,, ,, ,,	,,
R247	H15	,, 9 ,,	± 10
R248	H15	,, 109 ,,	± 2
R249	J15	,, 108 0·5W	,,
R250	J15	,, ,, ,,	,,
R251	O15	,, 9 0·25W	± 10
R252	R15	,, 100 1W	± 2
R253	T15	,, ,, ,,	,,
R254	J16	,, 108 0·5W	,,
R255	J16	Welwyn C24 0·25W	± 5
R256	O16	Erie 9 0·25W	± 10
R257	P16	Morganite LHAP/10350/ 48000	
R258	R16	Erie 108 0·5W	± 2
R259	U16	,, ,, ,,	,,
R260	D14	,, 9 0·25W	± 10
R261	S16	,, 100 1W	± 2
R262	U16	,, 108 0·5W	,,
R263	S16	,, 100 1W	,,
R264	V16	,, ,, ,,	,,
R265	V16	Welwyn A3635 2W	,,
R280	O9	Erie 9 0·25W	± 10
R281	M9	,, ,, ,,	,,

Component Table Fig. 5 Continued

Comp.	Loc.	Type	Tolerance Per cent	Comp.	Loc.	Type	Tolerance Per cent
R282	G13	Erie 9 0·25W	±10	R288	G16	Erie 9 0·25W	±10
R283	I4	,, ,, ,,	,,	T1	C2	BBC LD/105/5B	
R284	V3	,, ,, ,,	,,	T2	C13	BBC M160	
R285	M14	,, ,, ,,	,,	W1, 2, 3, 4	D14	Westinghouse W6	

FIG 5 V3

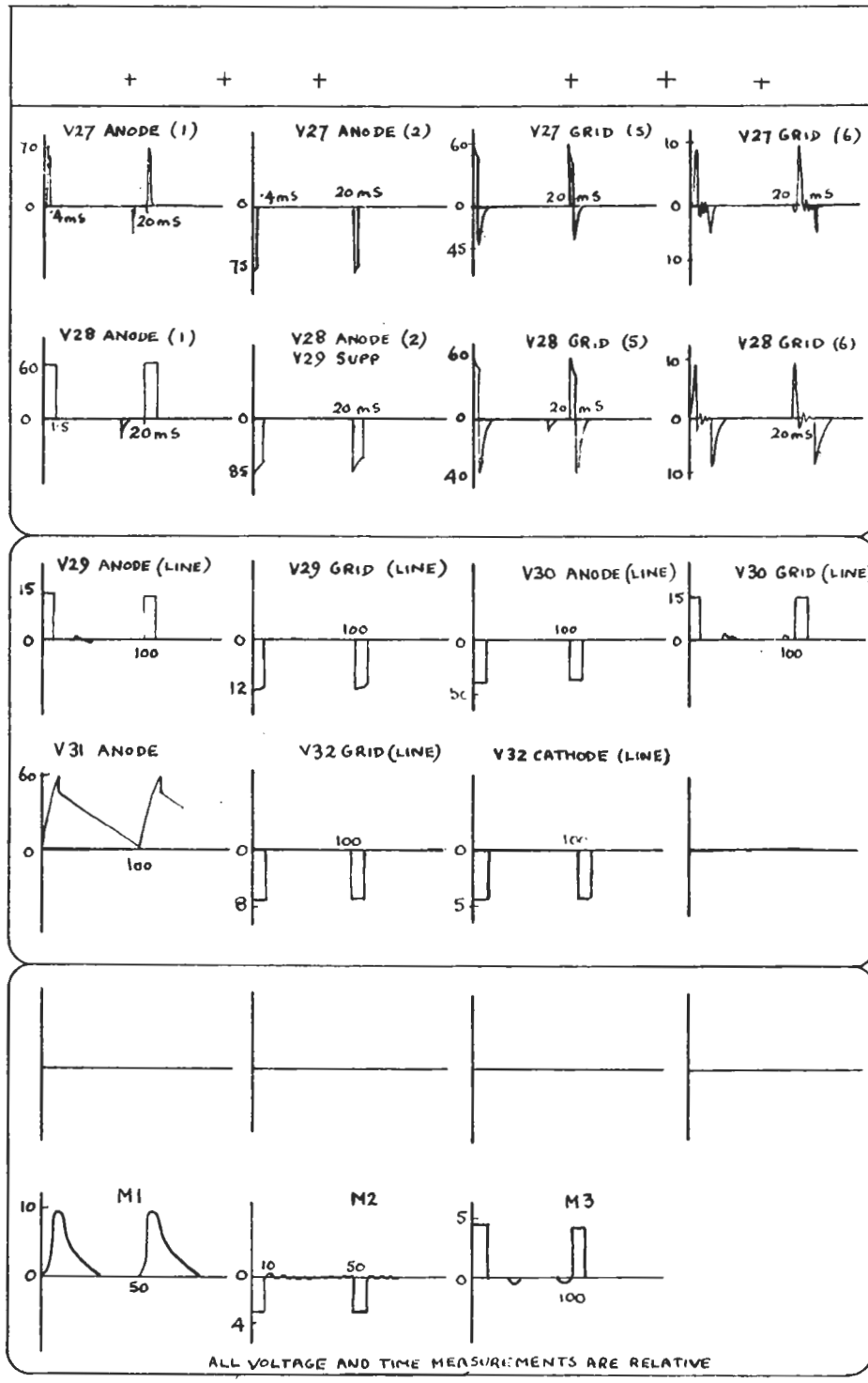
TELEVISION TEST GENERATOR TV/TG/1 CIRCUIT



TELEVISION TEST GENERATOR TV/TG/1
TYPICAL WAVEFORMS (1)

55/GGJ/008
DSKB/1106

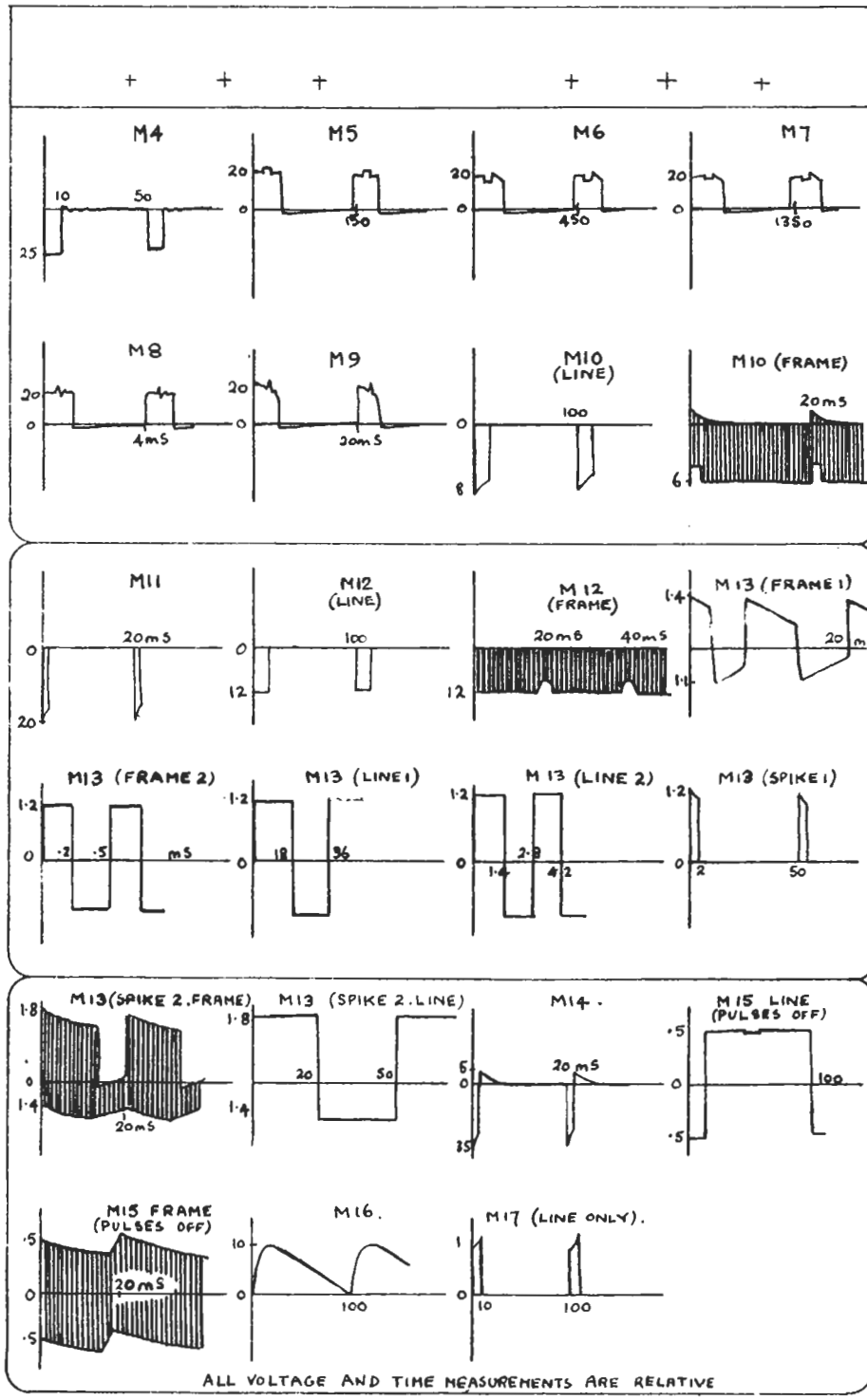
FIG 7 V3



TELEVISION TEST GENERATOR TV/TG/1
TYPICAL WAVEFORMS (2)

55/GGJ/009
DSKB/1107

FIG 8 V3



TELEVISION TEST GENERATOR TV/TG/1
TYPICAL WAVEFORMS (3)