SECTION 2

STABILISING AMPLIFIERS: TV/STA/2 SERIES

Introduction

The TV/STA/2 stabilising amplifier and variant forms of that equipment have almost identical circuits. The series includes a TV/STA/2A version produced for use at low-power transmitting stations, and also a portable version identified by the coding TV/PSTA/1. Information on variants follows a detailed description of the parent TV/STA/2 equipment. Note the reference, on page 2.15, to an optional noise-limiting feature in these amplifiers.

TV/STA/2

The TV/STA/2 is a multi-purpose video-frequency unit, designed to work between 75-ohm terminations. The normal signal output level is 1 volt d.a.p.; the overall gain, when employed as a straightforward amplifier, has a maximum value of 6 db. The unit is mounted on a 19 × 10½ inch panel suitable for bay mounting; when so mounted, it projects through the bay. Input and output connections are made via *Musa* plugs at the rear of the unit; monitoring plugs are mounted on the front panel. Power supplies are normally obtained from a Stabilised Power Supply Unit being made by an eight-pin plug at the rear of the unit.

The unit provides a number of important facilities, which can be employed when required. These comprise:

(a) Equalisation for standard lengths of coaxial cable Type PT11YM, up to 2,200 feet.
(b) Line frequency black-level clamping.
(c) Stabilisation of output sync-pulse amplitude; this remains substantially constant for a variation of up to 12 db in input sync-pulse amplitude.
(d) Independent control of the output amplitudes of the picture and the sync pulses; the range of variation of sync pulse output amplitude is approximately 0·3-0·4 volt, so that the picture/sync ratio can be varied between 7 : 3 and 6 : 4, at the normal output of 1 volt d.a.p.

When (b), (c) and (d) are employed, it is essential for the correct operation of the unit that the input picture signal is positive-going. These facilities are employed when it is desired to minimise the effect of certain forms of signal distortion, occurring particularly when a number of links in series are used. Such links may include lengths of coaxial cable and a number of amplifiers. Where coaxial lines are included in the signal chain, pick-up from the power-supply mains may occur, and equalisation for high-frequency losses may be necessary. The amplifiers may introduce appreciable low-frequency distortion, and if overload occurs, the amplitude of the sync pulses may change with changes of picture content.

Circuit Description

A complete circuit diagram of the stabilising amplifier is shown in Fig. 2. The amplifier can be considered in five sections; these are (a) cable equaliser, (b) video-frequency amplifier (V1-V5), (c) black-level clamping and sync-pulse stabilising stage (V6), (d) output stage (V7), and (e) black-level clamp-pulse derivation chain. These sections will be described in the order set out above.

(a) *Cable Equaliser*

The cable equaliser comprises five sections of similar type in cascade. Each section comprises a constant-resistance equaliser network, which is shown in basic form in Fig. 2.1. This type of equaliser is discussed in detail in Television Engineering, Volume 4. The output from the equaliser is assumed terminated in a resistance R_0; then provided that $R_1+R_0R_2/(R_0+R_2)=R_0$ and $R_0^2=L/C$, the input impedance of the equaliser is resistive and equal in value to R_0 at all frequencies. The equalising characteristic of the section is shown diagrammatically in Fig. 2.2. The total low-frequency loss is given by $g_1/(g_0+g_1+g_2)$, where $g_0=1/R_0$ etc. The shape

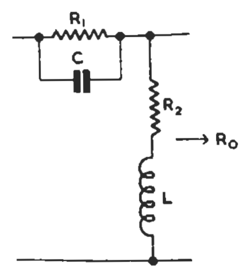

Fig. 2.1 TV/STA/2: Basic Form of Cable Equaliser Sections

of the characteristic is determined by the values of L and C; the larger the value of L, the lower is the frequency region in which the effective change of attenuation occurs.

Five such sections are provided, and in each the series capacitor and shunt inductance can be removed from circuit by the operation of a key; when this is done, the section behaves solely as an attenuator. The first section introduces a loss of 1 db at low frequencies; at 3 Mc/s the loss is 0·1 db, so that the equalising characteristic rises by 0·9 db from low frequencies to 3 Mc/s. This amount of top lift just offsets the h.f. loss in 200 feet of coaxial cable Type PT11YM. In the second and third sections, the components are chosen to compensate for the losses in 400 and 600 feet of cable respectively. The fourth and fifth sections operate together to compensate for the losses in

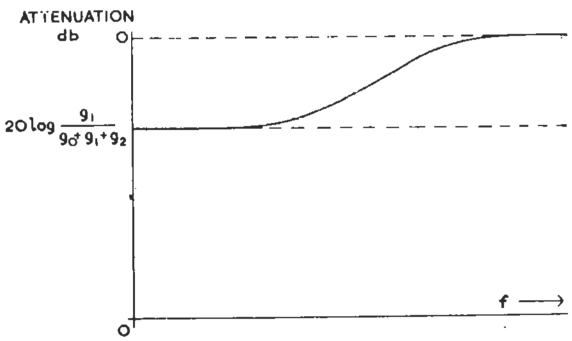

Fig. 2.2 TV/STA/2: Equalisation Characteristic of Cable Equaliser Section

1,000 feet of cable. Two sections are necessary in order to secure simultaneously the right amount of lift at 3 Mc/s with the correct slope of equalising characteristic. With a single section, these conditions cannot be satisfied simultaneously.

Because of the constant-resistance property of each section, the action of the sections are independent. It is thus possible to equalise for lengths of cable up to a total of 2,200 feet, the equalising characteristic employed being that appropriate to the nearest multiple of 200 feet. The overall low-frequency attenuation of the equaliser is 12 db. The equaliser is terminated by the parallel combination of R1 and R2 (75 ohms); R2 is the gain control.

(b) *Video-frequency Amplifier*

The stages V1-V5 comprise a conventional video-frequency amplifier. Stages V1-V3 employ similar valves, and generally similar circuit arrangements. A shunt-inductance circuit is employed to maintain the high-frequency response; this type of circuit is discussed in detail in Television Engineering, Volume 2. The interstage coupling circuit time constants are staggered to ensure stability at low frequencies. Valve V4 is of a higher current rating than V1-V3, to provide adequate drive to the cathode follower V5. V4 also employs a shunt-inductance circuit; part of the inductance is provided by the wire-wound load resistor R12 itself. For this reason, this resistor should be of the type specified in the Component Table. In order to stabilise the stray capacitance at the output of V4, capacitor C45 is included.

The cathode follower, V5, is of conventional design. The valve type employed, 6F14, is necessary to allow for the high peak currents required for the operation of the black-level clamp.

(c) *Black-level Clamping and Sync-pulse Stabilising Stage*

The black-level clamping is accomplished at the grid of V6. The output from the video-frequency amplifier is fed via a capacitor C (C12, C41 or C42) to the grid of V6, to which is connected also the anode of the diode V11(a) and the cathode of the diode V11(b). Except for a short interval at the clamping period, the diodes are non-conducting.

The voltage at the grid of V6 comprises the sum of the signal voltage and a quasi zero-frequency component. This latter is equal to the voltage at which the black level is clamped. The action of the clamping circuit is as follows:—

At the end of the line-sync pulse period, two short pulses of duration of the order of four microseconds are applied simultaneously to the diodes V11(a) and V11(b). The magnitudes and polarities of these pulses are such that the valves are driven hard into conduction. The circuit condition can then be represented by the equivalent diagram of Fig. 2.3; in this figure the components connected to the junction of the diodes have been omitted. The voltage E represents the amplitude of the clamping pulses, R1, the source resistance of the pulse generators, whilst R2 and R3 are the leak resistors for the diodes. Since R2 and R3 are each very much greater than R1, the rectification efficiency is high, and a voltage very nearly equal to 2E is developed across R2 and R3 in series.

The presence of the components at the grid of V6 modifies the circuit of Fig. 2.3 to that of Fig.

2.4. In this figure E_c is the voltage across the capacitor C (C12, C41 or C42) R4 is the output resistance of V5, and E_s is the instantaneous signal amplitude during the clamping period. If the signal amplitude is at the level established as the black level in previous clamping periods, E_s is, of course, zero. Assuming that the forward

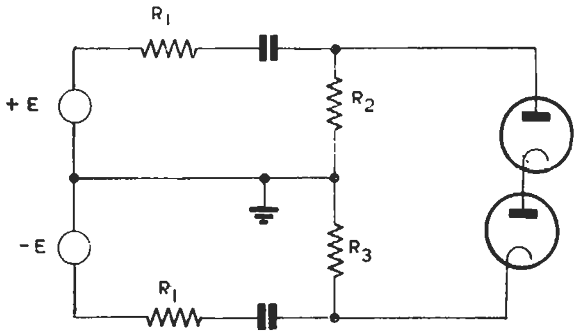

Fig. 2.3. TV/STA/2: Black-level Clamp. Showing Equivalent Circuit Diagram at Instant of Clamping, omitting the Components at the Junction of the Diodes

resistances of the diodes are equal, the circuit may be treated as that of a bridge, and the voltage between points A and earth during the clamping period is driven to the value $E\,(R_2-R_3)/(R_2+R_3)$. Of necessity this is equal to E_s+E_c; hence the quiescent value of E_c with $E_s=0$ is $E_c=E(R_2-R_3)/(R_2+R_3)$. If, however, the signal

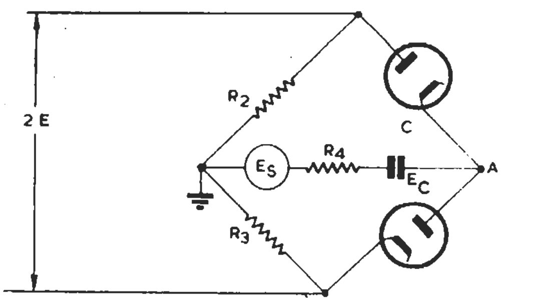

Fig. 2.4. TV/STA/2. Equivalent Circuit Diagram for Determining the Black-level Clamping Voltage

amplitude at the clamping period is not zero, then current will flow to charge or discharge the capacitor C, tending to keep the sum of E_s and E_c constant. If the time constant is sufficiently short, the voltage between point A and earth will be restored to $E(R_2-R_3)/(R_2+R_3)$; i.e. the voltage across the capacitor will have altered by an amount equal to the departure of the signal from its black-level value, and this change will be of opposite polarity to that of the change in signal amplitude. The waveform at the grid of V6 as compared with that at the cathode of V5 is shown in Fig. 2.5. It will be seen, therefore, that provided the time constant associated with the capacitor C is small, the circuit maintains the black level substantially constant, by altering the voltage across the capacitor in discrete steps to achieve this. If the time constant associated with capacitor C is not very short, the clamping action will be imperfect, i.e. the variations in black level instead of being substantially removed,

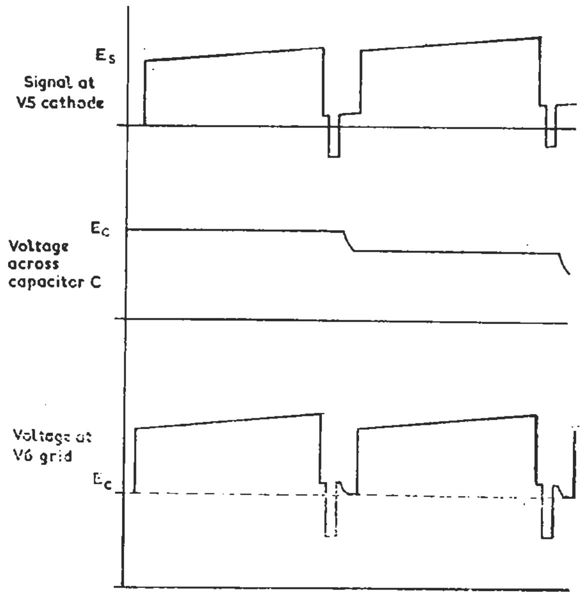

Fig. 2.5. TV/STA/2: Black-level Clamp. Waveforms at Cathode of V5 and Grid of V6

will be only partially cancelled. In the actual circuit a choice of time constant is provided. The reason for this is as follows :—

Clamping pulses are produced from the sync pulses of the signal; a 'spike' of interference of the correct polarity and magnitude may therefore produce a spurious clamping pulse. If a short clamping time constant is employed in such circumstances, the signal will be clamped with the instantaneous signal amplitude at black level. With a longer clamping time constant the black level can only change relatively slowly, and so the effect of a spurious clamping pulse is less marked. Additionally, any noise present during the clamping period will affect the clamping level, and to minimise spurious fluctuations of black level with noise, a long clamping time constant is desirable. Hence in the presence of impulsive interference and noise, a relatively long clamping time constant may be preferred, to reduce the picture distortion arising from spurious clamping action. When this is done, the reduction of low-frequency distortion and hum is lessened. Hence the choice of clamp time constant is a compromise between the two requirements, and a choice of three time constants is provided.

It will be seen in the actual circuit that the black level can be varied by means of R84 (*Set Black Level*) which varies (R_2-R_3) of Fig. B.4. The magnitude of the clamping pulses is 35 volts, so that the black level can be set within the limits of ± 5 volts approximately with respect to earth.

Valve V6 acts as an amplifier for the input signal. A high value of cathode-load resistor is employed, which provides substantial negative current feedback to the picture signal, positive-going at the grid of V6. A crystal diode G1 is connected between the cathode and a point of variable positive potential, the slider of R29 (*Crystal Bias*). Because of the bias applied to the crystal diode, it is non-conductive for the whole range of amplitudes of the picture signal, the setting of R29 being chosen to ensure this. When, however, a sync pulse occurs, and the signal is negative-going, the crystal commences to conduct when the sync-pulse amplitude carries the cathode potential of V6 below the value of that applied to the crystal diode. The effective cathode-earth impedance is then substantially reduced, to a value equal to the forward resistance of the diode (about 150 ohms); with only a small further increase of sync-pulse amplitude, the anode current in V6 is cut off. Thus provided that the input sync pulses are of sufficient amplitude to cut off anode current in V6 as described above, any variation of magnitude is not transmitted. In this way, the amplitude of the output sync pulses is made uniform, irrespective of variations of amplitude in the input signal. This stabilising of sync-pulse amplitude is, of course, possible only because of the constancy of black level produced by the clamping action.

In the anode circuit of V6, provision is made for varying the amplitude of the sync pulses with respect to the picture-signal amplitude; the operation of the circuit is as follows:—

Since the black level of the signal corresponds to a definite value of grid bias, the value of the anode current when the signal is at black level is fixed and does not vary with the anode potential, since V6 is a pentode. At the occurrence of each sync pulse, the anode current is driven to zero. The amplitude of the output sync pulses is thus given by the magnitude of the anode current at black level, multiplied by the anode load of V6. This load comprises the resistor R25, in parallel with the crystal diode G1 and R26 in series. The chain R26, R80, R83 provides a bias for the crystal diode, and ensures that it only conducts when the anode voltage of V6 falls below the bias value. When this occurs, the effective anode load of V6 falls, due to the shunting effect of R26. The crystal bias is normally set so that the diode conducts for the whole range of picture-signal amplitude, and part of that of sync-pulse amplitude. By varying the anode supply voltage to V6 by means of R81 (*Sync. Pulse Amp.*) an equal fall of anode voltage occurs, and the portion of the sync-pulse range over which the diode conducts is altered; as the quiescent anode voltage is lowered, so the portion becomes greater. As the amplification afforded to the signal is lower when the diode is conducting, the two portions of the sync signal are amplified differently. Thus the overall magnitude of the output sync-pulse amplitude can be varied by altering the setting of R81. The gain with G1 conducting is approximately 2/3 of that in the non-conducting condition. The sync-pulse amplitude can consequently be varied over a range of 1·5 : 1.

It will be seen that variations of sync-pulse amplitude can be accomplished by varying R81 or R83 (*Set Sync Range*); R81 alone is used in practice. R83 is a pre-set control which is adjusted to ensure that the variable gain action is confined to the sync pulse only; it is adjusted in combination with R84 which adjusts the black level. Of necessity, the setting of R29 must also be adjusted in conjunction with R84, to ensure that the action of the crystal diode G1 is confined to the sync pulses only.

In order to preserve the frequency response of the stage level at high frequencies, a shunt-inductance L4 is employed, and additionally a small cathode capacitor C43.

When black-level clamping is not required, the unit may be used as a conventional amplifier by throwing switch S7 to *Clamp Out*. When this is done, the signal at the grid of V6 is held with the tips of the sync pulses at earth potential by the d.c. restoring action of V11(b). The discharge time constant associated with this d.c. restoration circuit is very long, since the discharging resistor comprises the leakage paths from the grid of V6 to earth only. The differential cathode feedback due to G1 is defeated in this condition, since the circuit to the crystal diode is interrupted. The differential amplification circuit in the anode is also non-operative, since the bias is such that, with a normal amplitude input signal, the anode potential of V6 does not fall below the value at which the crystal diode G4 conducts.

(d) *Output Stage*

The output stage comprises V7. Current feedback is applied by R35 to reduce non-linear distortion in the valve, and to increase the apparent value of R31, to ensure adequate low-frequency response. The output is fed from the anode of V7 to the output socket via C15. The principal components of the anode load are R37, and the external circuit. Under normal conditions, this latter circuit will also represent a load of 75 ohms, so that the total load of V7 is some 37·5 ohms.

(e) *Black-level Clamp-pulse Derivation Chain*

The signal at the cathode of V5 is fed via C10 and C16 to the grid of V8. Black-level clamping is introduced at the junction of C10 and C16; the reason for this will be discussed later. Waveforms at various points in the chain are shown in Fig. 2.6. From the grid of V8 to earth is the crystal diode G2; this serves to clamp the negative-going peaks of the sync signals at earth potential. V8 has a large cathode bias resistor, so that under quiescent conditions it is biased nearly to cut-off; the tips of the sync pulses are thereby partially 'crushed,' reducing the relative amplitude of noise at the sync bottom. Additionally, the stage employs a high-value anode load. At the peaks of the picture signal, the anode potential is driven to a value below the 'knee' of the i_a-v_a characteristic, i.e. the valve 'bottoms.' By this means partial removal of the picture signal is effected.

From the anode of V8 the signal is passed to the sync separator stage, V9(a). The sync pulses are positive-going at the anode of V8, and the tips of the pulses are clamped at earth potential by grid current in V9(a). As a result, the whole range of picture signal amplitude exceeds the valve cut-off bias, and the signal at the anode of V9(a) comprises negative-going sync pulses only.

The charge time constant associated with the grid circuit of V9(a) is relatively long, due to the high output impedance of V8 (10 kilohms approximately). For this reason, the bias applied to V9(a) cannot be suddenly increased by a 'spike' of interference, which might cause subsequent sync pulses to lie in the region beyond cut-off. This long time constant also serves to minimise 'jitter' due to noise at the sync bottom; in this, the action of the circuit is supplemented by the action of V8, which reduces the relative amplitude of noise at sync bottom.

The pulses at the anode of V9(a) are fed to the grid of V9(b), which is also grid-current biased. The amplitude of the pulses at this grid exceeds the cut-off bias, and hence the output at the anode of V9(b) comprises positive-going sync pulses, with any noise on the tips of the pulses removed in the output.

From the anode of V9(b) the pulses are applied to the differentiating circuit at the input to V10(a). The crystal diode G3 is normally conducting due to the positive bias applied through the resistor R54, and hence presents a low resistance. Thus on the leading edge of the pulse, the positive-going spike is of very small amplitude and very short duration; this spike is then further reduced in amplitude by the action of the grid resistor R55 in combination with grid current in V10(a). The negative-going spike coincident with the trailing edge of the pulse drives the crystal diode G3 below earth potential, and hence current in the crystal ceases to flow; its resistance is then much higher. The amplitude of the spike is consequently relatively large, and exceeds the cut-off bias of V10(a). The spike is clipped and amplified in V10(a) and applied to one of the clamping diodes, V11(b). A portion of the signal at the anode of V10(a) (across R57) is fed to the grid of V10(b) where it is amplified and fed to the diode V11(a).

The duration of the spike at the grid of V10(a) is governed by the time constant of the differentiating circuit, determined by the magnitude of C23 and the resistance of R54 and the back resistance of the crystal G3 in parallel. The clamping pulses developed at the anodes of V10(a) and V10(b) are at peak value for a period of 2 microseconds approximately; the total duration of the pulses is of the order of 5 microseconds.

From the differentiating network (C23, R54, G3) an output is taken to the grid of V12(a). The circuit of V12(a), V12(b), V13(a), V13(b), is

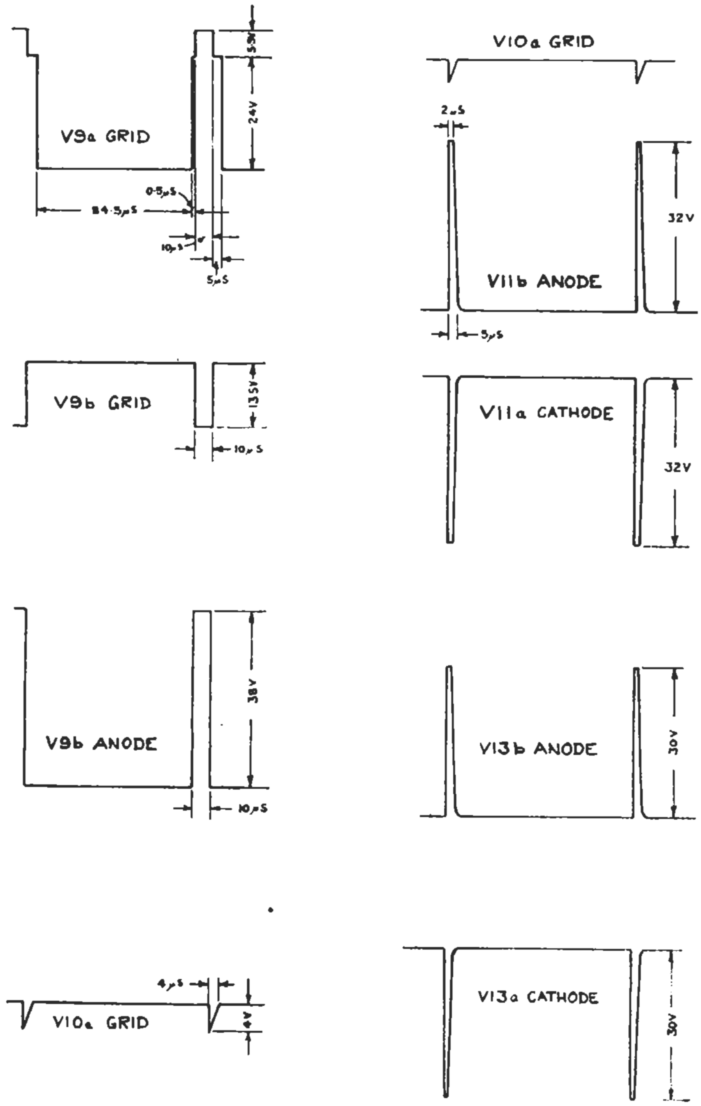

Fig. 2.6. TV/STA/2: Waveforms in Clamp-pulse Derivation Chain

almost identical with that of V10 and V11 described above; this portion of the circuit provides black-level clamping for the signal applied to the input of the clamp pulse derivation chain, clamping occurring at the junction of C10 and C16. The main purpose of this clamp is to minimise any low-frequency distortion of the signal, and to reduce any accompanying hum to negligible proportions; the d.c. restoring circuit at the grid of V8 falls short of the desired performance in this respect, and hence necessitates the employment of the clamp. This black-level clamping circuit employs a relatively long clamp time constant, equal to the largest available at the grid of V6. The reason for this is that it is desirable that the signal to the clamp pulse derivation chain should not be affected by ' spikes ' of interference. Although the signal clamp at the grid of V6 provides an output with the black level clamped, a separate clamp at the input of the clamp pulse derivation chain is preferred so that the signal clamp time constant can be selected independently.

Monitoring Facilities

Three outputs are provided for monitoring purposes. These are in parallel with the input socket, output socket and the grid of V6 respectively. The input and output monitor sockets, designated *Monitor Input* and *Monitor Output* respectively, project through the front panel of the unit. The socket connected to the grid of V6 is designated *Monitor Black Level* and is mounted on the sub-panel carrying the major components of the unit. To avoid mis-matching effects, any monitoring equipment connected at these points should have a high input impedance.

Metering

The anode current feeds for all stages except V6 can be measured by means of the internal meter mounted on the front panel. Full-scale deflection occurs for a current of 1 mA, and the meter is scaled 0-50. By means of its selector switch the meter can be connected in parallel with any of the metering resistors. The meter resistance is built out to 500 ohms, so that full-scale deflection normally corresponds to a current of 50 mA in the circuit being checked. When the meter is connected in parallel with R27, the current indicated comprises the anode current of V6 and the current of the two associated bleeder chains.

Mechanical Construction

The unit is mounted on a 19 in. × 10½ in. panel suitable for bay mounting. When so mounted it projects through the bay. Behind the front panel, and at a distance of 5 in. from it, is a sub-panel secured to side panels attached to the front panel. On the sub-panel are mounted the amplifier valves and components. The amplifier is enclosed by a cover which is detached from the rear and located when in place by the side panels. The cover width at the rear is less than the full width of the amplifier, to expose the input, output, and power supply plugs.

Access to the valves and pre-set controls from the front of the unit is through a detachable plate secured to the front panel. The plate is fitted with a handle, and is held in place by the pressure of spring mountings on two fasteners at the top and bottom centre of the plate. Additionally, handles are attached to the front panel to assist removal and replacement of the amplifier. The general layout of the unit can be seen in Plates I and II.

General Data

Feed Meter
Weston Type S33 1 mA F.S.D. scaled 0-50.

Input, Output and Monitor Plugs
P.O. Coaxial Plug No. 1.

Impedances
Input : Z = 75 ohms resistive.
Output : Z = 75 ohms resistive.

Normal Working Levels
Input : 1 volt d.a.p.
Output : 1 volt d.a.p.

Power Consumption
H.T. : 170 mA at 300 volts.
L.T. : 2·8 A at 6·3 volts and 2·3 A at 6·3 volts.
Power supply normally obtained from stabilised power-supply unit SPS/4 or SPS/7.

Valve Data

All readings taken with no signal input.

Valve	Anode Current Panel Meter Reading	Anode Voltage* reading	Screen Voltage* reading	Cathode Voltage** reading
V1 CV138	6	140 (120)	205 (175)	2·0 (1·9)
V2 CV138	6	140 (120)	205 (120)	2·0 (1·9)
V3 CV138	6	140 (120)	205 (175)	2·0 (1·9)
V4 6F14	16	180 (175)	170 (160)	8·1 (8·0)
V5 6F14	22	220 (220)	220 (220)	65 (65)***
V6 CV138	26	285 (280)	300 (300)	5·7 (4·7)***
V7 EF55	39	165 (160)	300 (300)	22 (21)***
V8 CV138	2	200 (175)	220 (175)	15·0 (10·0)***
V9 CV858	8	(a) 40 (26)	—	0
		(b) 100 (90)	—	0
V10 CV858	11	(a) 70 (70)	—	0
		(b) 100 (100)	—	0
V11 CV140	—			
V12 CV858	11	(a) 70 (70)	—	0
		(b) 100 (100)	—	0
V13 CV140	—			

*Measured with AVO Model 7 on 480 V range; figures in brackets AVO Model 40, 400 V range.
**Measured with AVO Model 7 on 12 V range; figures in brackets AVO Model 40, 10 V range.
***Measured with AVO Model 7, on 120 V range; figures in brackets, AVO Model 40, 100 V range.
Tolerance on all readings, ± 20 per cent.

Lining-up Instructions (TV/STA/2)

1. Switch on power supplies, and allow ten minutes to elapse for unit to warm up.
2. Check that h.t. voltage is 300, and that all valve feeds are in accordance with the values given in the Valve Data section.
3. Set all the equaliser switches to OUT, and check that the amplifier output is terminated in 75 ohms.
4. Apply a 1 V d.a.p. signal consisting of 0·3 V sync and 0·7 V line saw-tooth; adjust the *Gain* control to give a signal of 6·5 V d.a.p. sync and 15 V picture at the *Monitor Black Level* plug, measured with a high impedance waveform monitor (*Open Grid* input of TV/WM/1).
5. Transfer the waveform monitor to the output and check that the output signal is 1±0·1V d.a.p. Adjust the *Gain* control so that the output falls by 6 db. Adjust the *Crystal Bias* control until the sync-pulse amplitude reaches maximum. Note setting of control.
6. Advance the *Crystal Bias* control until the black-level amplitude changes. Note setting of control.
7. Set *Crystal Bias* control to position midway between the positions found in 5 and 6 above. Restore the output to normal level.
8. Set the sync-pulse amplitude to that desired by means of the *Sync Pulse Amp.* control. If the amplitude required cannot be obtained it may be necessary to adjust the *Set Sync Range* control, as described in the test specification.
9. Set the *Clamp Time Constant* to give the best compromise between the removal of low-frequency distortion and spurious clamping by noise pulses.

Test Specification (TV/STA/2)

The apparatus required comprises:—

1 Video-frequency Oscillator, 100 kc/s-4 Mc/s.
1 Moullin Valve Voltmeter or other similar voltmeter.
1 Avometer (Model 7 or 40).
1 Television Waveform Monitor TV/WM/1.
1 Television Test Generator TV/TG/1.

During all tests, except where otherwise specified, the output of the unit should be terminated in a 75-ohm load. In the following tests voltages are given in d.a.p.; the corresponding approximate r.m.s. figures for sinusoidal waveforms are given in brackets.

1. With all equalisers set to the *Out* position the input and output impedances measured at d.c. should be 75 ohms ±3 per cent.
2. Switch on power supplies and allow ten minutes to elapse for unit to warm up.
3. Check that the h.t. voltage is 300, and that the valve feeds are as given in the Valve Data section.
4. Set the *Gain* control to maximum, switch S7 to CLAMP OUT and apply a signal at 100 kc/s from the video-frequency oscillator of amplitude 0·5V (175 mV). Measure the signal amplitude at the cathode of V5. This should be 21·5±2·0 V (7·7±0·8 V). Repeat at frequencies of 500 kc/s, 1 Mc/s, 2 Mc/s and 3 Mc/s; the output at these frequencies should be within 2 per cent of that at 100 kc/s. If necessary adjust the cores of L1, L2, L3 and L5 to achieve this; the major control is obtained by varying L3.
5. A television signal from the TV/TG/1 comprising sync pulses and lift without frame pulses at 1 V amplitude, should now be applied to the input. Connect the waveform monitor *D.C.* input to *Monitor Black Level* plug and set the waveform monitor input selector switch to OPEN GRID. Adjust *Gain* control until the signal amplitude is 21·5 V. Restore switch S7 to CLAMP IN.
6. By means of the waveform monitor, examine the clamping pulses at the diodes V11 and V13. The amplitudes of these pulses should be greater than 32 V and the shape and duration should be as shown in Fig. B.6. If these pulses are not in accordance with the figure, the waveforms at the various points in the chain of valves V8-V13 should be checked. If the duration of the pulses at the grid of V10(a) is not within the range 4·5±0·5 microseconds, C23 should be adjusted. If the value of C23 necessary to achieve this lies outside the range 33-68 pF, the crystal diode G3 should be suspected.
7. With the waveform monitor set to *Open Grid* and connected to the *Monitor Black Level* plug, set the *Adjust Black Level* control so that the black level is at a potential of +1 V with respect to earth. Vary the *Gain* control setting so that the signal amplitude varies over the range 8·5 V to 34 V; check that the black-level voltage does not change by more than 0·2 V. Restore *Gain* control to give signal amplitude of 21·5 V.
8. Transfer the waveform monitor to the *Monitor Output* plug; check that the picture signal amplitude is 0·7±0·1 V. Reduce the output picture signal amplitude to 0·28 V and adjust the *Crystal Bias* control until the sync-pulse amplitude reaches its maximum value; note position of control. Advance the control further until the black-level amplitude changes; note position of control. Set the control to the position midway between the two positions found above.
9. Adjust the input signal amplitude so that the output picture signal amplitude is 0·7 V. Set *Sync Pulse Amplitude* control to its minimum setting and adjust *Set Sync Range* control so that the sync-pulse amplitude is 0·28 V.
10. Set the *Sync Pulse Amplitude* control to maximum and check that the sync-pulse amplitude is 0·38±0·02 V. Check that at no setting of the control is the picture waveform affected. Set *Sync Pulse Amplitude* control so that the output sync-pulse amplitude is 0·3 V.
11. Connect the output of the video-frequency oscillator to the external signal input of the TV/TG/1. Set the TV/TG/1 control to EXT. SIG. AMP. Set *Ext Sig Level* control to 100 and adjust input signal amplitude until the *Ext Sig Level* meter reads 50.
12. Set the oscillator frequency to 100 kc/s and measure the amplitude of the input signal to the TV/STA/2. If the amplitude is measured by a valve voltmeter, calibrated in r.m.s. values for sinusoidal input, the meter reading should be 0·25 V. Transfer the valve voltmeter to the *Monitor Output* socket and note reading.
13. Repeat 12 above at oscillator frequencies of 500 kc/s, 1 Mc/s, 2 Mc/s and 3 Mc/s, adjusting L4 if necessary to achieve a frequency response flat to within 2 per cent up to 3 Mc/s.

N.B.—The reading of the valve voltmeter is influenced by the presence of the sync pulses in both the input and output signals and hence does not give the true value of the amplitude of the sinusoidal component.

Further, the ratio of the output signal amplitude to the input signal amplitude is not a true indication of gain since the picture/sync ratio at the output differs from that at the input. Provided, however, that the readings of the output voltage in (13) above do not differ by more than 3 per cent from that in (12) above, the percentage differences may be regarded as equal to the change of gain with sufficient accuracy.

14. Apply a *Spike 1* waveform from the TV/TG/1, and check the time of rise of the output signal. This should not exceed 0·16 microseconds; the overshoot should not exceed 6 per cent.

15. Apply a *Frame 1* waveform with frame-sync pulses from the TV/TG/1 to the input. With *Clamp Time Constant* set to its minimum value, check that the sync-pulse amplitude at the output is constant and undistorted when the output picture signal amplitude is decreased to 0·35 V or increased to 1·1 V; Insert a 16 μF-capacitor in series with the input and observe that the output waveform suffers little or no distortion.

16. With an input signal comprising sync pulses and line saw-tooths, check that the output picture signal amplitude when limiting commences is greater than 1·2 V.

17. Measure the input resistance at d.c. and throw equaliser switches to IN in succession. Check that the value remains at 75 ohms ±3 per cent. If possible, measure the input impedance at 3 Mc/s. At all settings of the equaliser switches the magnitude of the input impedance should be 75 ohms ±4 per cent, and the phase angle of the impedance should be 0±10 degrees.

18. Connect the output of the video-frequency oscillator to the amplifier input, Set *Gain* control to minimum setting and connect the valve voltmeter across R1; with an input level of 3·2 V (1·0 V), check that the frequency responses of the various equaliser sections are as set out in the table below; the maximum error should not exceed 0·25 db.

Frequency	200-*ft.* *Equaliser*	400-*ft.* *Equaliser*	600-*ft.* *Equaliser*	1,000-ft. *Equaliser*	
				Section 1	*Section* 2
	db	db	db	db	db
10 kc/s	1	2	3	2	4
100	1	2	2·9	1·8	4
300	0·8	1·8	2·6	0·9	4
500	0·7	1·6	2·4	0·5	3·8
700	0·6	1·4	2·1	0·3	3·7
1 Mc/s	0·6	1	1·8	0·1	3·4
1·5	0·5	0·6	1·1	0	2·9
2	0·3	0·4	0·8	0	2·3
3	0·1	0·2	0·4	0	1·5
4	0	0·1			

TV/PSTA/1

The TV/PSTA/1 is a portable version of the TV/STA/2, incorporating a mains unit. The circuit details and performance of the amplifier are almost identical with those of the TV/STA/2, and reference should be made to the preceding portion of this Instruction for these. A circuit diagram of the unit is shown in Fig. 3; from this it will be seen that the only difference between the TV/PSTA/1 and the TV/STA/2 is the omission in the former of the capacitor C45 at the grid of V5. The reason for this omission is the higher stray capacitance existing in the TV/PSTA/1 due to the different layout. The h.t. and l.t. supply arrangements differ in that the supply connections are permanently made in the TV/PSTA/1; the l.t. supply is from a heater transformer in the amplifier sub-chassis, fed at 180 V from the mains transformer on the mains unit sub-chassis.

The circuit diagram of the mains unit is shown in Fig. 4. The mains transformer is designed to operate from a wide range of input voltages (180-240); its primary winding is used as an auto-transformer to feed the heater transformer at 180 volts. Additionally a supply at 115 volts is tapped off for the cooling fan.

The h.t. supply is stabilised by a circuit of conventional design, achieved by the action of the valves V3, V4 and V5. V3 is a double triode the two halves being connected in parallel; it acts as a cathode follower, the external circuit comprising its cathode load. The output voltage is slightly higher than the valve grid-earth voltage, and this latter voltage is that of the anode of V4. This valve is an amplifying stage, having a stabilised cathode potential; its grid is fed from the potential divider chain R12, R14 and R13 across the h.t. output. Any change in this output is, therefore, amplified and communicated to the grid of V3 in a sense such as to oppose the change occurring. The input to the grid of V4 is necessarily positive with respect to earth; consequently the cathode of V4 must be at a positive potential. The cathode potential is stabilised for two reasons:

1. If a cathode resistor were employed, a high degree of negative current-feedback would exist, reducing the amplifier gain.

2. The circuit operates by variation of the grid-cathode potential of V4 and any change in V4 cathode potential would alter the value of the stabilised output in the same way as a change of grid potential. The performance of the stabilising section is therefore critically dependent on the performance of V5.

The h.t. voltage can be varied within limits by adjustment of the *Set 300 V* control R14. This adjusts the quiescent grid potential of V4 and hence the anode potential of V.4.

Capacitor C5 is included to reduce the higher order components of the ripple output. C45 provides a low impedance to the grid of V4 for these components, which are amplified by V11; the output voltage thus varies in such a way as to minimise their amplitude. The value of C5 represents a compromise; if too large a value is chosen, the circuit tends to overshoot in correcting changes in output voltage.

For a more detailed discussion of the technique of voltage stabilisation, reference should be made to Technical Instruction V.4.

Mechanical Construction

The unit is mounted in a carrying case of overall dimensions 23 × 12 × 10 in; this case is of the standard type employed in Pye OB equipment. The ON/OFF switch, fuses, mains selector switch feed meter and its associated switch are mounted on the front panel of the unit, as shown in Plate III. The mains input plug together with the signal and monitor coaxial plugs are mounted on the rear panel of the unit, as shown in Plate IV. The signal and monitor plugs differ from those used in the TV/STA/2; in the former they are of F. and E. Type SO/239, whilst the latter are of Type P.O. Coaxial No. 1 (*Musa* plugs). The cooling fan, which extracts warm air from the interior of the unit, is fitted through the rear panel.

The side panels of the case are held by quick-release fasteners, and when removed, give access to the sub-chassis carrying the mains unit (on left, viewed from front) and the amplifier (on right, viewed from front). The interior of the unit with the side panels removed is shown in Plates V and VI. The two chassis are mounted in the vertical plane, back to back. The amplifier chassis is carried at the bottom by two hinged plates; two captive bolts normally retain the chassis in its vertically mounted position. When these are released, the chassis can be swung downwards to give access to the underside of the chassis (see Plate VII).

TV/STA/2A

The TV/STA/2A is basically similar to the TV/STA/2, and differs principally in that the output stages have been modified to provide the correct picture/sync ratio and the high-level signal necessary to drive the low-power television transmitters with which the amplifier is employed. The TV/STA/2A accepts a standard 1 volt d.a.p. television signal of picture/sync ratio 70/30, and produces at its output a 32 volt d.a.p. signal with a picture/sync ratio variable between 60 : 40 and 45 : 55; the normally employed ratio is 50 : 50. The output sync bottom voltage is held constant, and the amplitude of the sync pulses does not vary appreciably over a range of input signal variations of −6 to +4 db relative to 1 volt d.a.p. Additionally, low-frequency distortion and hum are greatly reduced by the action of the black-level clamp. The amplitude of the sync pulses at the output can be set independently of the amplitude of the picture signal.

Circuit Description

The circuit diagram of the unit is shown in Fig. 5 from which it will be seen that the circuit is identical with that of the TV/STA/2 in the clamp pulse derivation chain and in the main chain up to valve V6, with the exception of the omission of the switch S7 which, in the TV/STA/2, removed the black-level clamping action. Reference should therefore be made to the early part of this Instruction for details of the operation of these portions of the circuit.

In the anode circuit of V6 the values of the resistors in the bleeder chain feeding the crystal diode G4 have been altered, R119 and R118 replacing R26 and R80. The chief result of the change is that the amplification afforded to the picture, which is determined by the parallel combination of resistors R119 and R25 (2.1 kilohms), is appreciably lower than that in the TV/STA/2. The overall effect is to enhance the sync-pulse output amplitude relative to that of the picture, so that the desired range of picture/sync ratios may be achieved.

The valve V7, operated in the TV/STA/2 with a low-value anode load as the output stage, is here utilised as an amplifier to drive the output cathode follower V14. The output impedance of V14 is given by $1/g_m$ (75 ohms approximately), where g_m is the mutual conductance of the valve. The external load must, however, be of high impedance because the valve is not capable of supplying to a matched load the necessary current swing, to follow the input voltage.

The output black-level voltage is determined by the setting of the potentiometer R112 and the action of the d.c. restoring diode V15, which determines the quiescent bias of V14, and hence the corresponding value of quiescent cathode potential. The setting of R112 determines the voltage corresponding to sync bottom, as V15 serves to clamp the tips of the sync pulses at this voltage. Because the amplitude of the sync pulses is stabilised, the black-level voltage at the grid of V14, being equal to the sum of the voltage at the slider of R112 and the sync-pulse amplitude, is also constant.

Lining-up Instructions (TV/STA/2A)

The lining-up instructions for the TV/STA/2A are identical with those for the TV/STA/2 with the exception of paras. 5-9 which should be replaced by :—

5. Transfer the waveform monitor to the output and check that the output signal is 32±3 V d.a.p. Adjust the *Gain* control so that the output falls by 6 db. Adjust the *Crystal Bias* control until the sync-pulse amplitude reaches maximum. Note setting of control.
6. Advance the *Crystal Bias* control until the black-level amplitude changes. Note setting of control.
7. Set *Crystal Bias* control to position midway between the positions found in 5 and 6 above. Restore the output to normal level.
8. Set the sync-pulse amplitude to the desired value, normally 16 V d.a.p. If the amplitude required cannot be obtained, it may be necessary to adjust the *Set Sync Range* control as described in the Test Specification.
9. Adjust R112 to give the required value of black level, normally +32 V.
10. Adjust *Gain* control if necessary to obtain required output picture amplitude. The alteration of the *Gain* control setting should not be large and the sync-pulse amplitude should remain unchanged.
11. Set the *Clamp Time Constant* to give the best compromise between the removal of low-frequency distortion and spurious clamping by noise pulses.

Test Specification (TV/STA/2A)

The apparatus required comprises :—

1 Video-frequency Oscillator 100 kc/s-4 Mc/s
1 Moullin Valve Voltmeter or other similar voltmeter
1 Avometer (Model 7 or 40)
1 Television Waveform Monitor TV/WM/1
1 Television Test Generator TV/TG/1.

During all tests the main output of the unit should be terminated in a high impedance.. In the following tests voltages are given in d.a.p. ; the corresponding approximate r.m.s. figures for sinusoidal waveforms are given in brackets. The noise limiter should be out of circuit for the duration of these tests.

1. With all equalisers set to the *Out* position the input impedance measured at d.c. should be 75 ohms ±3 per cent.
2. Switch on power supplies and allow ten minutes for unit to warm up.
3. Check that the h.t. voltage is 300 and that the valve feeds are as given in the Valve Data section. The voltage at the anode and screen of V14 should be 295, and at the cathode 16 ; the voltage at the anode of V15

should be 6·7 and at the cathode 6·4.

4. The output impedance measured at d.c. at the *Monitor Output* plug should be 75 ohms ±5 per cent.
5. Set the *Gain* control to maximum and apply a signal at 100 kc/s from the video-frequency oscillator of amplitude 0·5 V (175 mV). Measure the signal amplitude at the cathode of V5; this should be 21·5±2 V (7·7±0·8V.) Repeat at frequencies of 500 kc/s, 1 Mc/s, 2 Mc/s and 3 Mc/s; the output at these frequencies should be within 2 per cent of that at 100 kc/s. If necessary adjust the cores of L1, L2, and L3 and L5 to achieve this; the major control is obtained by varying L3.
6. A television signal, comprising sync pulses and lift without frame pulses, from the TV/TG/1, should now be applied to the input at 1 V amplitude. Connect the waveform monitor *D.C.* input to *Monitor Black Level* plug and set the waveform monitor input selector switch to OPEN GRID. Adjust *Gain* control until the signal amplitude is 21·5 V.
7. By means of the waveform monitor examine the clamping pulses at the diodes V11 and V13; the amplitudes of these pulses should be greater than 32 V and the shape and duration should be as shown in Fig. 2.6. If these pulses do not accord with those shown in the figure, the waveforms at the various points in the chain of valves V8-V13 should be checked. If the duration of the pulses at the grid of V10(a) is not within the range 4·5±0·5 microseconds, C23 should be adjusted. If the value of C23 necessary to achieve this lies outside the range 33-68 pF, the crystal diode G3 should be suspected.
8. With the waveform monitor set to *Open Grid* and connected to the *Monitor Black Level* plug, set the *Adjust Black Level* control so that the black level is at a potential of +1 V with respect to earth. Vary the *Gain* control setting so that the signal amplitude varies over the range 8·5 V to 34 V; check that the black-level voltage does not change by more than 0·2 V. Restore *Gain* control to give signal amplitude of 21·5 V.
9. Transfer the waveform monitor to the *Output* plug; check that the picture signal amplitude is 16±1 V. Reduce the output picture-signal amplitude to 6·5 V, and adjust the *Crystal Bias* control until the sync-pulse amplitude reaches its maximum value; note position of control. Advance the control further until the black-level amplitude changes; note position of control. Set the control to midway between the two positions found above.
10. Adjust the output picture signal amplitude to 16 V. Set *Sync-Pulse Amplitude* control to its maximum setting and adjust *Set Sync Range* control so that the sync pulse amplitude is 20 V.
11. Set the *Sync Pulse Amplitude* control to minimum and check that the sync-pulse amplitude is 10±2 V. Check that at no setting of the control is the picture waveform affected.
12. Set the *Sync Pulse Amplitude* control so that the output signal sync-pulse amplitude is 16 V. Check that the potential of the sync bottom can be varied between the limits +10 and +22 V with respect to earth by means of the control. Set the output black level at +32 V with respect to earth. These measurements should be made using the *Open Grid* position of the TV/WM/1.
13. Terminate *Monitor Output* plug in 75 ohms and check that the main output amplitude does not change by more than 3 per cent. Check that the output measured at the *Monitor Output* plug terminated in 75 ohms is 1±0·03 V and that the black level is at +1±0·03 V with respect to earth.
14. Connect the output of the video-frequency oscillator to the external signal input of the TV/TG/1. Set the TV/TG/1 *Ext Sig Level* control to 100, and adjust oscillator output so that *Ext Sig Level* meter reads 50.
15. Set the oscillator frequency to 100 kc/s and measure the amplitude of the input signal to the TV/STA/2A. If this is done by means of a valve voltmeter calibrated in r.m.s. values for sinusoidal inputs, the meter reading should be 0·25 V. Transfer the valve voltmeter to the *Monitor Output* socket and note reading.
16. Repeat 15 above at oscillator frequencies of 500 kc/s, 1 Mc/s, 2 Mc/s and 3 Mc/s, adjusting L4 if necessary to achieve a frequency response flat to within 2 per cent up to 3 Mc/s. *N.B.*—The reading of the valve voltmeter is influenced by the presence of the sync pulses in both the input and output signals and

hence does not give the true value of the amplitude of the sinusoidal component. Further, the ratio of the output signal amplitude to the input signal amplitude is not a true indication of gain since the picture/sync ratio at the output differs from that at the input. Provided, however, that the readings of the output voltage in 16 above do not differ by more than 3 per cent from that in 15 above, the percentage differences may be regarded as equal to the change of gain with sufficient accuracy.

17. Apply a *Spike 1* waveform from the TV/TG/1, and check the time of rise of the output signal. This should not exceed 0·16 microseconds; the overshoot should not exceed 6 per cent.

18. Apply a *Frame 1* waveform with frame-sync pulses from the TV/TG/1 to the input. With the *Clamp Time Constant* set to its minimum value, check that the sync-pulse amplitude at the output is constant and undistorted when the output picture-signal amplitude is decreased to 6·5 V or increased to 25 V; check also that the black-level voltage does not change by more than 3·2 V. Insert a 16 μF-capacitor in series with the input and observe that the output waveform suffers little or no distortion.

19. With an input signal comprising sync pulses and line saw-tooths, check that the output picture amplitude when limiting commences exceeds 32 V.

20. Measure the input resistance at d.c. and throw equaliser switches to IN in succession. Check that the input resistance remains at 75 ohms ±3 per cent. If possible, measure the input impedance at 3 Mc/s. At all settings of the equaliser switches the magnitude of the input impedance should be 75 ohms ±4 per cent and the phase angle of the impedance should be 0±10 degrees.

21. Connect the output of the video-frequency oscillator to the amplifier input and connect the valve voltmeter across R1. With an input level of 3·2 V (1·0 V) check that the frequency responses of the various equaliser sections are as set out in the table below. The maximum error should not exceed 0·25 db.

Frequency	200-*ft.* *Equaliser*	400-*ft.* *Equaliser*	600-*ft.* *Equaliser*	1,000-*ft.* *Equaliser*	
				Section 1	*Section* 2
	db	db	db	db	db
10 kc/s	1	2	3	2	4
100	1	2	2·9	1·8	4
300	0·8	1·8	2·6	0·9	4
500	0·7	1·6	2·4	0·5	3·8
700	0·6	1·4	2·1	0·3	3·7
1 Mc/s	0·6	1	1·8	0·1	3·4
1·5	0·5	0·6	1·1	0	2·9
2	0·3	0·4	0·8	0	2·3
3	0·1	0·2	0·4	0	1·5
4	0	0·1			

Noise Limiter

A limiter of a simple a.c. operated type is fitted in the TV/STA/2A and can be wired into circuit if desired. A similar type of limiter may be fitted to the TV/STA/2 and the TV/PSTA/1.

The limiter comprises a small-value capacitor, C50 (0·005 μF) and a crystal diode G5 connected in series between the anode of V4 and earth. The forward time constant determined by the forward resistance of G5, the anode load R12 and the magnitude of the capacitor, is relatively low and hence the capacitor charges rapidly to the peak value of a repetitive signal. The discharge time constant, determined by the back resistance of the crystal and the magnitude of C50, is large and hence the limiter takes current only on the brightest detail of the picture.

Impulsive interference, which is of very short duration and not repetitive, is unable to alter the charge of C50 appreciably. The circuit, therefore remains of low impedance for the duration of the impulse and limits its amplitude to that of the maximum white amplitude in the picture. In the presence of extremely severe interference the charge of C50 will change and the limiter action will be impaired.

Under normal working conditions the limiter introduces very slight distortion of the picture. With an input signal comprising sync pulses and line saw-tooths, the tips of the saw-tooths will be clipped by the action of the limiter. This action should be confined to the top 5 per cent of the saw-tooth waveform.

TV/STA/2B

The TV/STA/2B differs from the TV/STA/2A only in its modification to give a smaller output signal. For that purpose the V14 cathode circuit is rearranged, with a change in the value of R116 and the introduction of an extra component R120, as shown by the separate diagram in Fig. 5.

The test specification and lining-up instructions for the TV/STA/2A apply to the TV/STA/2B, except that voltages measured at the output socket should be scaled down in the ratio 2 : 1, approximately.

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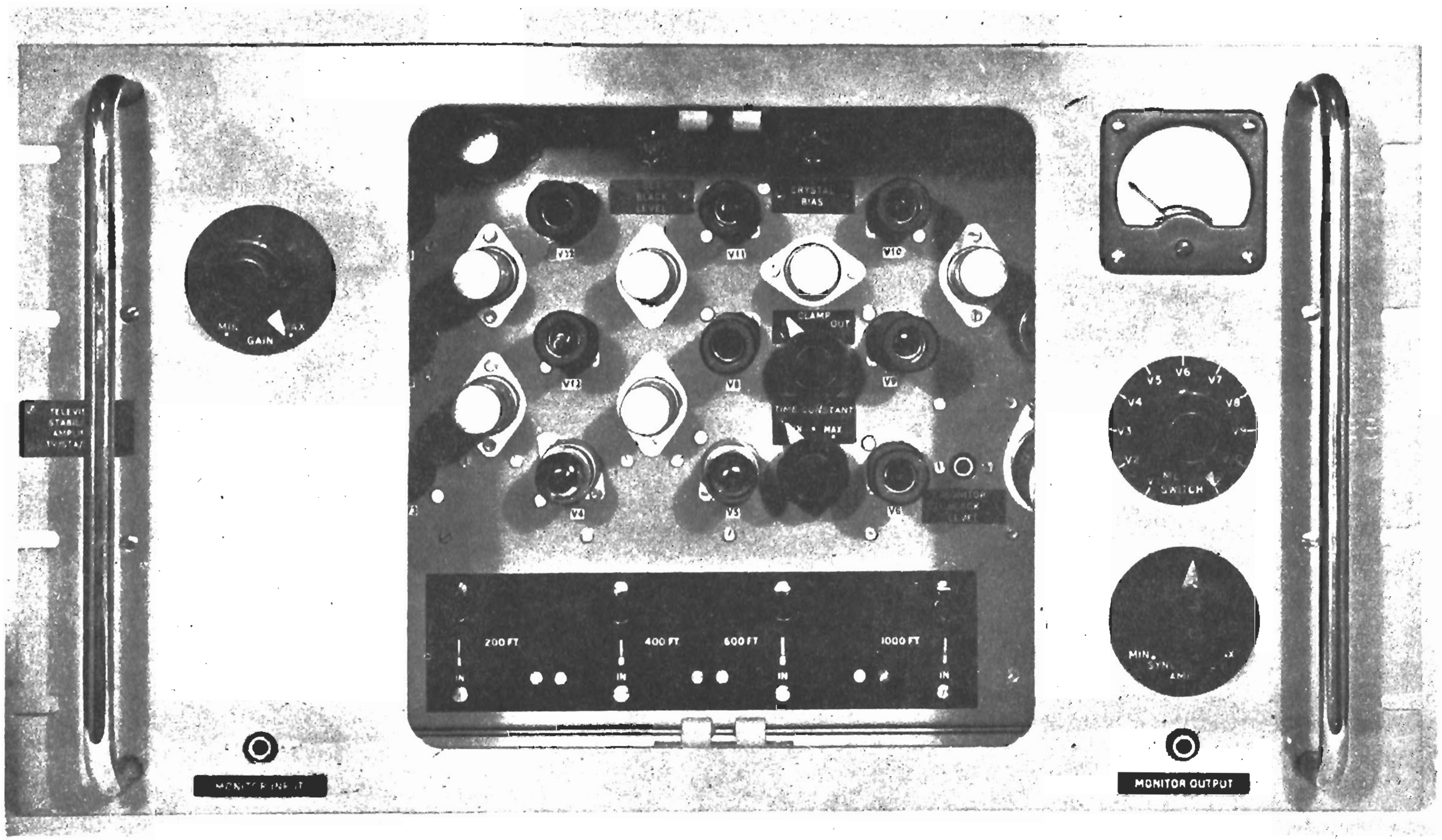

PLATE 1. Television Stabilising Amplifier TV/STA/2. Front View

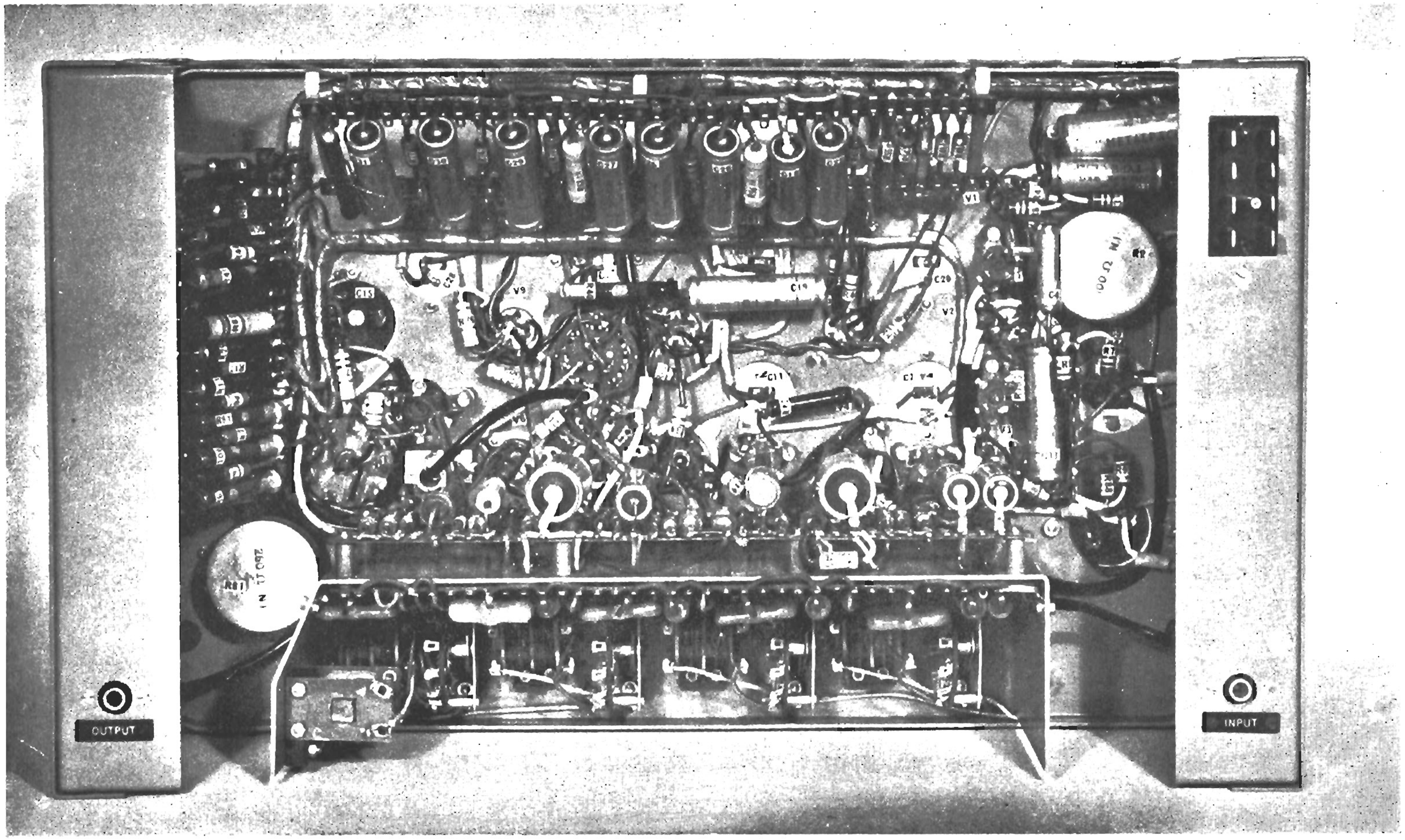

PLATE II. Television Stabilising Amplifier TV/STA/2. Rear View

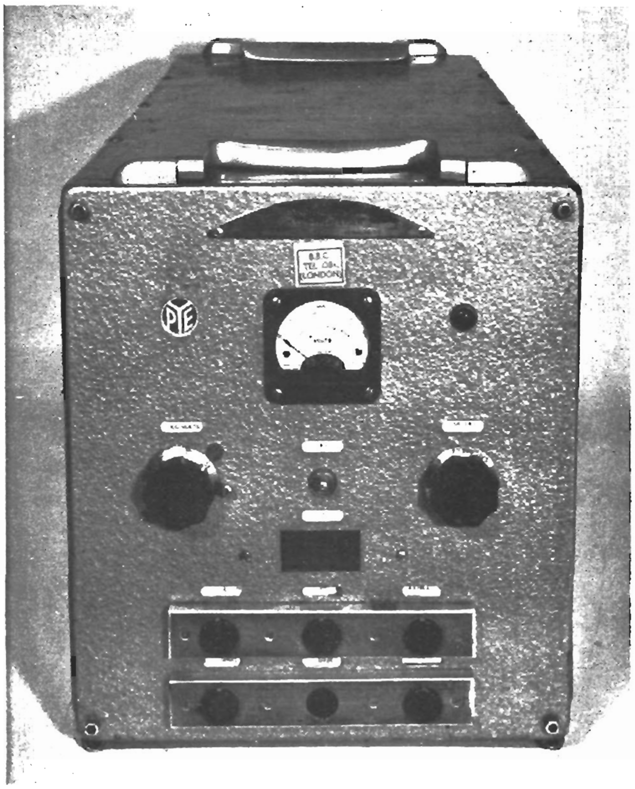

PLATE III. Television Portable Stabilising Amplifier TV PSTA I. Front View

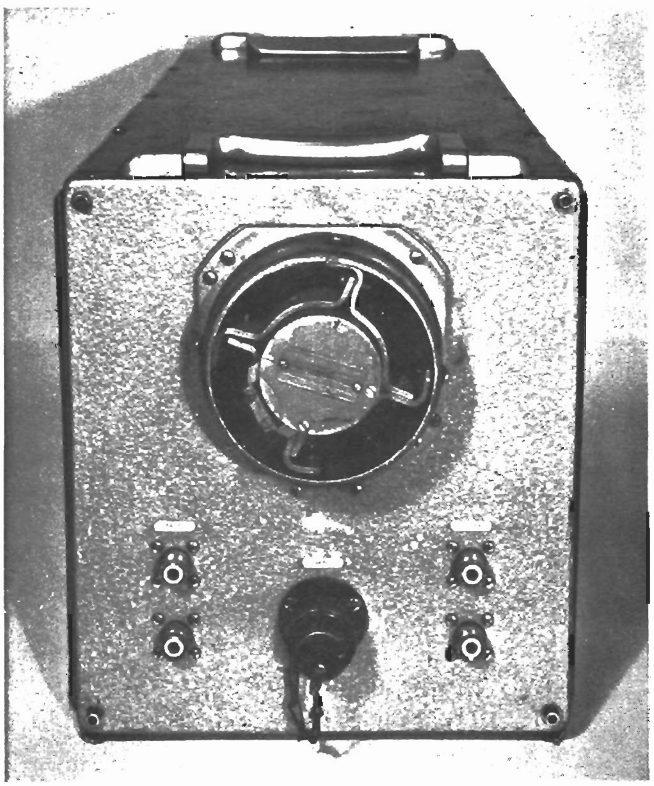

PLATE IV. Television Portable Stabilising Amplifier TV/PSTA/I. Rear View

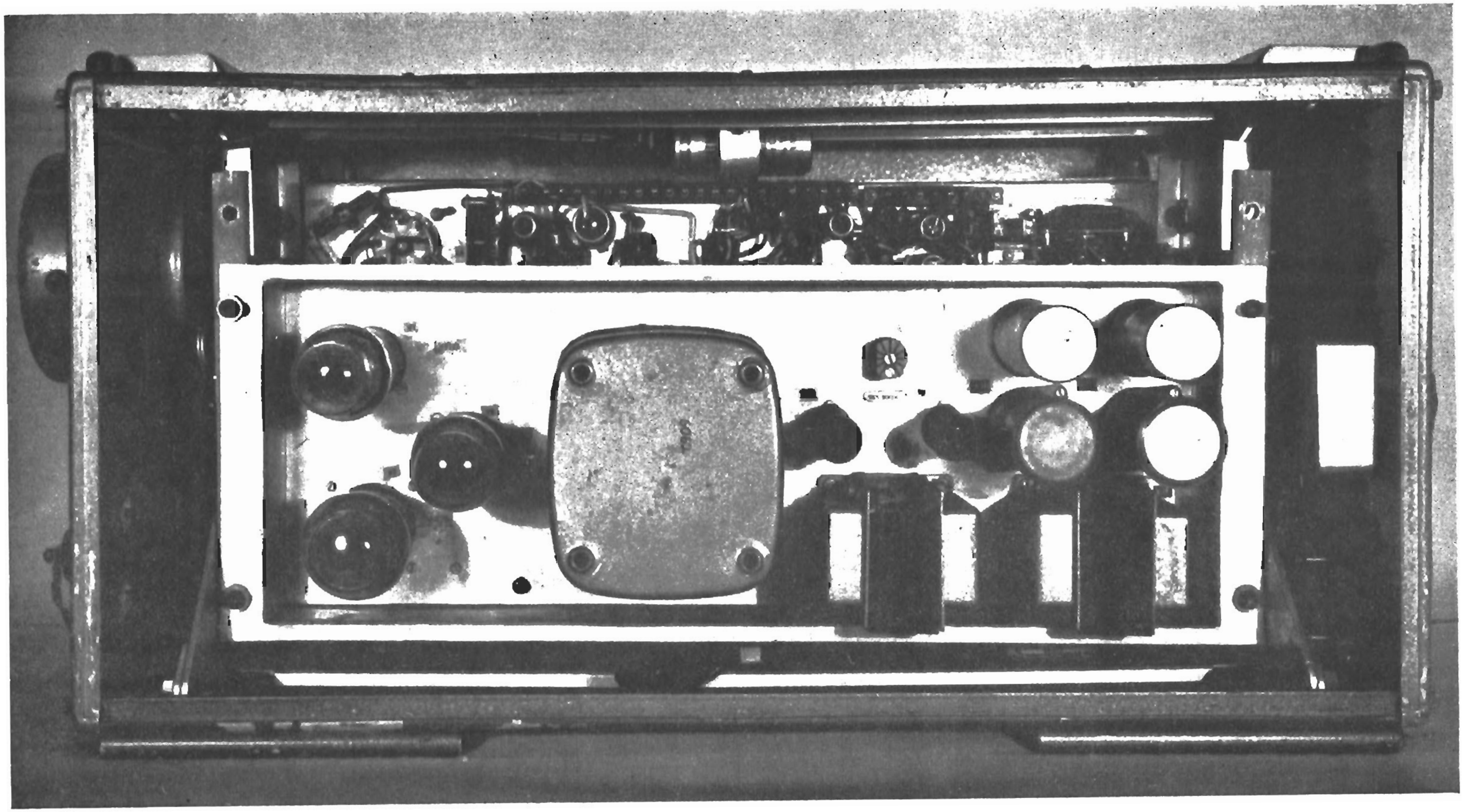

PLATE V. Television Portable Stabilising Amplifier TV/PSTA/1. Side View

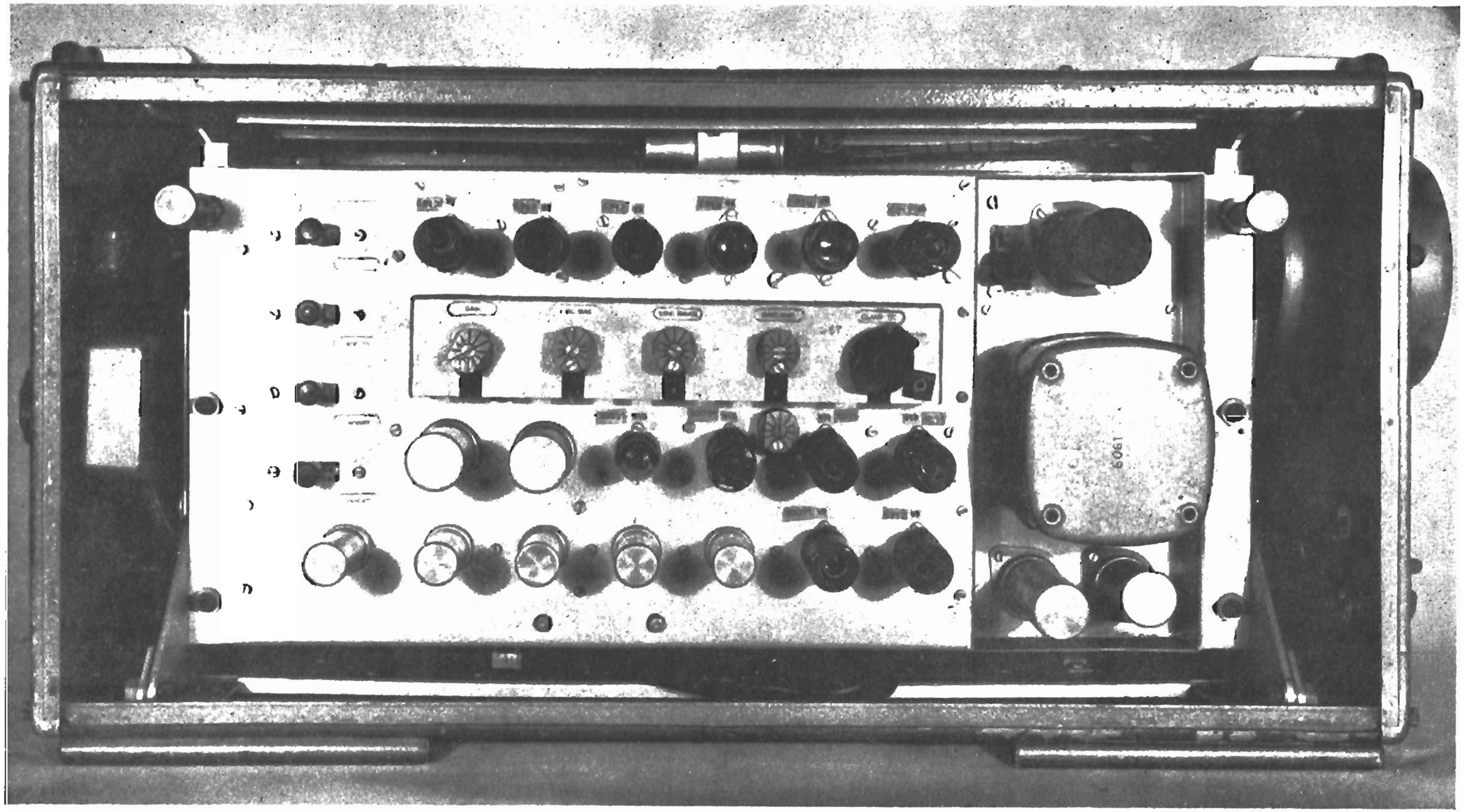

PLATE VI. Television Portable Stabilising Amplifier TV/PSTA/1. Reverse Side View

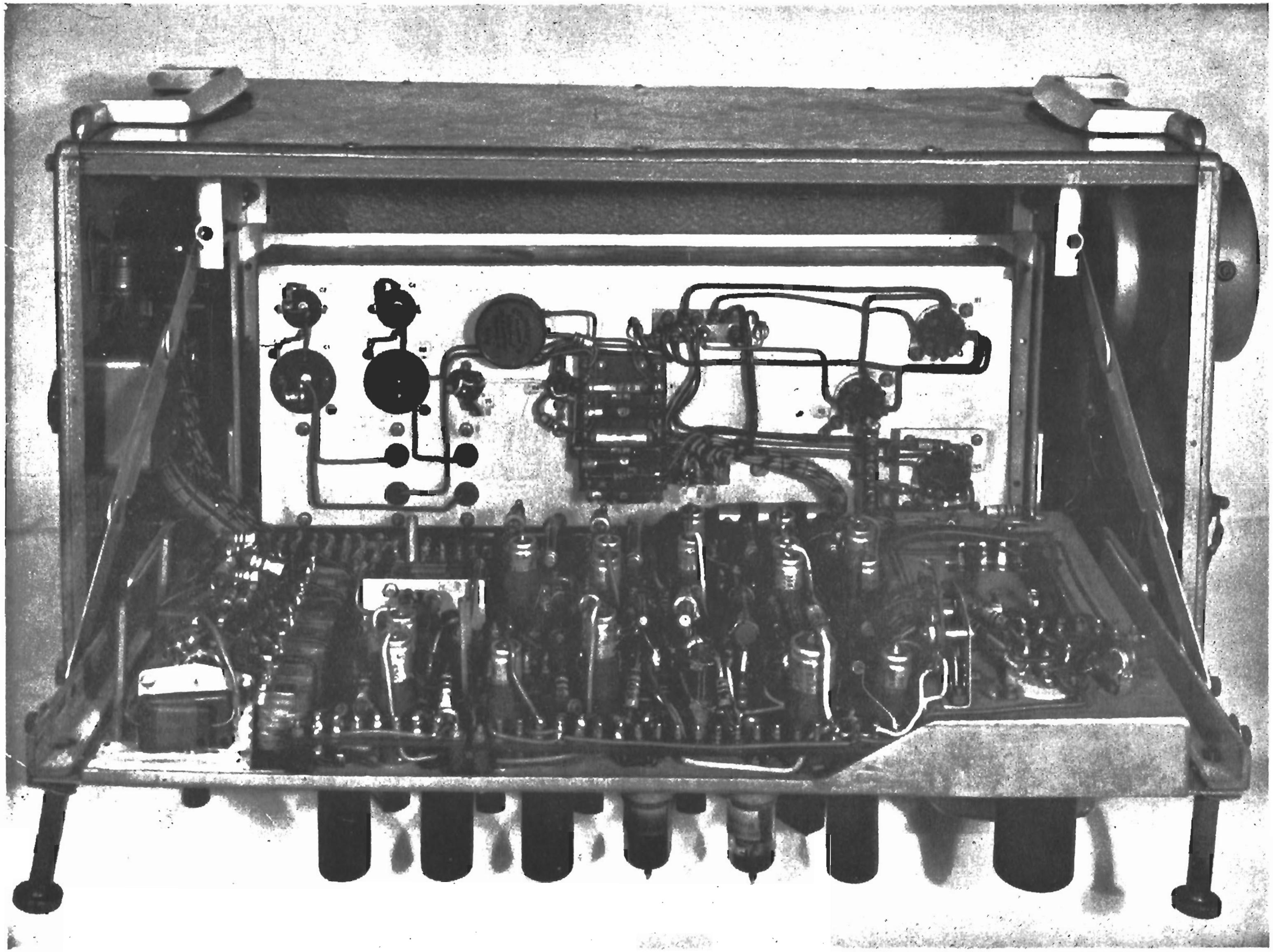

PLATE VII. Television Portable Stabilising Amplifier TV/PSTA/1. As for Plate VI but with Amplifier Chassis lowered into Servicing Position

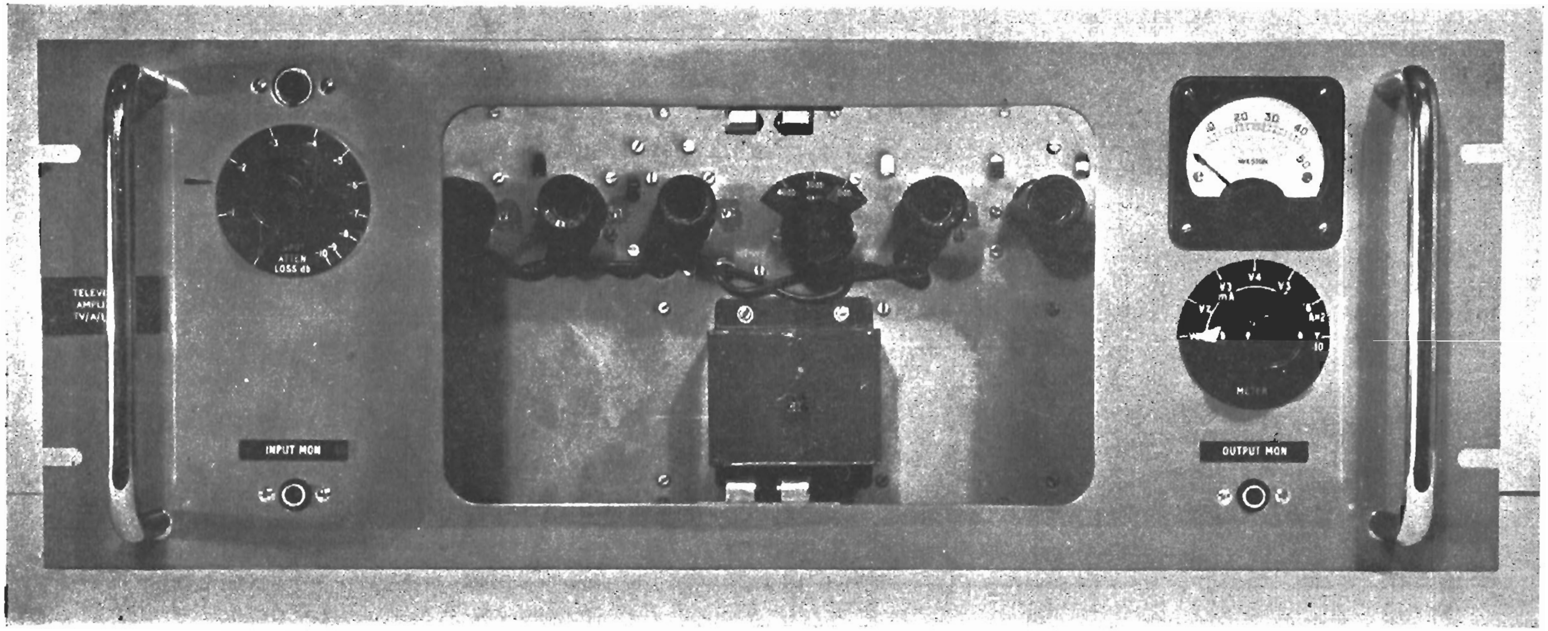

PLATE VIII. Television Amplifier TV/A/1. Front View with Cover Plate removed

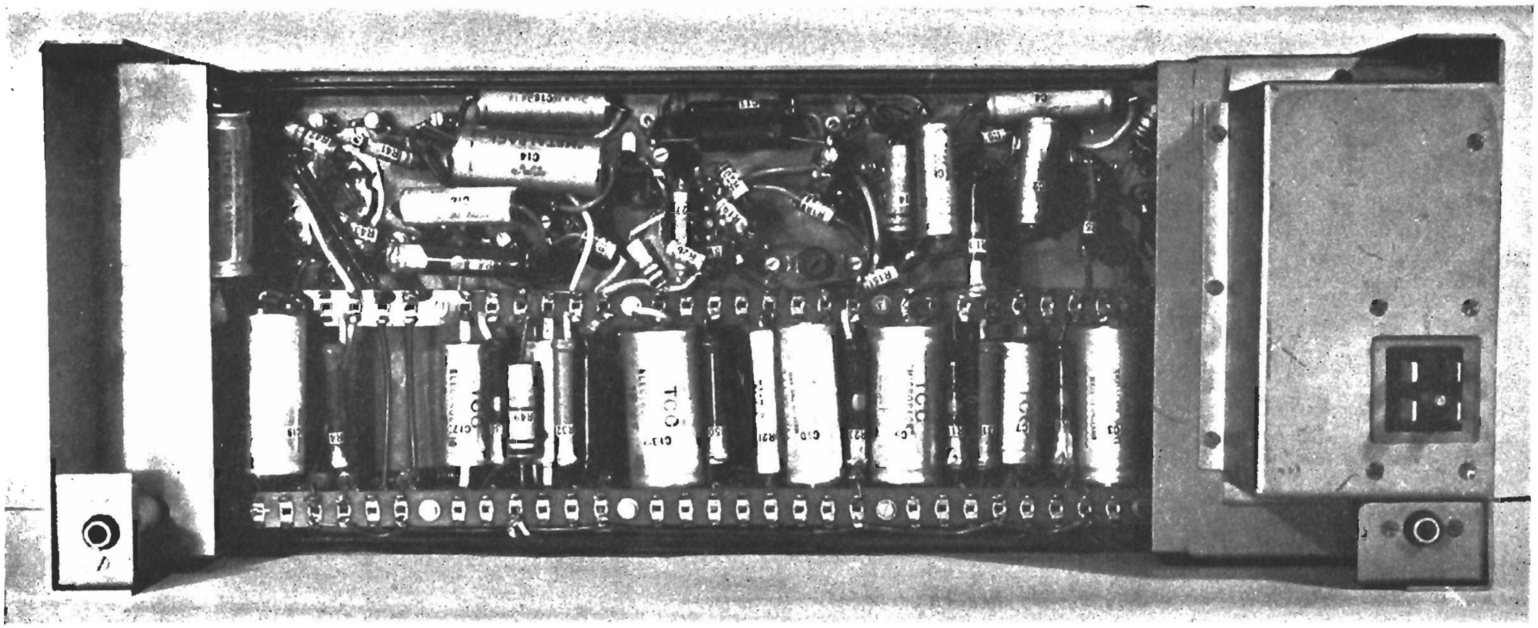

PLATE IX. Television Amplifier TV/A/1. Rear View with Cover removed

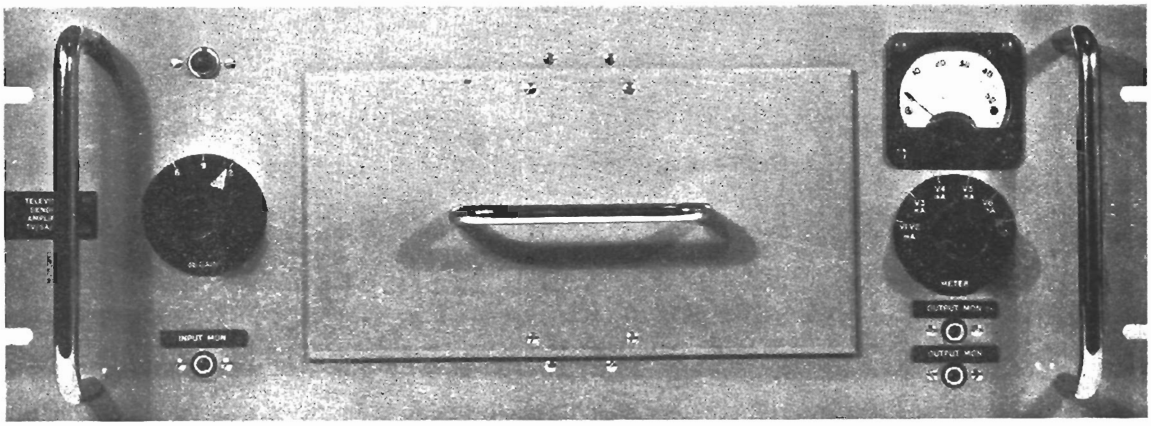

Plate X. Television Sending Amplifier TV/SA/1. Front view.

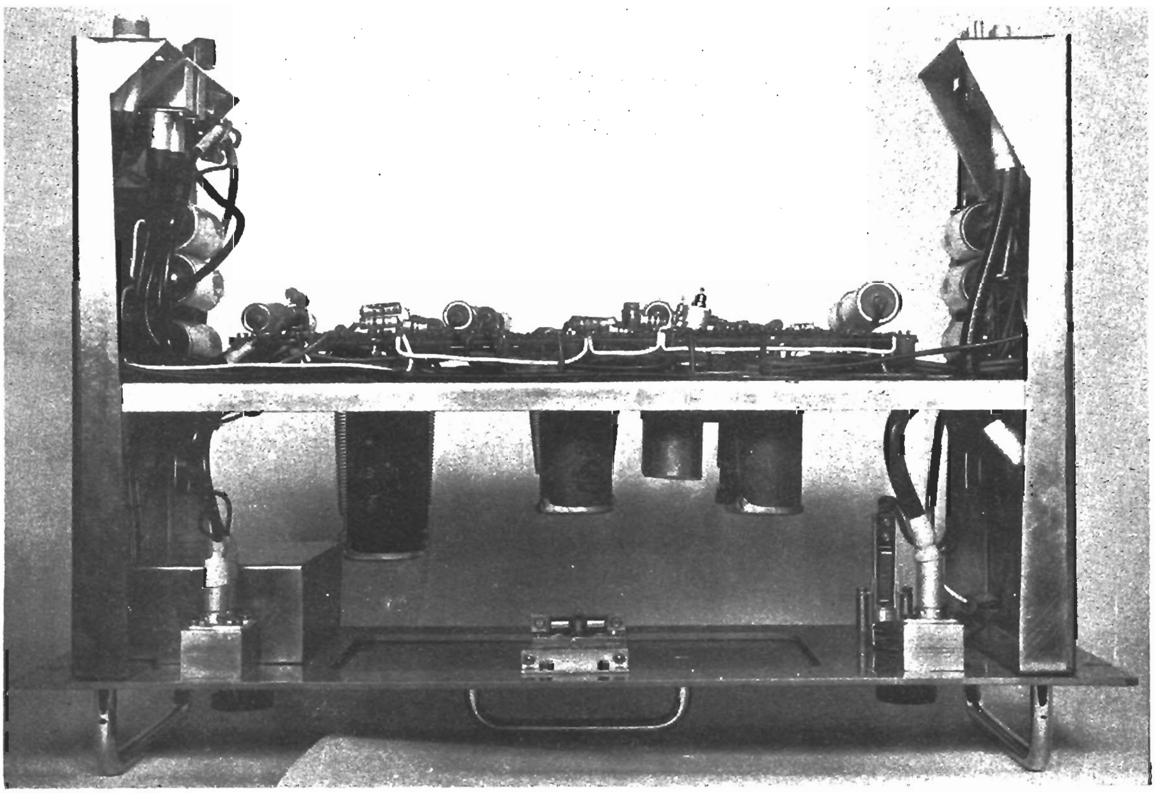

Plate XI. Television Sending Amplifier TV/SA/1. Side view with cover removed.

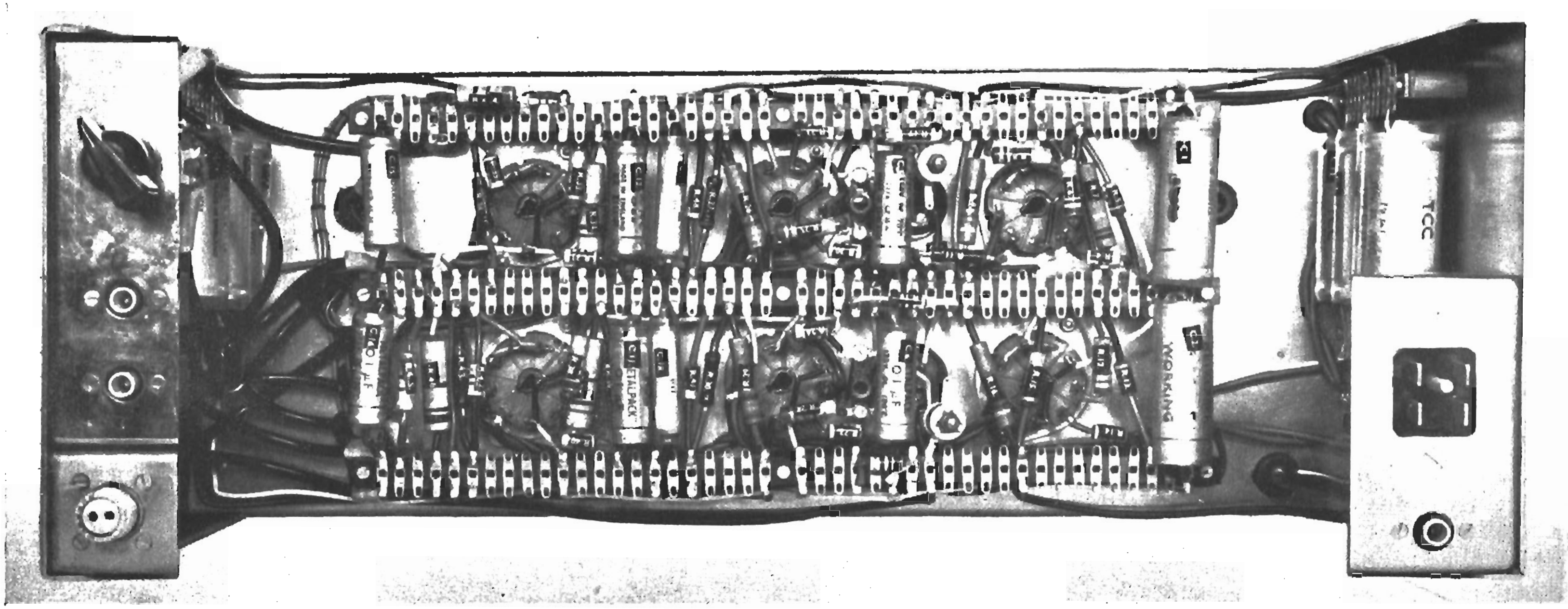

Plate XII. Television Sending Amplifier TV/SA/1. Rear view with cover removed.

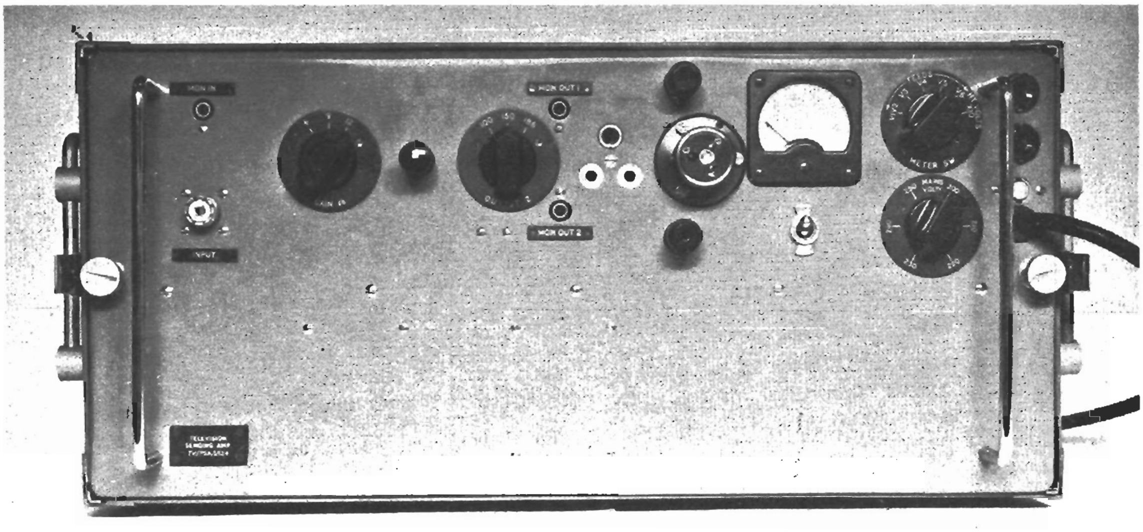

Plate XIII. Television Portable Sending Amplifier TV/PSA/1. Front view

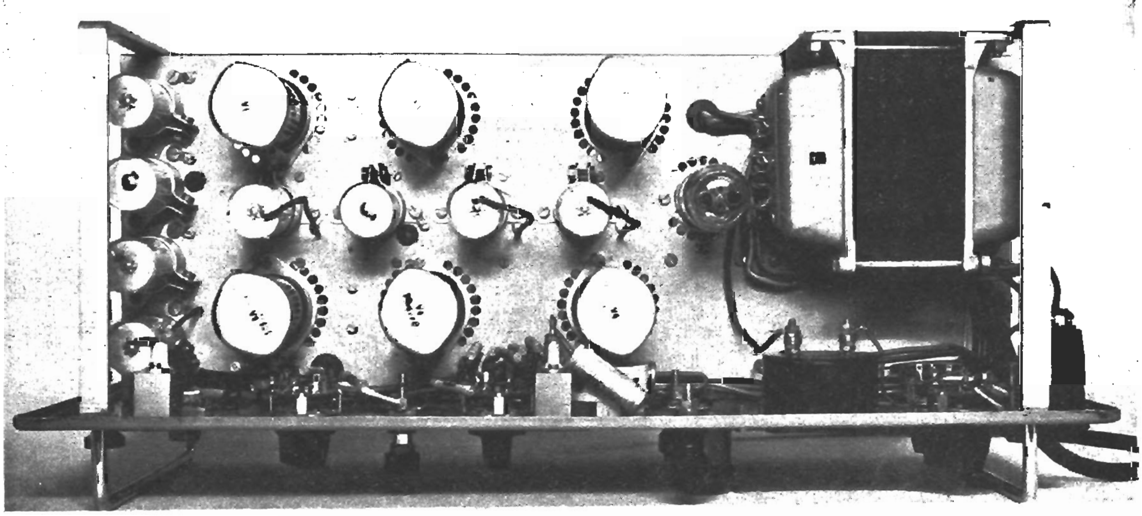

Plate XIV. Television Portable Sending Amplifier TV/PSA/1. Top view with cover removed

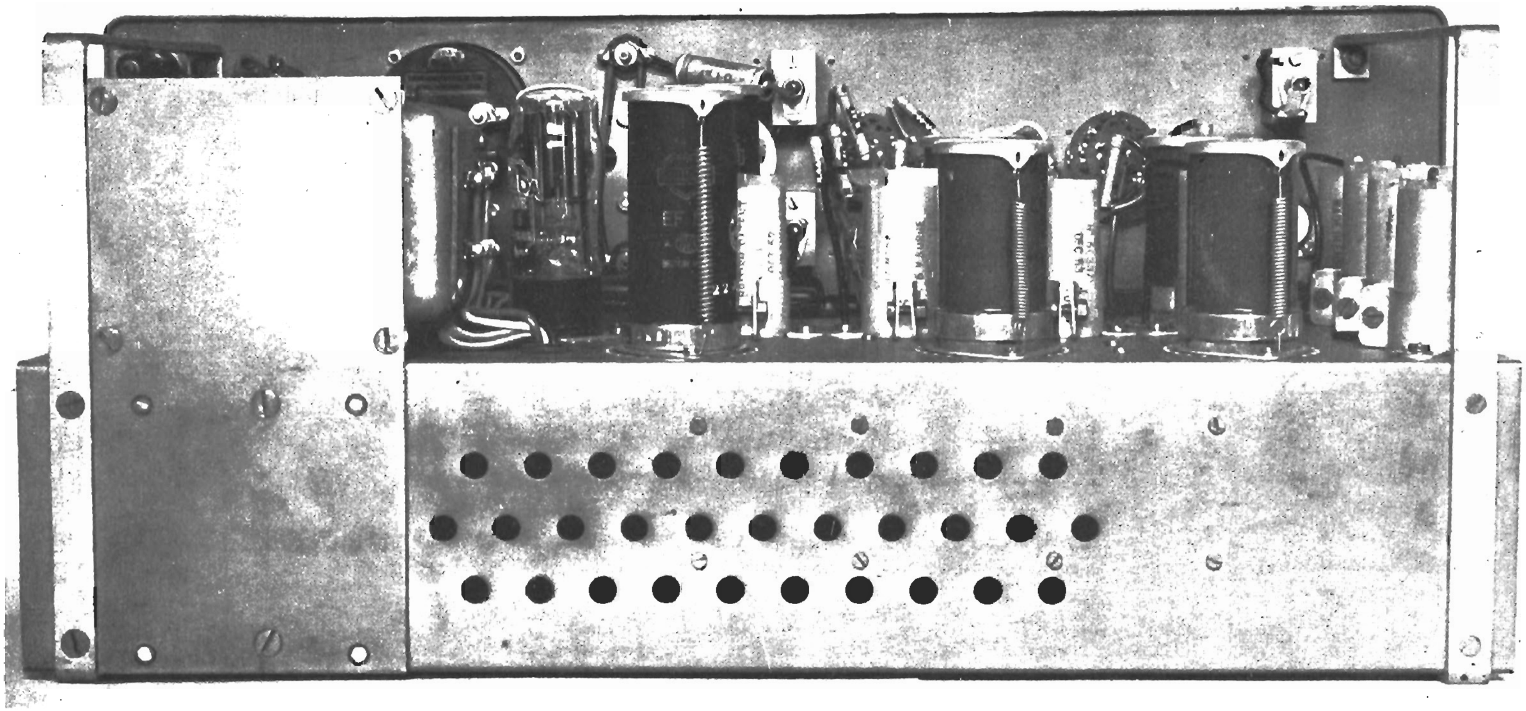

Plate XV. Television Portable Sending Amplifier TV/PSA/1. Rear view with cover removed.

COMPONENT TABLE: FIGS. 2 AND 3
PAGE 1

Comp.	Loc.	Type	Tolerance per cent	Comp.	Loc.	Type	Tolerance per cent
C1	B7	T.C.C. CP47S/PVC	20	L1	D6		
C2	C6	B.E.C. CE808/1	−20 +50	L2	F6		
C3	D8	T.C.C. SCE77L/PVC	−20 +50	L3	L6		
C4	E7	T.C.C. CP33N/PVC	20	L4	Q7		
C5	E6	B.E.C. CE818/1	−20 +50	L5	J6		
C6	K7	T.C.C. CP32N/PVC	25	L6	C3	BBC LD/6B/101	
C7	K6	B.E.C. CE809/1	−20 +50	L7	E3	BBC LD/6B/102	
C8	M8	T.C.C. SCE79PE/PVC	−20 +50	L8	G3	BBC LD/6B/103	
C9	N7	T.C.C. CP32N/PVC	25	L9	J3	BBC LD/6B/104	
C10	P8	T.C.C. CP32N/PVC	25	L10	L3	BBC LD/6B/105	
C11	O8	B.E.C. CE809/1	−20 +50				
C12	P7	Hunt B818	20	R1	A8	Erie 109 0·25W	2
C13	R8	T.C.C. CE18B/PVC	−20 +50	R2	B8	Reliance TW/1/8	
C14	R7	T.C.C. CP35N/PVC	20			Non-inductive	
C15	U7	B.E.C. CE811/1	−20 +50	R3	C8	Erie 9 0·25W	10
C16	F12	T.C.C. CP46S/PVC	20	R4	C7	Erie 9 0·25W	10
C17	G11	B.E.C. CE809/1	−20 +50	R5	C7	Erie 109 0·25W	2
C18	H12	T.C.C. SCE77L/PVC	−20 +50	R6	C6	Dubilier BTB 1W	10
C19	H11	T.C.C. CP46S/PVC	20	R7	C5	Erie 9 0·25W	5
C20	J11	B.E.C. CE809/1	−20 +50	R8	D8	Erie 9 0·25W	10
C21	K10	B.E.C. CE809/1	−20 +50	R9	D6	Erie 9 0·25W	10
C22	L11	T.C.C. CP46S/PVC	20	R10	K8	Erie 9 0·25W	10
C23	L11	T.C.C. CSM20N	5	R11	K8	Erie 9 0·25W	10
C24	N10	B.E.C. CE809/1	−20 +50	R12	L7	Painton P301 4·5W	5
C25	O11	T.C.C. CP46S/PVC	20	R13	L6	Painton P301 4·5W	5
C26	P12	T.C.C. CP46S/PVC	20	R14	L5	Erie 9 0·25W	5
C27	Q13	T.C.C. CP46S/PVC	20	R15	L9	Erie 9 0·25W	10
C28	T10	B.E.C. CE809/1	−20 +50	R16	L8	Erie 9 0·25W	10
C29	U11	T.C.C. CP46S/PVC	20	R17	M6	Erie 9 0·25W	10
C30	U12	T.C.C. CP46S/PVC	20	R18	N8	Erie 9 0·25W	10
C31	X13	T.C.C. CP46S/PVC	20	R19	N7	Erie 9 0·25W	10
C32	G8	T.C.C. SCE77L/PVC	−20 +50	R20	O6	Painton P301 4·5W	5
C33	G7	T.C.C. CP46S/PVC	20	R21	O5	Erie 9 0·25W	5
C34	H6	B.E.C. CE808/1	−20 +50	R22	O8	Dubilier BTB 1W	10
C35	J8	T.C.C. SCE77L/PVC	−20 +50			in parallel	
C36	B2	T.C.C. 701SMP FIN. C	2	R23	O8	Erie 9 0·25W	10
C37	D2	T.C.C. 701SMP FIN. C	2	R24	P8	Erie 9 0·25W	10
C38	F2	T.C.C. 701SMP FIN. C	2	R25	Q6	Erie 109 0·25W	5
C39	H2	T.C.C. SM1007	2	R26	P6	Erie 108 0·5W	5
C40	K2	T.C.C. 701SMP FIN. C	2	R27	Q5	Erie 9 0·25W	5
C41	P7	Hunt B815	20	R28	Q8	Erie 109 0·25W	2
C42	P7	T.C.C. CP32N/PVC	25	R29	R8	Reliance TW/1	
C43	Q8	Erie P199/K Insulated	10			Non-inductive	
C44	Y7	B.E.C. CE818/1	−20 +50	R30	R7	Painton P302 6W	5
C45	M8	Erie P100/K Insulated	10	R31	S8	Erie 9 0·25W	10
C46	F11	T.C.C. CSM20N	5	R32	S7	Erie 9 0·25W	10

COMPONENT TABLE: FIGS. 2 AND 3
PAGE 2

Comp.	Loc.	Type	Tolerance per cent	Comp.	Loc.	Type	Tolerance per cent
R33	S6	Painton P301 4·5W	5	R72	S10	Erie 9 0·25W	5
R34	S5	Erie 9 0·25W	5	R73	T12	Erie 9 0·25W	10
R35	T8	Erie 100 1W	2	R74	U12	Erie 9 0·25W	10
R36	T8	Erie 108 0·5W	2	R75	V12	Erie 108 0·5W	2
R37	U8	Erie 108 0·5W	2	R76	W12	Erie 108 0·5W	2
R38	F13	Erie 9 0·25W	10	R77	W12	Erie 109 0·25W	2
R39	F12	Erie 9 0·25W	10	R78	E8	Erie 9 0·25W	10
R40	G11	Dubilier BTB 1W	10	R80	P8	Erie 100 1W	2
R41	G10	Dubilier BTB 1W	10	R81	R6	Reliance TW/1 Non-inductive	
R42	G9	Erie 9 0·25W	5				
R43	G13	Erie 9 0·25W	10	R82	R6	Erie 100 1W	2
R44	H10	Erie 9 0·25W	10	R83	P8	Morganite ANAR 50350 19800 with screwdriver slot	
R45	H13	Erie 9 0·25W	10				
R46	J12	Erie 9 0·25W	10				
R47	J11	Erie 9 0·25W	10	R84	P13	Morganite ANAR 15450 19800 with screwdriver slot	
R48	J11	Erie 9 0·25W	10				
R49	K11	Erie 9 0·25W	10				
R50	K10	Dubilier BTB 1W	10	R85	F5	Erie 9 0·25W	5
R51	K9	Erie 9 0·25W	5	R86	G8	Erie 9 0·25W	10
R52	K12	Erie 9 0·25W	10	R87	G6	Erie 9 0·25W	10
R53	L13	Erie 9 0·25W	10	R88	H8	Erie 9 0·25W	10
R54	L10	Erie 9 0·25W	10	R89	H7	Erie 9 0·25W	10
R55	M12	Erie 9 0·25W	10	R90	H7	Erie 109 0·25W	2
R56	M11	Erie 100 1W	2	R91	J6	Dubilier BTB 1W	10
R57	M10	Erie 108 0·5W	2	R92	J5	Erie 9 0·25W	5
R58	N10	Erie 108 0·5W	2	R93	J8	Erie 9 0·25W	10
R59	N10	Painton P306 4·5W	5	R94	J6	Erie 9 0·25W	10
R60	N9	Erie 9 0·25W	5	R95*	C1	Erie 100 1W	2
R61	N12	Erie 9 0·25W	10	R96	C2	Erie 109 0·25W	2
R62	O13	Erie 9 0·25W	10	R97	E1	Erie 100 1W	2
R63	P12	Erie 109 0·25W	2	R98	E2	Erie 109 0·25W	2
R64	E8	Erie 9 0·25W	10	R99	G1	Erie 100 1W	2
R65	Q12	Erie 109 0·25W	2	R100	G2	Erie 109 0·25W	2
R66	Q12	Erie 109 0·25W	2	R101	H1	Erie 100 1W	2
R67	R12	Erie 9 0·25W	10	R102	J2	Erie 109 0·25W	2
R68	S11	Erie 100 1W	2	R103	K1	Erie 108 0·5W	2
R69	S10	Erie 108 0·5W	2	R104	L2	Erie 109 0·25W	2
R70	T11	Erie 108 0·5W	2	R105	F7	Erie 109 0·25W	2
R71	S10	Painton P306 4·5W	5	R106	F6	Dubilier BTB 1W	10

*Comprises two resistors in parallel of 16·3 ohms each.

FIG. 3

As for Component Table Fig. 2 with the following omission:

Comp.	Loc.
C45	N8

54/GGJ/006
DJ1295
ISS. 5

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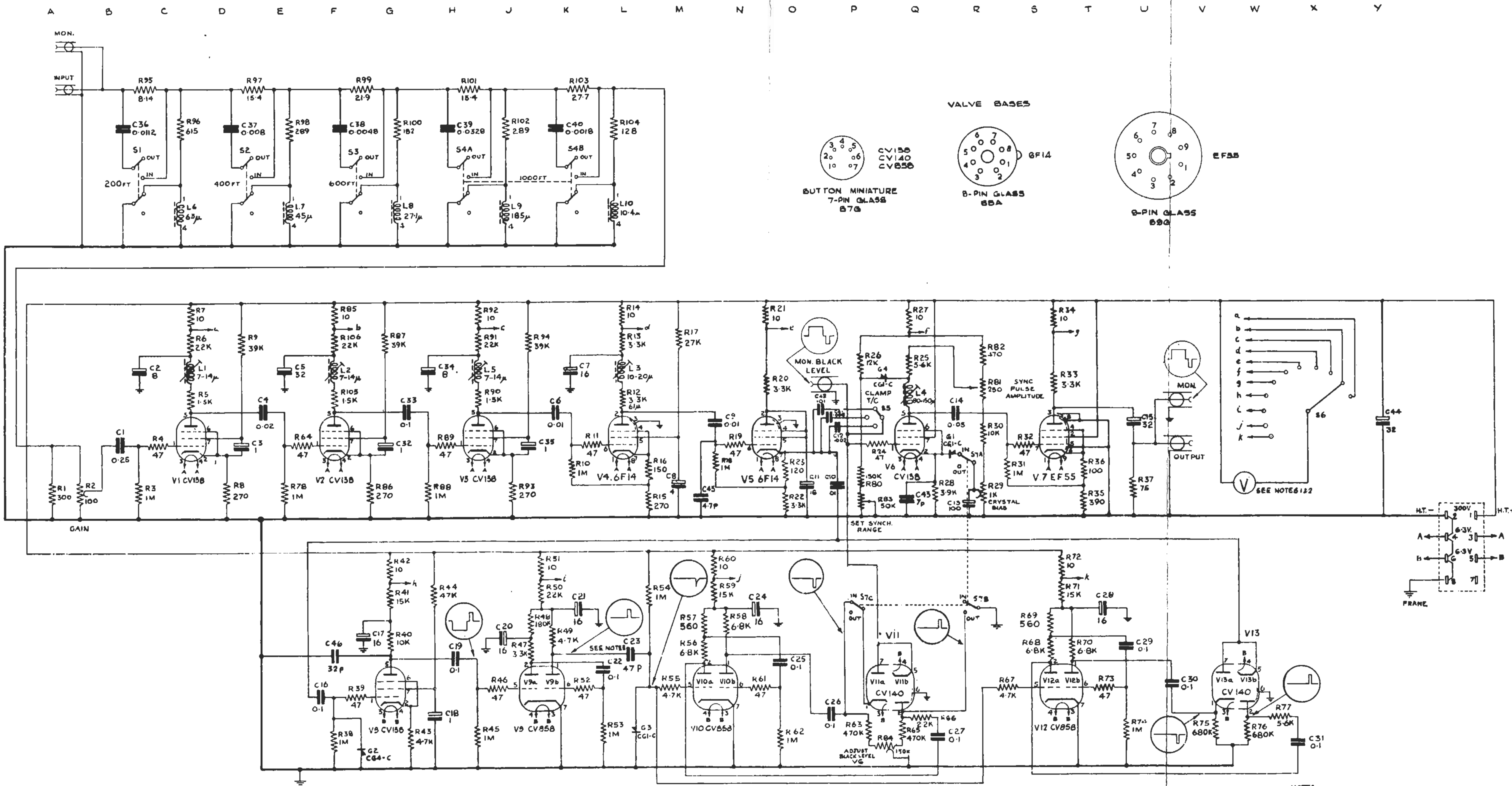
FIG 2
ISSUE 2

V2



NOTES.

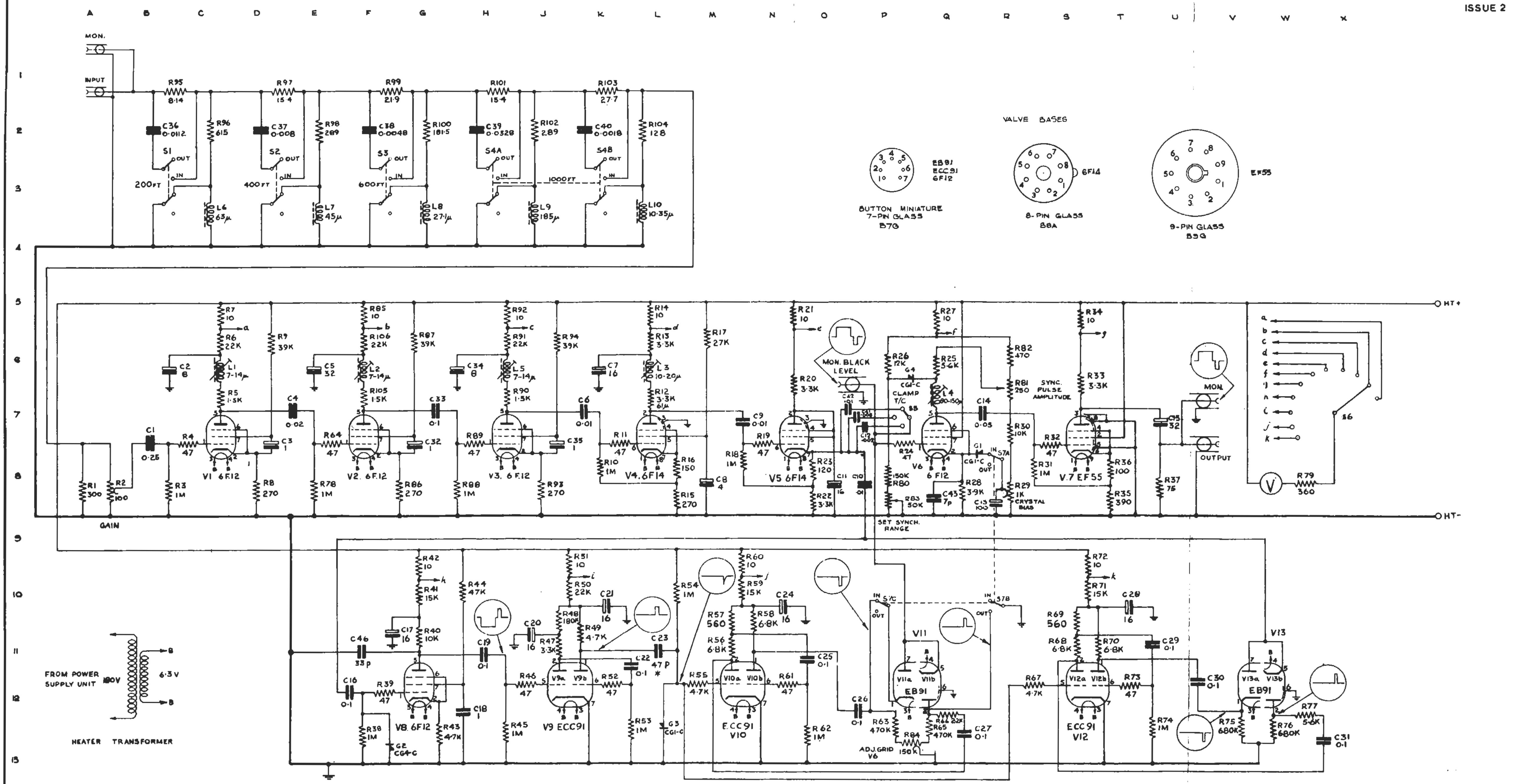
1. METER BUILT OUT TO 500Ω
2. WHEN AN EAC METER IS USED A 430Ω SERIES RESISTOR (R79) IS FITTED.
3. C23 TO BE ADJUSTED ON TEST.

TELEVISION STABILISING AMPLIFIER TV/STA/2 : CIRCUIT

54/GGJ/009
DJ 1005

V2

FIG 3
ISSUE 2



TELEVISION PORTABLE STABILISING AMPLIFIER TV/PSTA/1 : CIRCUIT

Component Table Fig. 4

Comp.	Loc.	Type	Tolerance Per cent
C1	F2	Plessey Electrolytic CE874/1	
C2	F6	,, ,, ,,	
C3	G2	,, ,, ,,	
C4	G6	,, ,, ,,	
C5	L5	T.C.C. CP46S PVC	
C6	C8	Hunt 351/A	
C7	D8	,, ,,	
L1	E1	Pye 6029	
L2	F1	,, ,,	
R1	E2	Erie 109 0·25W	±2
R2	E6	,, ,, ,,	,,
R3	F2	,, ,, ,,	,,
R4	F6	,, ,, ,,	,,
R5	K6	,, 9 ,,	±10
R6	M6	,, ,, ,,	,,
R7	L4	,, ,, ,,	±5
R8	K4	,, ,, ,,	±10
R9	J1	,, ,, ,,	,,
R10	H1	Morganite R 1W	,,
R11	H6	,, ,, ,,	,,
R12	N5	,, ,, ,,	,,
R13	N7	,, ,, ,,	,,
R14	N6	Reliance TW/1/8S	±5
R15	K1	Erie 8 0·5W	±10
R16	L1	,, ,, ,,	,,
R17	L3	,, ,, ,,	,,
R18	K3	,, ,, ,,	,,
T1	B3	Pye 6062	

54/GGJ/008
DB1004

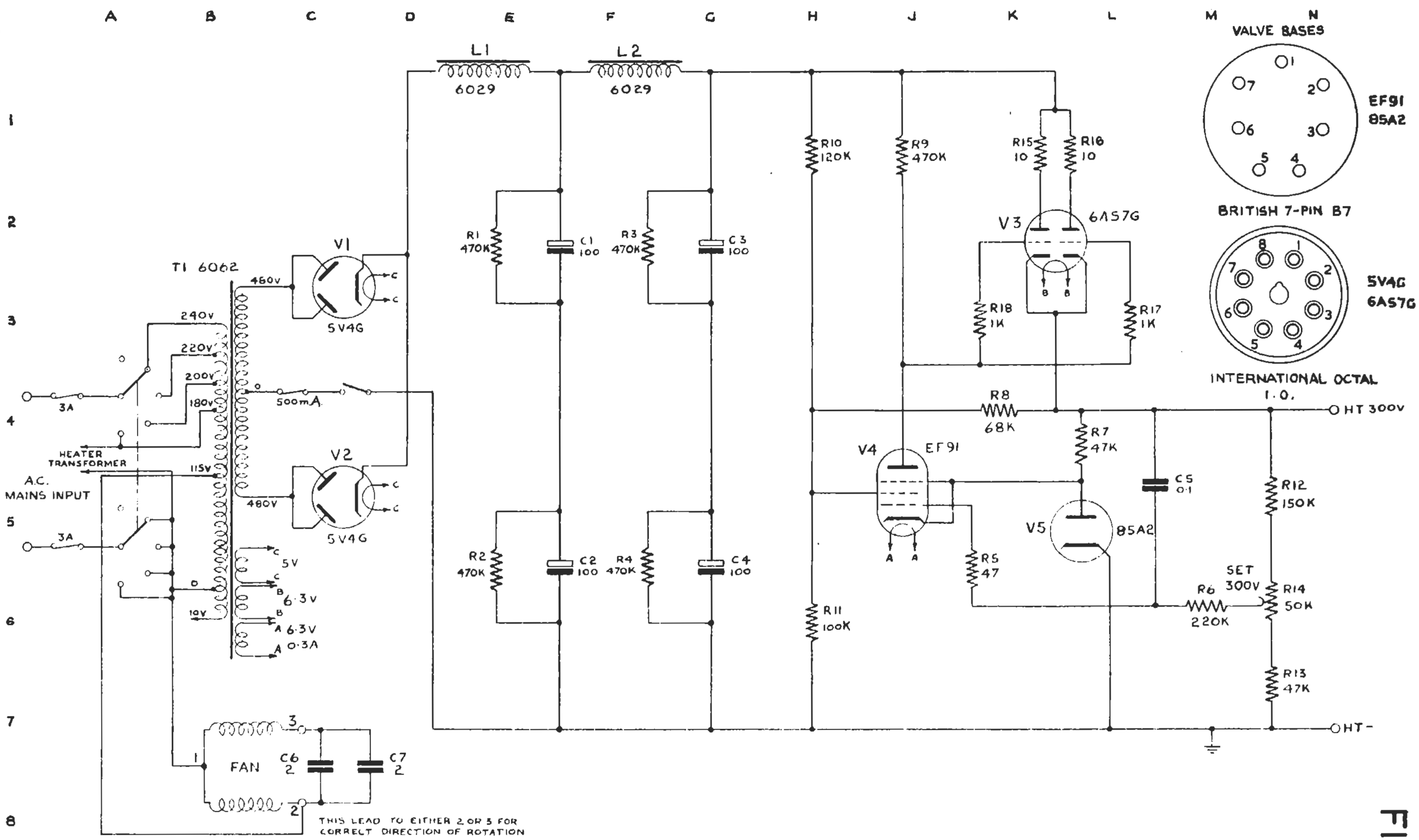


FIG 4

TELEVISION PORTABLE STABILISING AMPLIFIER TV/PSTA/1 MAINS UNIT

V2

COMPONENT TABLE: FIG. 5

PAGE 1

TELEVISION STABILISING AMPLIFIER TV/STA/2A

Comp.	Loc.	Type	Tolerance per cent	Comp.	Loc.	Type	Tolerance per cent
C1	B8	T.C.C. CP47S/PVC	20	L1	D6		
C2	C6	B.E.C. CE808/1		L2	F6		
C3	D8	T.C.C. SCE77L/PVC		L3	L6		
C4	E7	T.C.C. CP33N/PVC	20	L4	Q7		
C5	E6	B.E.C. CE818/1		L5	J6		
C6	K7	T.C.C. CP32N/PVC	25	L6	C3	BBC LD/6B/101	
C7	K6	B.E.C. CE809/1		L7	E3	BBC LD/6B/102	
C8	M8	T.C.C. SCE79PE/PVC		L8	G3	BBC LD/6B/103	
C9	N7	T.C.C. CP32N/PVC	25	L9	J3	BBC LD/6B/104	
C10	P8	T.C.C. CP32N/PVC		L10	L3	BBC LD/6B/105	
C11	O8	B.E.C. CE809/1					
C12	P7	Hunt B818		R1	A8	Erie 109 0·25W	2
C13	R8	T.C.C. CE18B/PVC		R2	B8	Reliance TW/1/8	
C14	R7	T.C.C. CP35N/PVC	20			Non-inductive	
C15	U7	B.E.C. CE811/1		R3	C8	Erie 9 0·25W	10
C16	F12	T.C.C. CP46S/PVC	20	R4	C7	Erie 9 0·25W	10
C17	G11	B.E.C. CE809/1		R5	C7	Erie 109 0·25W	2
C18	H12	T.C.C. SCE77L/PVC		R6	C6	Dubilier BTB 1W	10
C19	H11	T.C.C. CP46S/PVC	20	R7	C5	Erie 9 0·25W	5
C20	J11	B.E.C. CE809/1		R8	D8	Erie 9 0·25W	10
C21	K10	B.E.C. CE809/1		R9	D6	Erie 9 0·25W	10
C22	L11	T.C.C. CP46S/PVC	20	R10	K8	Erie 9 0·25W	10
C23	L11	T.C.C. CSM20N	5	R11	K8	Erie 9 0·25W	10
C24	N10	B.E.C. CE809/1		R12	L7	Painton P301 4·5W	5
C25	O11	T.C.C. CP46S/PVC	20	R13	L6	Painton P301 4·5W	5
C26	P12	T.C.C. CP46S/PVC		R14	L5	Erie 9 0·25W	5
C27	Q13	T.C.C. CP46S/PVC		R15	R9	Erie 9 0·25W	10
C28	T10	B.E.C. CE809/1		R16	L8	Erie 9 0·25W	10
C29	U11	T.C.C. CP46S/PVC	20	R17	M6	Erie 9 0·25W	10
C30	U12	T.C.C. CP46S/PVC		R18	N8	Erie 9 0·25W	10
C31	X13	T.C.C. CP46S/PVC		R19	N7	Erie 9 0·25W	10
C32	G8	T.C.C. SCE77L/PVC		R20	O6	Painton P301 4·5W	5
C33	G7	T.C.C. CP46S/PVC	20	R21	O5	Erie 9 0·25W	5
C34	H6	B.E.C. CE808/1		R22	O8	Dubilier BTB 1W	10
C35	J8	T.C.C. SCE77L/PVC				in parallel	
C36	B2	T.C.C. 701 SMP FIN. C	2	R23	O8	Erie 9 0·25W	10
C37	D2	T.C.C. 701 SMP FIN. C	2	R24	P8	Erie 9 0·25W	10
C38	F2	T.C.C. 701 SMP FIN. C	2	R25	Q6	Erie 109 0·25W	2
C39	H2	T.C.C. SM1007	2	R26	P6	Erie 108 0·5W	5
C40	K2	T.C.C. 701 SMP FIN. C	2	R27	Q5	Erie 9 0·25W	5
C41	P7	Hunt B815	20	R28	Q8	Erie 109 0·25W	2
C42	P7	T.C.C. CP32N/PVC	25	R29	R8	Reliance TW/1	
C43	Q8	Erie P100/K Insulated	10			Non-inductive	
C44	Z8	B.E.C. CE818/1		R30	R7	Painton P302 6W	5
C45	M8	Erie P199/K Insulated	10	R31	S8	Erie 9 0·25W	10
C46	S7	B.E.C. CE911		R32	S7	Erie 9 0·25W	10
C47	U7	T.C.C. CP47S/PVC		R33	S6	Painton P301 4·5W	5
C48	U8	B.E.C. CE809/1		R34	S5	Erie 9 0·25W	5
C49	W6	B.E.C. CE809/1		R35	T8	Erie 100 1W	2
C50	O3	Hunt B815		R36	T8	Erie 108 0·5W	2
C51	F11	T.C.C. CSM20N	5	R38	F13	Erie 9 0·25W	10

COMPONENT TABLE: FIG. 5
PAGE 2

Comp.	Loc.	Type	Tolerance per cent	Comp.	Loc.	Type	Tolerance per cent
R39	F12	Erie 9 0·25W	10	R83	P8	Morganite ANAR 50350	
R40	G11	Dubilier BTB 1W	10			20800 with screwdriver	
R41	G10	Dubilier BTB 1W	10			slot	
R42	G9	Erie 9 0·25W	5	R84	Q13	Morganite ANAR 15450	
R43	G13	Erie 9 0·25W	10			20800 with screw-	
R44	H10	Erie 9 0·25W	10			driver slot	
R45	H13	Erie 9 0·25W	10	R85	F5	Erie 9 0·25W	5
R46	J12	Erie 9 0·25W	10	R86	G8	Erie 9 0·25W	10
R47	J11	Erie 9 0·25W	10	R87	G6	Erie 9 0·25W	10
R48	J11	Erie 9 0·25W	10	R88	H8	Erie 9 0·25W	10
R49	K11	Erie 9 0·25W	10	R89	H7	Erie 9 0·25W	10
R50	K10	Dubilier BTB 1W	10	R90	H7	Erie 109 0·25W	2
R51	K9	Erie 9 0·25W	10	R91	J6	Dubilier BTB 1W	10
R52	K12	Erie 9 0·25W	10	R92	J5	Erie 9 0·25W	5
R53	L13	Erie 9 0·25W	10	R93	J8	Erie 9 0·25W	10
R54	L10	Erie 9 0·25W	10	R94	J6	Erie 9 0·25W	10
R55	M12	Erie 9 0·25W	10	R95	C1	Erie 100 1W	2
R56	M11	Erie 100 1W	2			in parallel	
R57	M10	Erie 108 0·5W	2	R96	C2	Erie 109 0·25W	2
R58	N10	Erie 108 0·5W	2	R97	E1	Erie 100 1W	2
R59	N10	Painton P306 4·5W	5	R98	E2	Erie 109 0·25W	2
R60	N9	Erie 9 0·25W	10	R99	G1	Erie 100 1W	2
R61	N12	Erie 9 0·25W	10	R100	G2	Erie 100 1W	2
R62	O13	Erie 9 0·25W	10	R101	H1	Erie 100 1W	2
R63	P12	Erie 109 0·25W	2	R102	J2	Erie 109 0·25W	2
R64	E8	Erie 9 0·25W	10	R103	K1	Erie 108 0·5W	2
R65	Q12	Erie 109 0·25W	2	R104	L2	Erie 109 0·25W	2
R66	Q12	Erie 109 0·25W	2	R105	F7	Erie 109 0·25W	2
R67	R12	Erie 9 0·25W	10	R106	F6	Dubilier BTB 1W	10
R68	S11	Erie 100 1W	2	R107	T6	Painton AP301 4·5W	5
R69	S10	Erie 108 0·5W	2	R108	T6	Painton P301 4·5W	5
R70	T11	Erie 108 0·5W	2	R109	U6	Dubilier BTB 1W	10
R71	S10	Painton P306 4·5W	5	R110	U8	Painton P301 4·5W	5
R72	S10	Erie 9 0·25W	5	R111	U6	Painton P301 4·5W	5
R73	T12	Erie 9 0·25W	10	R112	U8	Morganite HNAP 10250	
R74	U12	Erie 9 0·25W	10			with screwdriver slot	
R75	V12	Erie 108 0·5W	2	R113	V8	Erie 9 0·25W	10
R76	W12	Erie 108 0·5W	2	R114	V7	Erie 9 0·25W	10
R77	W12	Erie 108 0·5W	2	R115	X8	Erie 108 0·5W	2
R78	E8	Erie 9 0·25W	10	R116	X7	Painton AP306 4·5W	5
R81	R6	Reliance TW/1		R117	W6	Painton P301 4·5W	5
		Non-inductive		R118	P8	Painton P302 6W	5
R82	R6	Erie 100 1W	2	R119	P6	Erie 108 0·5W	2

TELEVISION STABILISING AMPLIFIER TV/STA/2B

As for TV/STA/2A, with the following exceptions:

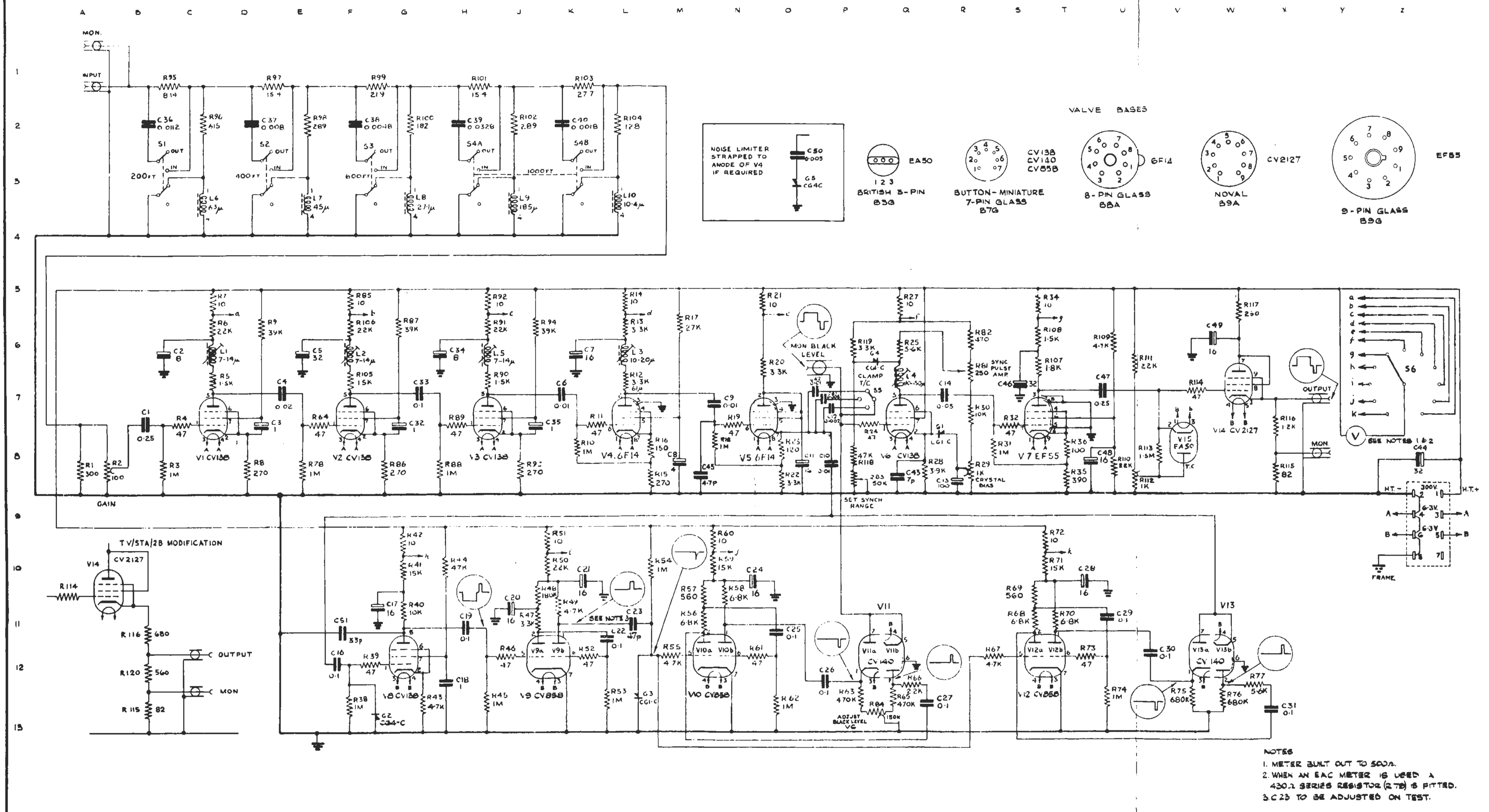
Comp.	Loc.	Type	Tolerance per cent
R116	B11	Erie 100 1W	2
R120	B12	Erie 100 1W	2

54/GGJ/007
DJ 1494
ISS 3

V2

FIG 5

ISSUE 2



TELEVISION STABILISING AMPLIFIERS TV/STA/2A AND 2B: CIRCUIT