SWITCH AND STORE PANELS PA1/514 SERIES

Introduction

The PA1/514 accepts either a picture signal or an I signal and a Q signal on one line standard and converts the input to another line standard. It also requires the following pulse inputs on the input and output line standards:

(a) Clock pulses, interrupted during line blanking, used to time high-speed shift registers.
(b) Line start pulses, used to start high-speed shift registers.
(c) Three pairs of drive pulse inputs, used to time low-speed shift registers.
(d) Reset pulses, used to start low-speed shift registers.

The input and output standards together with the signal converted for each variation in the series are given in Table 1. The starred standards represent an intermediate stage of a standards conversion process and therefore are not a broadcast standard.

General Description

Simplified block diagrams of the PA1/514 series are given in Fig. 1; the PA1/514B differs from the

TABLE 1

Unit	*PA1/514*	*PA1/514A*	*PA1/514B*	*PA1/514C*	*PA1/514D*
Converted signal	picture	picture	I and Q	picture	picture
Input standard	625/50	405/50	525/50*	525/50*	625/50
Output standard	405/50	625/50	625/50*	625/50	405/50

TABLE 2

The PA1/514 comprises the following units mounted in a special frame:

Unit	*PA1/514*	*PA1/514A*	*PA1/514B*	*PA1/514C*	*PA1/514D*
Input high-speed switch card	UN9/517i(36)	UN9/517Ai(36)	UN9/557(36)	UN9/557(36)	UN9/557(36)
Input high-speed switch supply	UN9/517ii	UN9/517ii	UN9/558	UN9/558	UN9/558
Store matrix	PA1/510(9)	PA1/510A(9)	PA1/510(9)	PA1/510B(9)	PA1/510B(9)
Shift register	PA1/511(3)	PA1/511(3)	PA1/511A(3)	PA1/511A(3)	PA1/511A(3)
Output high-speed switch card	UN9/518i(36)	UN9/518Ai(36)	UN9/518i(27) UN9/561(9)	UN9/518i(36)	UN9/559B(36)
Output high-speed switch supply	UN9/518ii	UN1/559	UN9/560	UN9/560	UN9/560

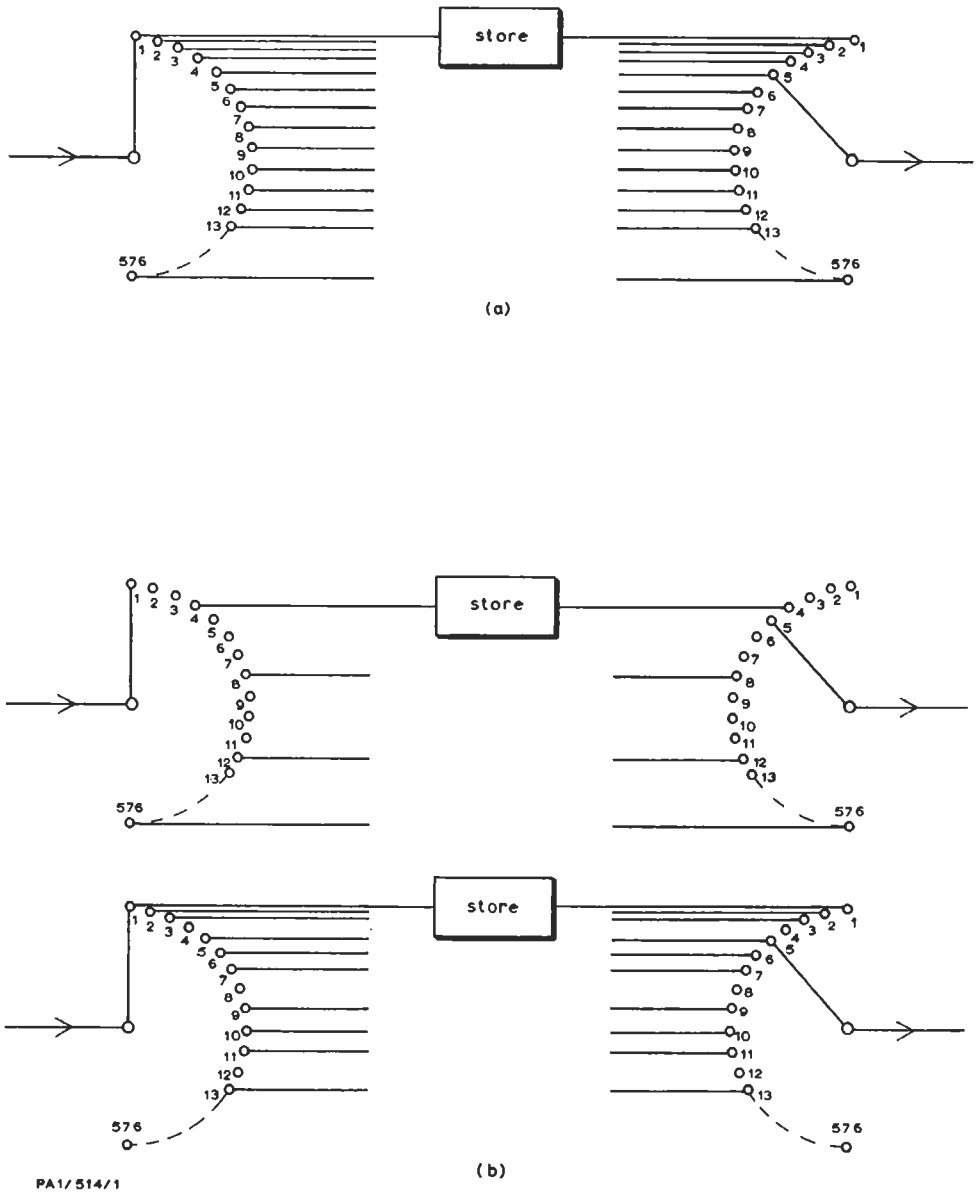

Fig. 1 Simplified Block Diagrams of the PA1/514
(a) all units except PA1/514B (b) PA1/514B

rest of the series as shown at (b). The input signal in Fig. 1(a) is fed via a switch to 576 store circuits. The switch connects the input to every store once in each active line period. The timing of these connections is the same for every line so that the signal fed to each store is a series of line-frequency pulses, the amplitudes of which corresponds to a signal which describes a vertical strip of the picture one picture-element in width.

Each store comprises a low-pass-filter type circuit which removes the input-standard line-frequency information and carries out the process of interpolation (see Instruction P.5). The low-frequency output signals of the stores are sampled by a switch operating at the output-standard line-frequency.

The PA1/514B is similar to the other versions in the series except that the 576 stores are distributed between two signal channels. One of these channels uses every fourth store. The second channel uses

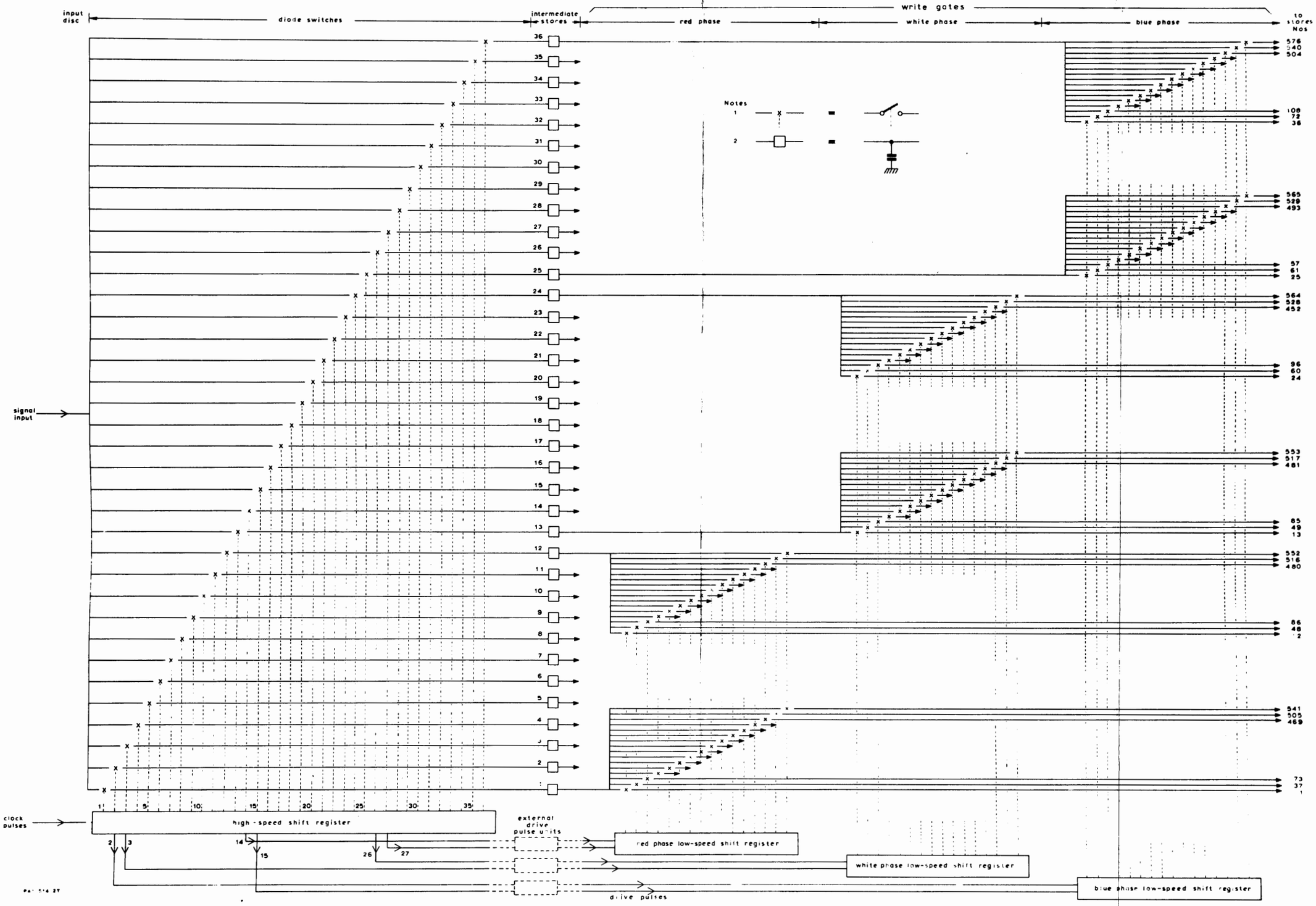

Fig. 2 Block Diagram of Input 2-stage Switching

the remainder of the stores.

Parts of the more detailed descriptions, which follow, of sections of the switch and store panel are given in terms of the PA1/514D. The other panels are similar.

Two-stage Switching

For convenience the 576-way switching is carried out in two stages as shown in Fig. 2. A 36-way high-speed switch feeds thirty-six 16-way low-speed switches. These 16-way switches are grouped in three phases (red, white, blue) of twelve switches in each phase. The 36-way switch closes each of its contacts in turn, feeding samples of input-signal information into the intermediate stores. This process is repeated 16 times throughout the active line period.

After the first 12 intermediate stores in the red phase have been fed with input signal information, the first contacts in the red-phase 16-way low-speed switches close, transferring this information to the main stores, and re-open; this leaves the intermediate stores ready to receive their next samples of input-signal information. This is repeated for the white and blue phases until the 576 main stores are filled. The output switching is similar to the input switching in reverse but the timing is different.

The switch connections are made by a series of pulses from a shift register. A shift register is a counter circuit which accepts timing pulses and a starting pulse. Each stage of the shift register in turn produces a pulse at a time determined by a timing pulse. The count is initiated by the starting pulse.

The high-speed shift register, which is distributed between the cards of the high-speed switches with one stage on each card, uses clock pulses for timing and start pulses to initiate the count. The output of the high-speed shift register is connected to its input so that the 36-way switching is repeated until the clock pulses finish at the end of each line.

Output pulses from the high-speed shift register are used to produce drive pulses externally to the panel. These drive pulses are used to time the low-speed shift register in each phase. The low-speed shift registers use reset pulses as starting pulses.

Fig. 3 shows the physical layout of the PA1/514.

Signal Transfer

A simplified circuit of the PA1/514D showing the signal path through one of the 576 main stores is given in Fig. 4. The input signal, from a low-impedance source, is fed to the centre of a circular

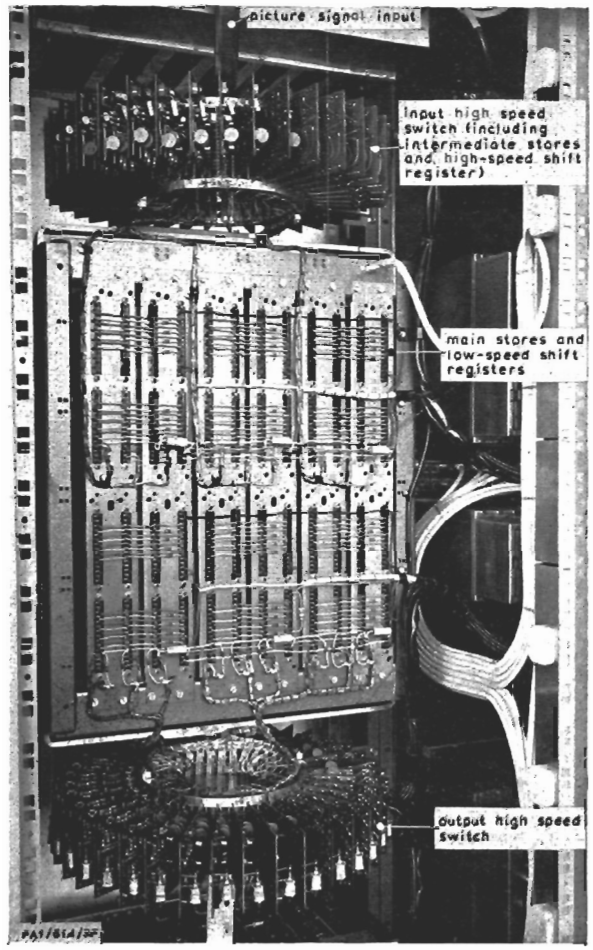

Fig. 3 Physical Layout of the PA1/514

disc loaded with capacitor C1. Thirty-six diode switches are arranged around the periphery of the disc to give equal delays to signals fed to each of the switches. Each diode switch closes for about 50 ns and the charge on capacitor C1 is shared with the intermediate store capacitor C2. Because of their relative values there is very little change in the voltage across capacitor C1 when this connection is made.

After all the 12 capacitors C2 in one phase have been charged with input-signal samples, the outputs of the amplifiers following these capacitors are connected, via their write gates, to their 12 respective main stores. These amplifiers have zero gain and low-impedance outputs so that capacitors C3 at the inputs to the main stores charge to the same voltage as that of the sampled input signal.

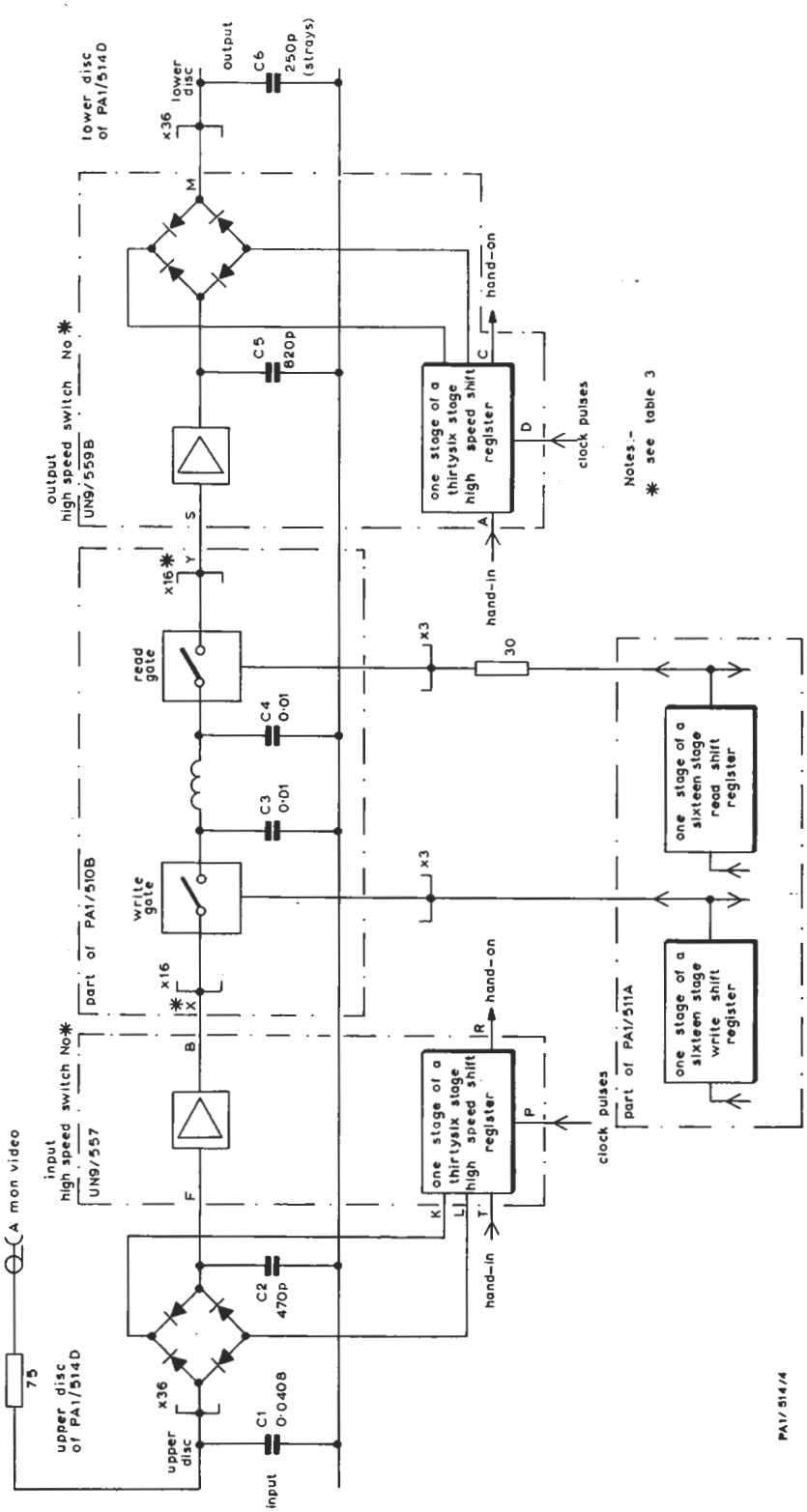

Fig. 4 Simplified Circuit of PA1/514D showing Signal Path Through One of Main Stores

The main stores comprise an unterminated dissipative low-pass filter which removes line-frequency information and provides a degree of vertical aperture correction.

A group of twelve read gates in one phase close at the same time. While these gates are closed capacitors C5 are charged from their amplifiers to the voltage across their respective capacitors C4. Also while these read gates are closed the 12 output diode switches in the same phase close in turn and the voltage developed across capacitor C6 is a picture signal whose standard depends upon the switching rate of the read gates and the output diode switches.

Table 3 gives the input and output connections for each group of 16 main stores. The layout of the sockets on the back of the PA1/514 is given in Fig. 5.

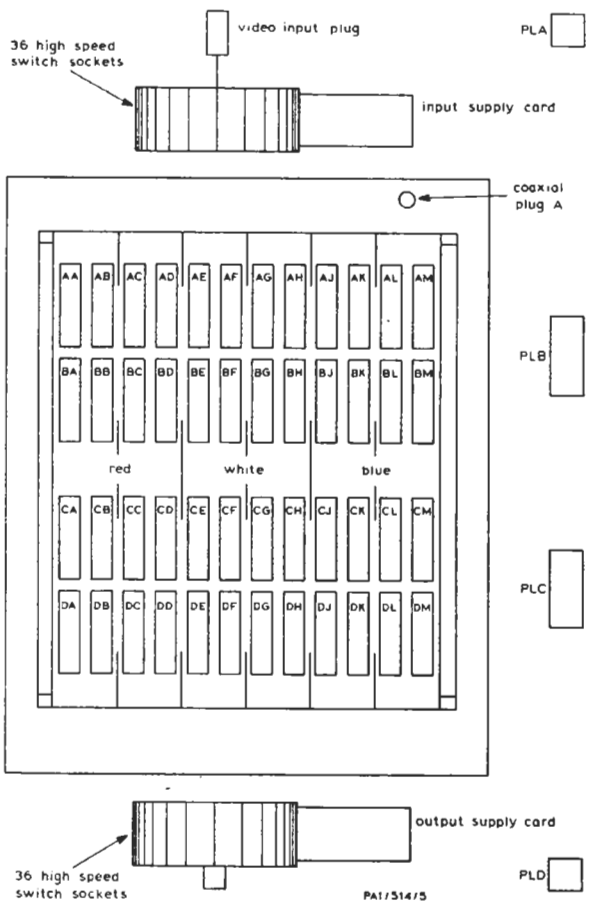

Fig. 5 Layout of Sockets on Back of PA1/514

TABLE 3

High-speed switch and store group Nos.	*X (skt & pin No.)*	*Y (skt & pin No.)*
1	BA12	DA12
2	BA13	DA13
3	BA14	DA14
4	BA15	DA15
5	BB12	DB12
6	BB13	DB13
7	BB14	DB14
8	BB15	DB15
9	BC12	DC12
10	BC13	DC13
11	BC14	DC14
12	BC15	DC15
13	BE12	DE12
14	BE13	DE13
15	BE14	DE14
16	BE15	DE15
17	BF12	DF12
18	BF13	DF13
19	BF14	DF14
20	BF15	DF15
21	BG12	DG12
22	BG13	DG13
23	BG14	DG14
24	BG15	DG15
25	BJ12	DJ12
26	BJ13	DJ13
27	BJ14	DJ14
28	BJ15	DJ15
29	BK12	DK12
30	BK13	DK13
31	BK14	DK14
32	BK15	DK15
33	BL12	DL12
34	BL13	DL13
35	BL14	DL14
36	BL15	DL15

Fig. 6 shows the wiring of part of the input and output discs. The diode switches on the input disc are located on the upper side of the disc and the capacitors (C1 = 6 × 0·0068 μF and 36 × C2 = 470 pF each) are located on the lower side of the disc. Fig. 7 shows the socket wiring of the store matrices and low-speed shift registers for one phase.

Pulse Timing

Input standard pulse waveforms showing typical relative timings are given in Fig. 8. Fig. 8(a) shows a composite video signal as fed to the parent converter although the signal fed to the PA1/514D is a picture signal. Start, reset and clock pulses, Fig. 8(b) to Fig. 8(d), are generated externally and are timed from the sync-pulse leading edges.

The positive-going trailing edge of the start pulse is fed to the output of high-speed switch card No. 24 where it triggers the blocking oscillator (a stage of

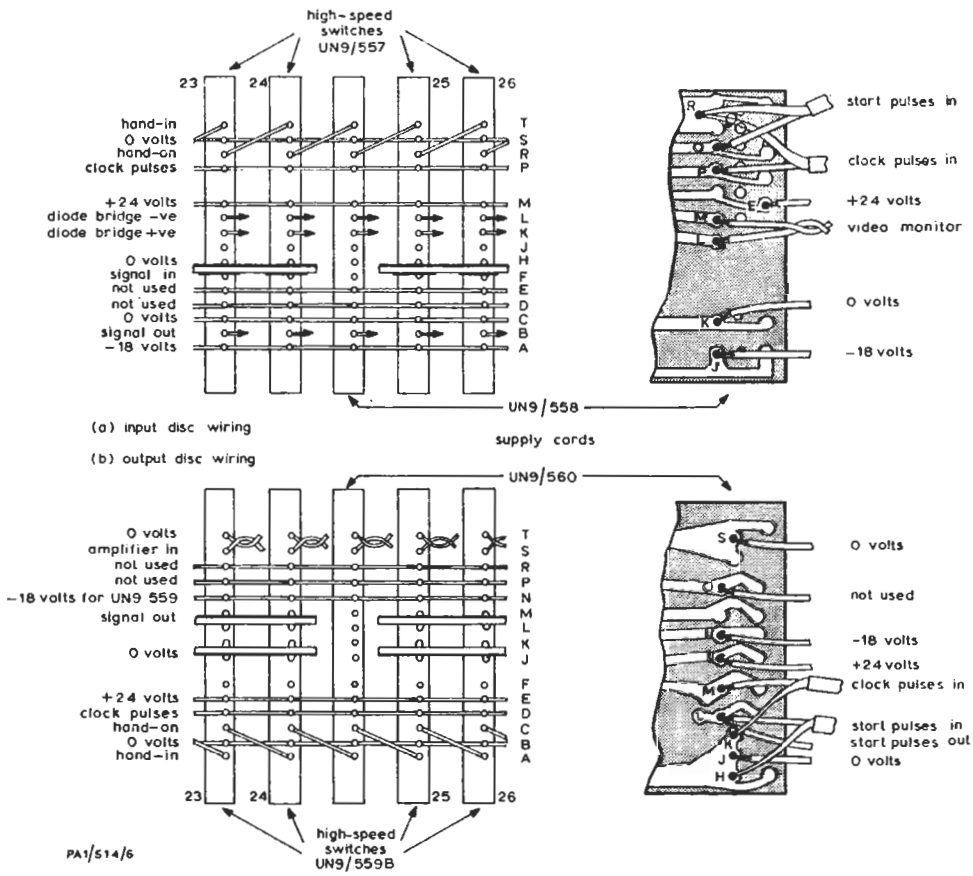

Fig. 6 Part of Wiring of Input and Output Discs

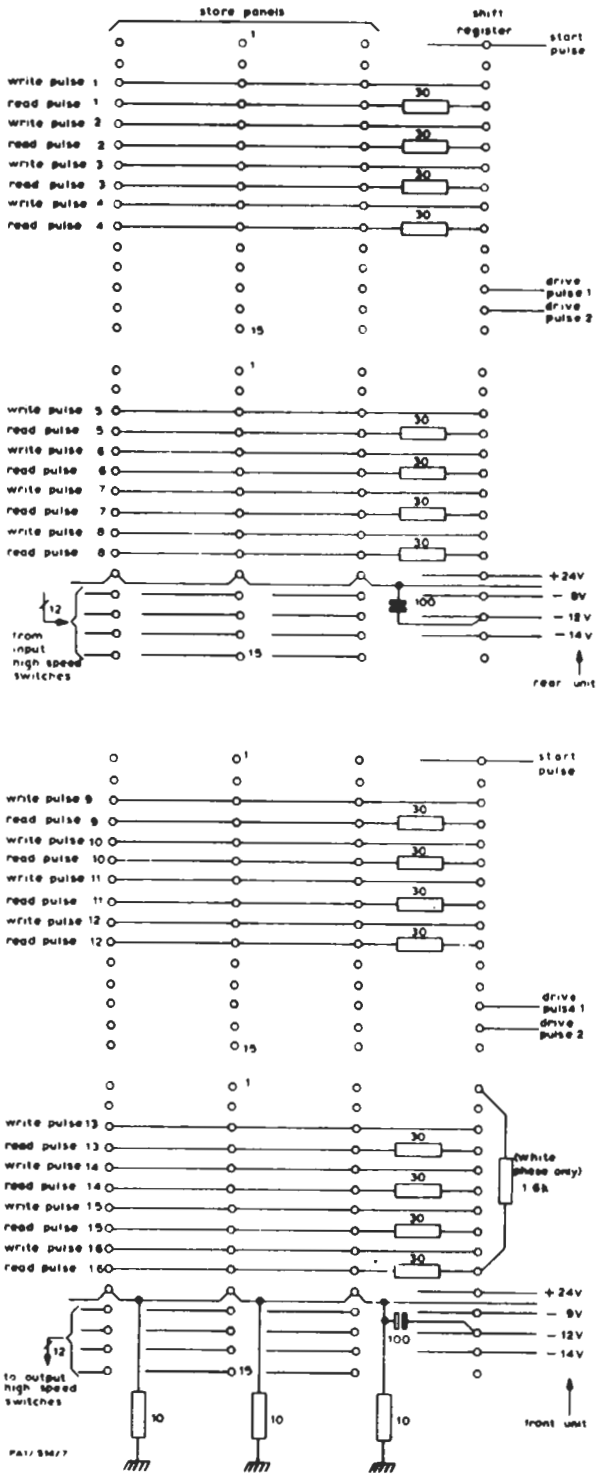

Fig. 7 Socket Connections of Store Matrices and Low-speed Shift-registers for One Phase

the high-speed shift register). The clock pulses then start and the high-speed switch cards give output switching pulses until there is a break in the clock pulses at about the end of the line period.

Output switching pulses, as shown in Table 4, are fed to three external drive pulse units associated with the red, white and blue phases.

TABLE 4

Phase	*Outputs from high-speed switch card Nos. to derive drive pulses*	
	start	*finish*
red	14	27
white	26	3
blue	2	15

In practice these pulses are taken from the hand-in inputs of the succeeding high-speed switch cards.

Each drive pulse unit produces two outputs of drive pulses. The start of each drive pulse is coincident with the first output given in Table 4 and the finish of each drive pulse is coincident with the second output pulse given in Table 4. The two drive pulse outputs in each phase produce pulses on alternate high-speed switching sequences. The first drive pulses in the white and blue phases are fed to the low-speed shift registers as drive pulse 2 and do not therefore result in a low-speed shift register output pulse. The first drive pulse in the red phase is fed to the red phase low-speed shift register as drive pulse 1 and therefore results in a shift register output pulse (red No. 1).

The sequence of pulses continues as shown in Fig. 8 until the clock pulses stop during the 17th high-speed switching sequence. If a high-speed switch output pulse is not available to finish the last blue phase drive pulse 2, it is ended by the reset pulse and in turn ends the low-speed shift register pulse (blue No. 16).

The relative timings shown in Fig. 8 depend upon the timing of the trailing edge of the start and reset pulses and upon the clock pulse frequency. The timing shown is typical in that three or four stores at either end of the active line are fed with blanking level.

The output line-standard pulse waveforms, shown in Fig. 9, are similar to the input line-standard waveforms with different pulse timings used to

trigger the drive pulses and hence the low-speed shift register pulses. These pulse timings are given in Table 5.

TABLE 5

Phase	*Outputs from high-speed switch card Nos. to derive drive pulses*	
	start	*finish*
red	27	18
white	3	30
blue	15	6

In practice these pulses are also taken from the hand-in inputs of the succeeding high-speed switch cards.

Output line-standard low-speed shift register pulse, white No. 16, and output line-standard start pulses are also used as outputs from the PA1/514D.

Test Procedure

The PA1/514 is tested as part of its parent unit.

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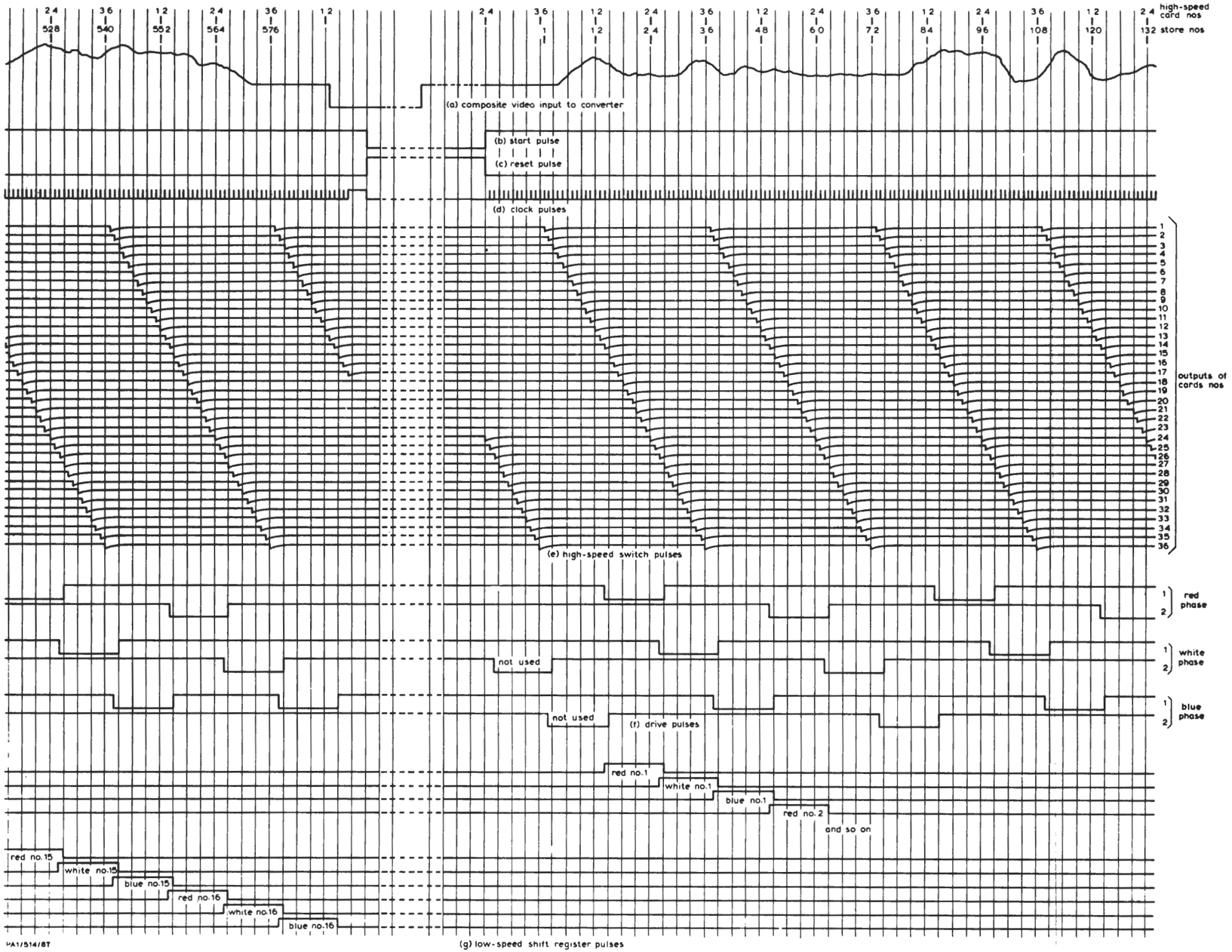

Fig. 8 Input Switching Waveforms

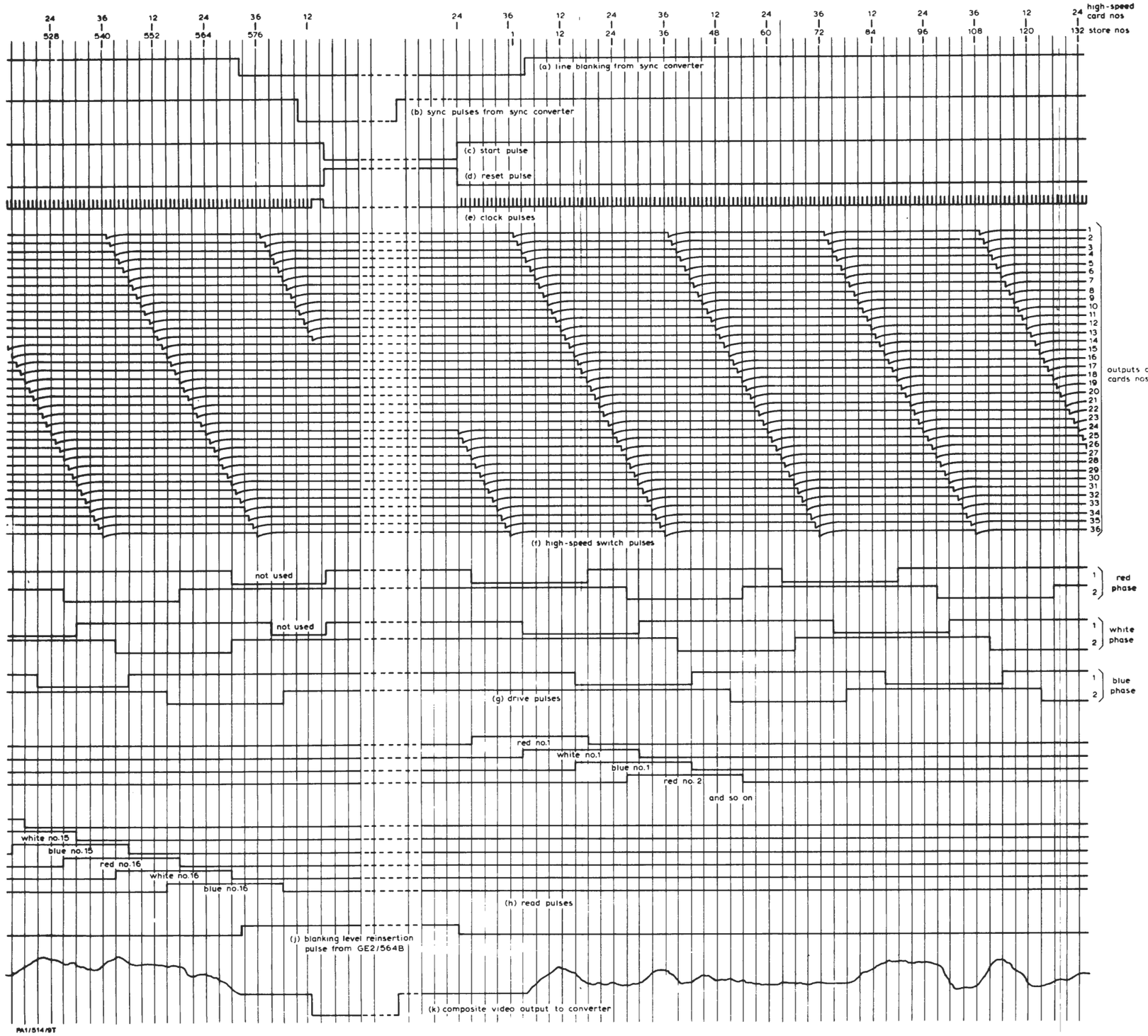

Fig. 9 Output Switching Waveforms