PULSED OSCILLATORS OS1/507 SERIES AND OS1/508 SERIES

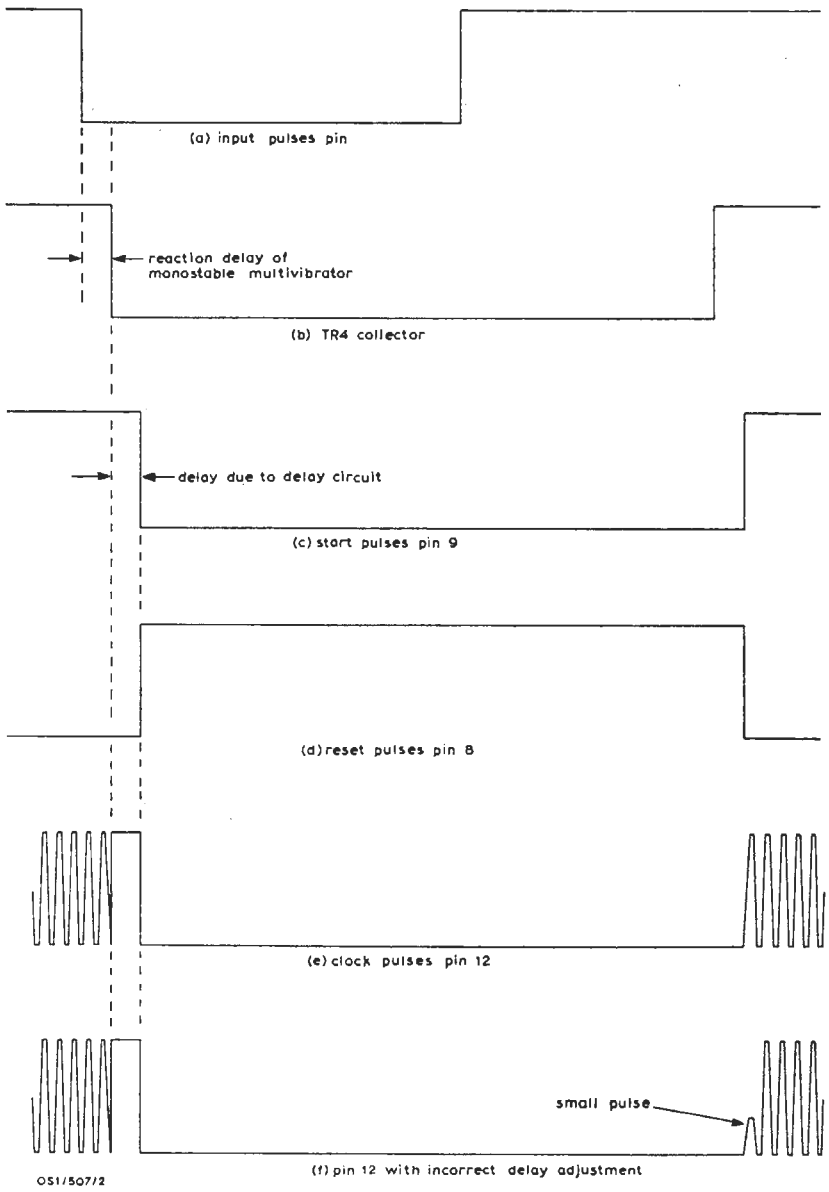

Fig. 1 Waveforms in the OS1/507 and OS1/508

Introduction

The OS1/507 and OS1/508 series of pulsed oscillators accept an input of line-frequency pulses: they produce a gated trapezoidal (clock pulse) output together with negative-going start pulses and positive-going reset pulses which start about 1 μs after the start of the input pulses. The duration of these pulses, shown in Fig. 1, is set to start the clock pulses during the back-porch period. Fine control of the trailing-edge timing of the pulses ensures that the first clock pulse is of full amplitude. The duration of these pulses and the frequency of the

clock pulses are given in Table 1. The OS1/508 also differs from the OS1/507 in that it has two identical clock pulse outputs.

TABLE 1

Oscillator	*Start and Reset Pulse Durations* (μs)	*Clock Pulse Frequency* (MHz)
OS1/507A	8	11
OS1/507B	13·8	7
OS1/508A	12·8	11
OS1/508B	7·2	9

These oscillators are constructed on CH1/12A chassis with index-peg positions 14 and 40.

General Description

A block diagram of the pulsed oscillators is given in Fig. 2. The input pulses trigger a monostable pulse generator to provide pulses of the required duration. These pulses, shown in Fig. 1(b), are fed to a gated oscillator to inhibit oscillation. The pulses are also fed via a delay stage to provide blanking pulses and the output start and reset pulses. The blanking pulses are fed to the clock-pulse output stages to remove the first few clock pulses during the onset of oscillation.

Circuit Description

The circuit of the pulsed oscillators, given in Fig. 3 on page 3, is conventional but the following points should be noted:

(a) A complementary monostable multivibrator circuit is used.

(b) A separate −6 volt supply rail is used for the oscillator and its inhibiting transistor TR6.

(c) The delay network is of the type with complex conjugate *m* values, described in Designs Department Technical Memorandum No. 9.91(61).

(d) Diode D19 is used to d.c. restore the blanking waveform.

(e) Complementary emitter followers are used as the output stages for both the clock pulses and the reset pulses.

Test Procedure

The pulsed oscillators are tested as part of their parent units.

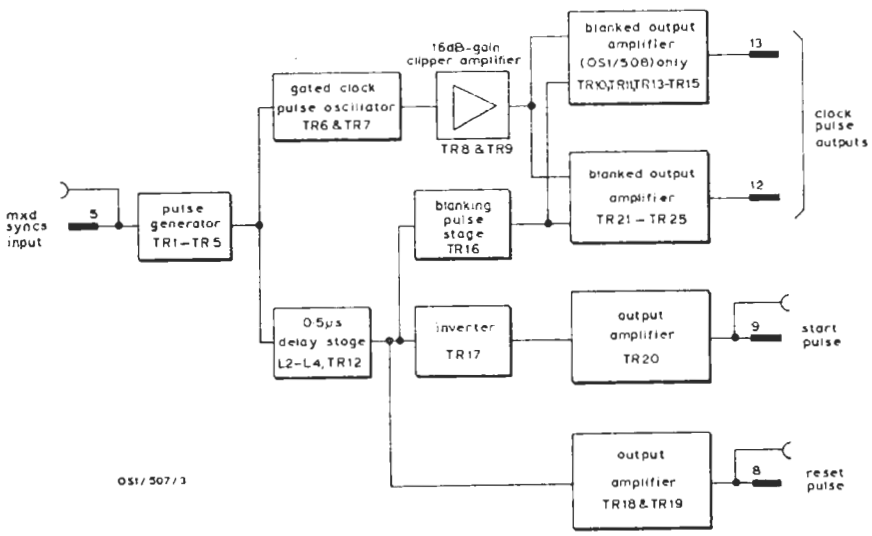

Fig. 2 Block Diagram of the OS1/507 and OS1/508

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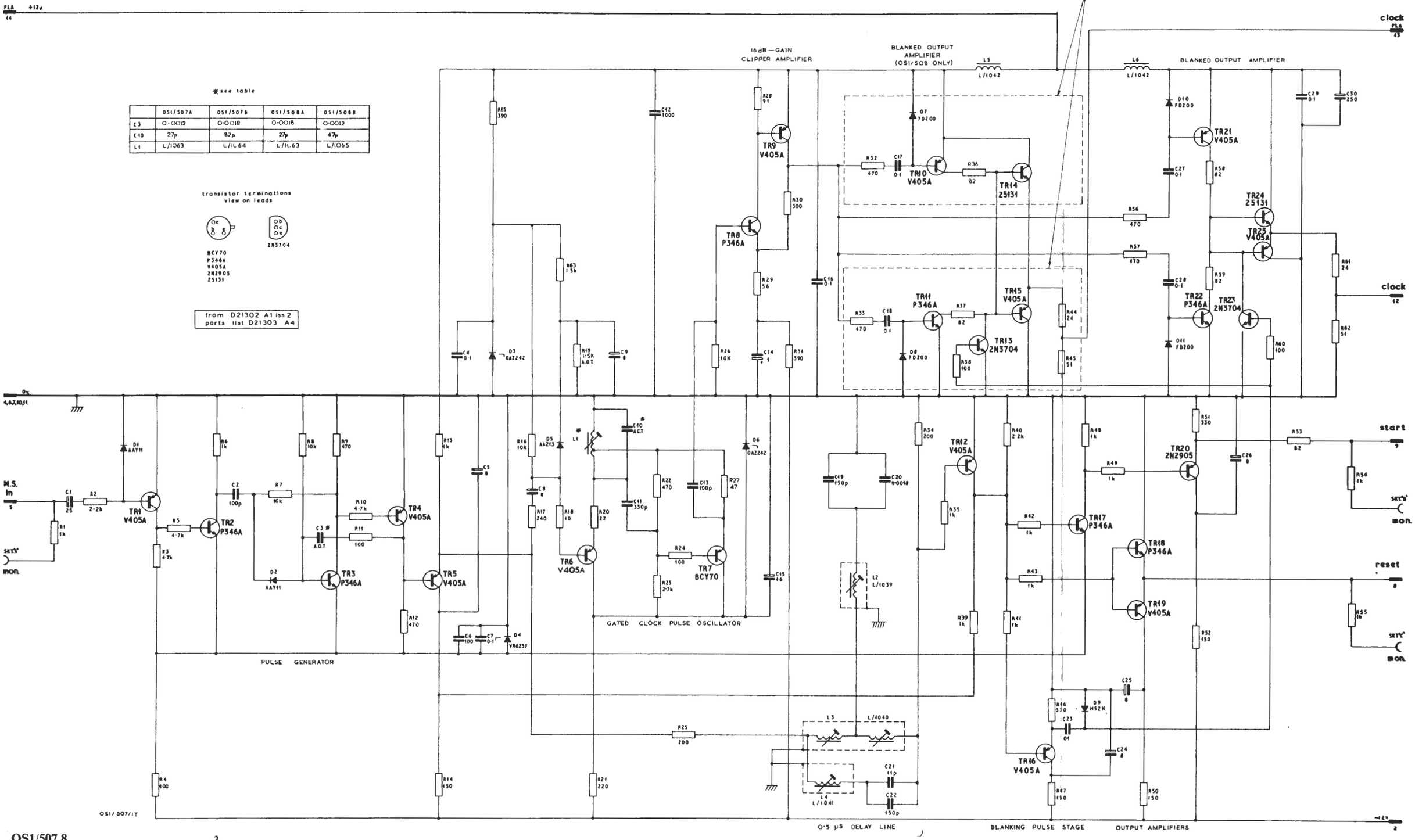

Fig. 3 Circuit of the OS1/507 and OS1/508