BURST LOCKED OSCILLATORS OS1/502 AND OS1/502A

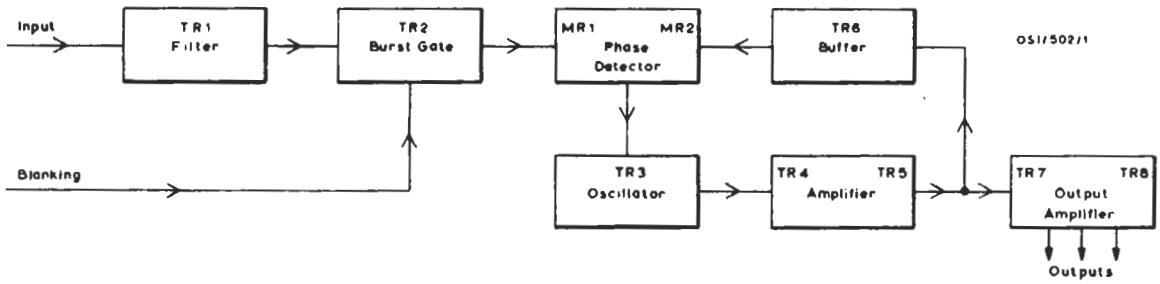

Fig. 1 Block Diagram of the OS1/502

Introduction

These units both accept a composite colour video signal and a back-porch gating pulse[1]; they both provide continuous subcarrier output signals of constant amplitude which have the same mean phase as the burst component of the input signal. The OS1/502 operates in the PAL mode with a swinging burst-phase, the OS1/502A operates in the NTSC mode with constant burst-phase.

The units continue to give subcarrier output signals when the input signals are removed. However, under these conditions the output frequencies and the rate of change of the output frequencies are not to PAL or NTSC specifications.

The units are mounted on a CH1/12A chassis with index-peg positions 9 and 25. Power supplies at +6 volts and −6 volts are required for the operation of the unit; a crystal oven requires a supply at either −18 volts or −6 volts[1].

General Specification

Inputs

Composite Video or Syncs plus Burst	burst component must be 0·3 V p-p ±6 dB
Gating Pulses	6 V p-p positive-going
Subcarrier Outputs	two at 1 V p-p one at 2 V p-p

Impedances

Inputs	high w.r.t. 75 ohms
Outputs	two at 75 ohms ±2% one high w.r.t. 75 ohms
Output Phase	same as input mean burst-phase

Output Frequency

OS1/502 (locked)	same as burst input
OS1/502 (unlocked)	4·4336187 MHz ±5 Hz
OS1/502A (locked)	same as burst input
OS1/502A (unlocked)	3·579545 MHz ±5 Hz

Oscillator Pull-in

OS1/502	± 40 Hz minimum
OS1/502A	± 100 Hz minimum

Oscillator Hold-in

OS1/502	± 150 Hz minimum
OS1/502A	± 350 Hz minimum

Crystal Oven Temperature	50 °C ±2 degrees

Signal-to-Noise Phase Error

OS1/502	0·5° at 20 dB r.m.s. s/n ratio
OS1/502A	1° at 20 dB r.m.s. s/n ratio

Phase Error/Temperature

OS1/502	0·35° over range 0—40 degrees C
OS1/502A	0·17° over range 0—40 degrees C
Operating Temperature	0 to 50 °C

Circuit Description

A block diagram is shown in Fig. 1 and the circuit diagram in Fig. 2. The block diagram applies to both units; the circuit diagram is basically that of a OS1/502 but the different phase-detector circuit used in the OS1/502A is

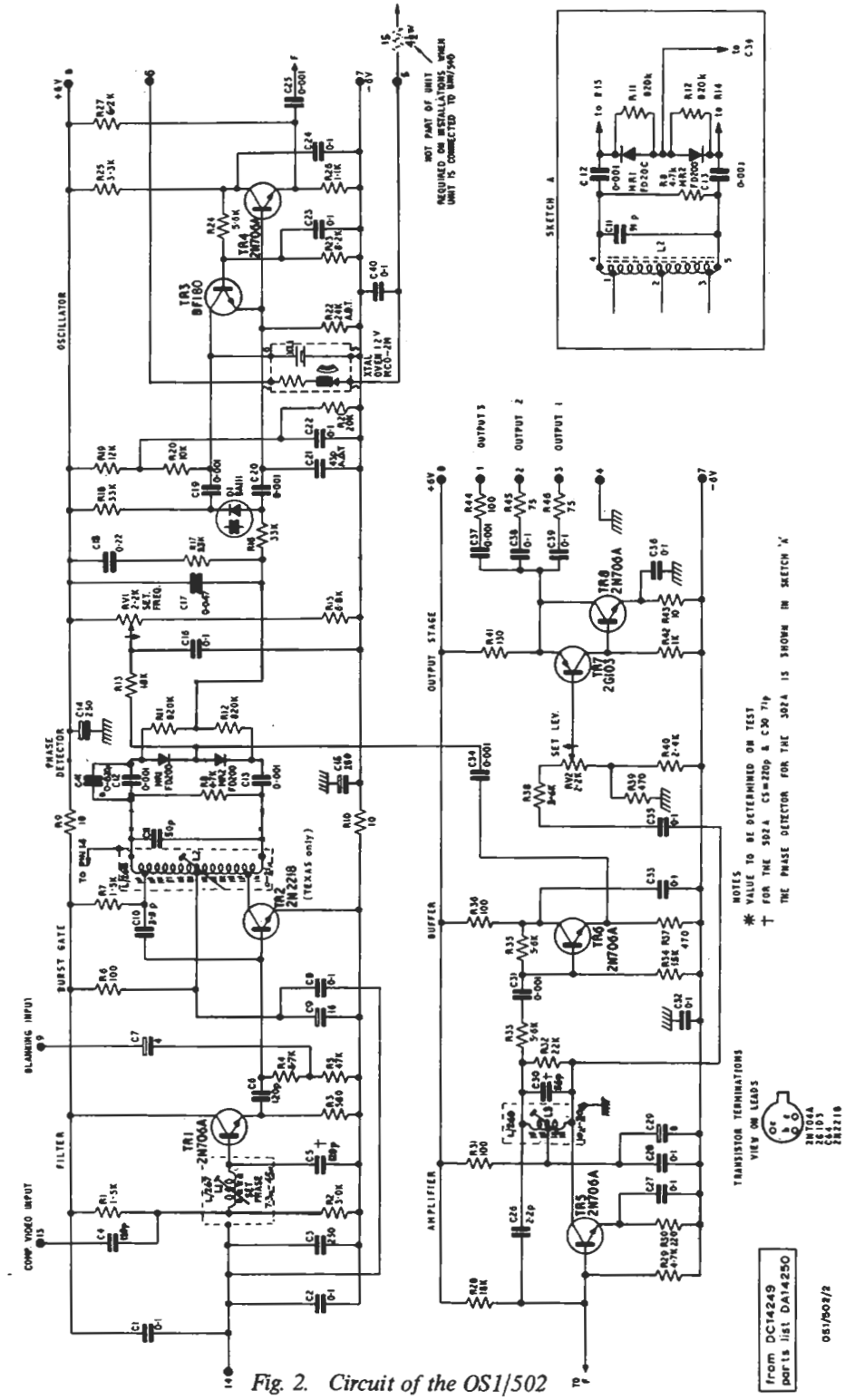

Fig. 2. Circuit of the OS1/502

given in an inset sketch. The description given below is valid for both units.

Burst Gate

The video input signal is applied to emitter-follower TR1 via a phase-shift and high-pass filter network comprising L1, C4, and C5. This network passes only chrominance information and the adjustable core of L1 provides a fine control of the overall phase delay at subcarrier frequency through the unit. From TR1 the chrominance signal is fed to the burst gate stage TR2. Transistor TR2 is normally cut off, but when positive-going gating pulses are applied to its base the transistor is driven into conduction and about 30 volts peak-to-peak of subcarrier signal is developed across L2 and applied to the phase detector. To prevent breakthrough of chrominance information during the picture period, a neutralising capacitor C10 is connected between L2 and the base of TR2.

Phase Detector

The subcarrier burst signal developed across L2 is applied in push-pull to the detector diodes MR1 and MR2 while the reference subcarrier signal is applied in quadrature to the junction of the diodes. The detector output consists of a d.c. component which is proportional to the phase error and an a.c. component at the error beat frequency. This signal is filtered by capacitors C17 and C18 before being applied to the oscillator stage; the a.c. to d.c. ratio, which controls the pull-in range of the oscillator, is determined by the value of R17.

Subcarrier Generator

Transistor TR3 functions as a crystal-controlled Colpitts oscillator in which the feedback path is via the variable-capacitance diode D1. The bias for D1 is obtained from the variable resistor RV1 which is connected in series with the phase-detector load; thus RV1 provides a fine frequency control. Transistor TR4 acts as a common-emitter feedback amplifier at d.c. and holds the operating point of the oscillator constant; at subcarrier frequency TR4 functions as a buffer emitter-follower and feeds the oscillator output to the following stage.

Transistor TR5 is a tuned amplifier and the signal amplitude developed across the collector load L3 is about 8 volts peak-to-peak. The signal appearing at the upper end of L3 is fed via the buffer emitter-follower stage TR6 to the junction of the phase-detector diodes, at which point it is in quadrature with the burst signal. Thus the subcarrier signal applied to the detector stage completes an automatic phase control loop[2] comprising the oscillator, the subcarrier amplifier and the phase detector.

Output Amplifier

The subcarrier signal developed at the collector of TR5 is fed via a variable resistor, which functions as a *Set Level* control, to the complementary output amplifier comprising transistors TR7 and TR8. Three outputs are taken from this stage; two of them have an output impedance of 75 ohms and provide a 1-volt peak-to-peak signal when terminated in 75 ohms, the third one provides a 2-volt peak-to-peak signal when feeding a high-impedance load.

Alignment

Tune L2 for maximum burst amplitude at TR2 collector then trim, within one turn, for coincidence of subcarrier and mean burst phase at pins 2 and 13 of connector, using an externally driven vectorscope with a 10:1 probe.

References

1. Sync Separator Unit UN1/540.
2. Designs Department Technical Memorandum 8/163 (64).

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