NATLOCK ERROR MONITOR MN1/509

Introduction

The MN1/509 accepts Natlock d.c. error signals produced in sync-timing and subcarrier-phase comparators and indicates any errors by means of lamps. If the error signals are such that sources being compared are non-synchronous a relay operates and lights an alarm lamp. A free change-over relay contact is provided to operate an external alarm. The alarm can be reset manually or automatically when synchronism is acheived. The unit can be switched to discount colour error signals when a monochrome source is being controlled.

The MN1/509 is constructed on a CH1/43 Chassis with index-peg positions 1, 2 and 15. An external d.c. supply of −12 volts at 350 mA is required to power the unit.

Specification

Input	
Fast, Advance, Retard error signals	from GE1L/532 Error Signal Generator
Colour error signal	from EP5L/505 or EP5M/506 Digital Phase Shifter
Input Levels	
Sync timing error signals	0V or −6V (nominal)
Colour error signals	0V, −3V or −6V (nominal)
Power Input	−12 volts at 350 mA (maximum) d.c.
Temperature Range	$0^{o}C$ to $45^{o}C$
Weight	0·34 kg (12 oz)

Design Philosophy

The error lamp circuitry is straightforward; its operation is described later.

The circuitry used to actuate the out-of-synchronism alarm uses a pair of type 9601 re-triggerable monostable integrated circuits. The logic diagram for the 9601 is shown in Fig. 1. The period of the monostable is set by the values of Cx and Rx. The monostable is triggered by the edge produced when inputs 1 or 2 go negative while inputs 3 and 4 are held positive or when inputs 3 and 4 go positive while inputs 1 or 2 are held negative. If the triggering edge recurs during the unstable period of the circuit the timing capacitor is rapidly reset and a new unstable period starts. A series of pulses arriving at a rate such that the time between pulses is less than the unstable period of the monostable will, therefore, produce a continuous output.

The presence of error signals at the inputs of the MN1/509 does not necessarily indicate that the source being controlled is non-synchronous. Even a so-called synchronous source requires occasional phase-shifting owing to the small but inevitable difference between the local and remote Natlock oscillators.

It has been decided that if an error signal persists for more than 0·7 seconds then the source, if supposedly synchronous, is sufficiently poor for an alarm to be given.

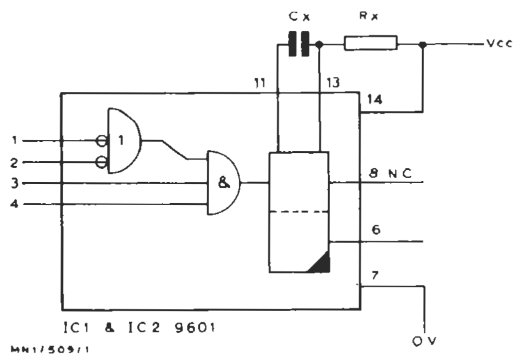

Fig. 1. Logic Diagram of 9601 Monostable Integrated Circuit

The appearance of an error signal is used to trigger a 0·7 s monostable. If the error is still present when the monostable returns to its stable state a bistable is triggered which operates the alarm relay. The 0·7 s monostable is re-triggerable so that if an error disappears and then reappears within 0·7 s the monostable is re-triggered.

Unfortunately a nominally continuous colour correction signal from the subcarrier phase comparator contains a 0·5-ms period without error signal every 40 ms caused by the resetting and sampling system used in the comparator. These 0·5-ms periods would keep re-triggering the monostable and so prevent the alarm ever being raised by a continuous colour correction signal.

This problem is overcome by using the termination of an error signal to trigger another monostable with a period of 7 ms. Thus every 40 ms when the colour error signal returns to zero the 7 ms monostable is triggered. The output of this monostable is used to inhibit the input to the 0·7 s monostable and so prevent it from being re-triggered by the 0·5 μs no-error periods.

The manual reset cancels the alarm and resets the 0·7 s monostable so that if it is operated when an error is present the alarm will be given again after 0·7 s.

Circuit Description

The circuit of the MN1/509 is shown in Fig. 2.

Error Lamp Circuits

The F', A' and R' error inputs are fed via emitter followers TR1, 4 and 7 to TR2, 5 and 8 which drive the F, A, and R lamps respectively. The lamp supply is fed via a 6-volt zener diode D1 which limits the lamp volts with the minimum of wasted power.

The circuits which drive the colour error lamps are more complicated because they must differentiate between –3 volts for a colour-retard instruction and –6 volts for a colour-advance instruction.

A colour-retard instruction (–3 volts) applied to emitter follower TR10 turns on TR11 and, provided TR12 is conducting, this will turn on TR13 and light LP4. By returning R21 to TR13 collector positive feedback is introduced which gives a Schmitt trigger action and speeds up the turn on of LP4. The emitter of TR10 is also connected to the base of TR15 via R28 and a 3·3-volt zener diode D2. The –3 volt signal at the emitter of TR10 is insufficient to break down D2 and so TR15 does not conduct. Hence TR14 does not conduct and LP5 is unlit. TR14 emitter is at about –6 volts which keeps TR12 hard on.

A colour-advance instruction (–6 volts) applied to emitter follower TR10 is sufficient to break down D2. This turns on TR15 which turns on TR14 and so lights LP5. When TR14 conducts its emitter approaches earth potential and so TR12 is switched off preventing LP4 from being lit.

When a monochrome signal is being controlled switch SA earths the base of TR10 which ensures that both colour-error lamps remain unlit.

Out-of-synchronism Detection Circuits

Waveforms for this part of the MN1/509 are shown in Fig. 3

Transistors TR3, 6, 9 and 16 amplify the error signals which are combined in the common load resistor R33. TR17 and TR18 form a Schmitt trigger which produces squared-up negative-going error signals at the collector of TR17 (waveforms a and b). TR17 switches between 0V and –5V regardless of which error signal is being received, so at TR17

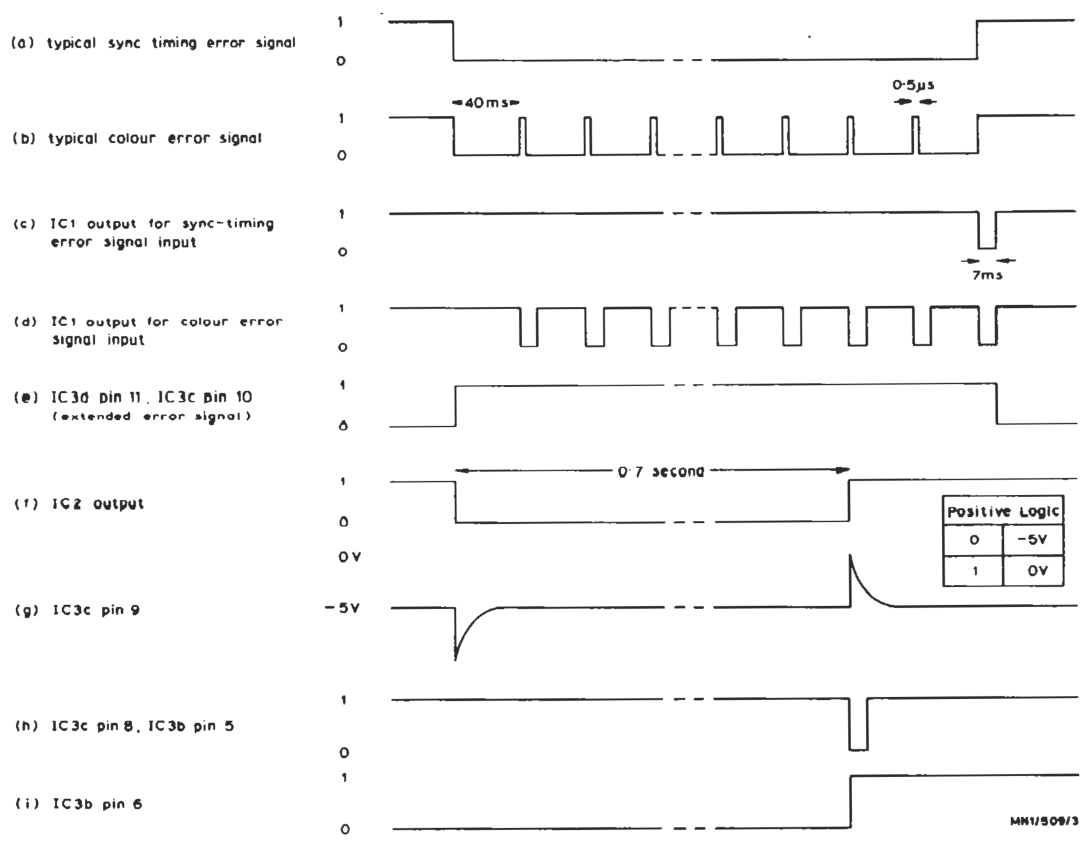

Fig. 3. Waveforms for Out-of-sync Detector

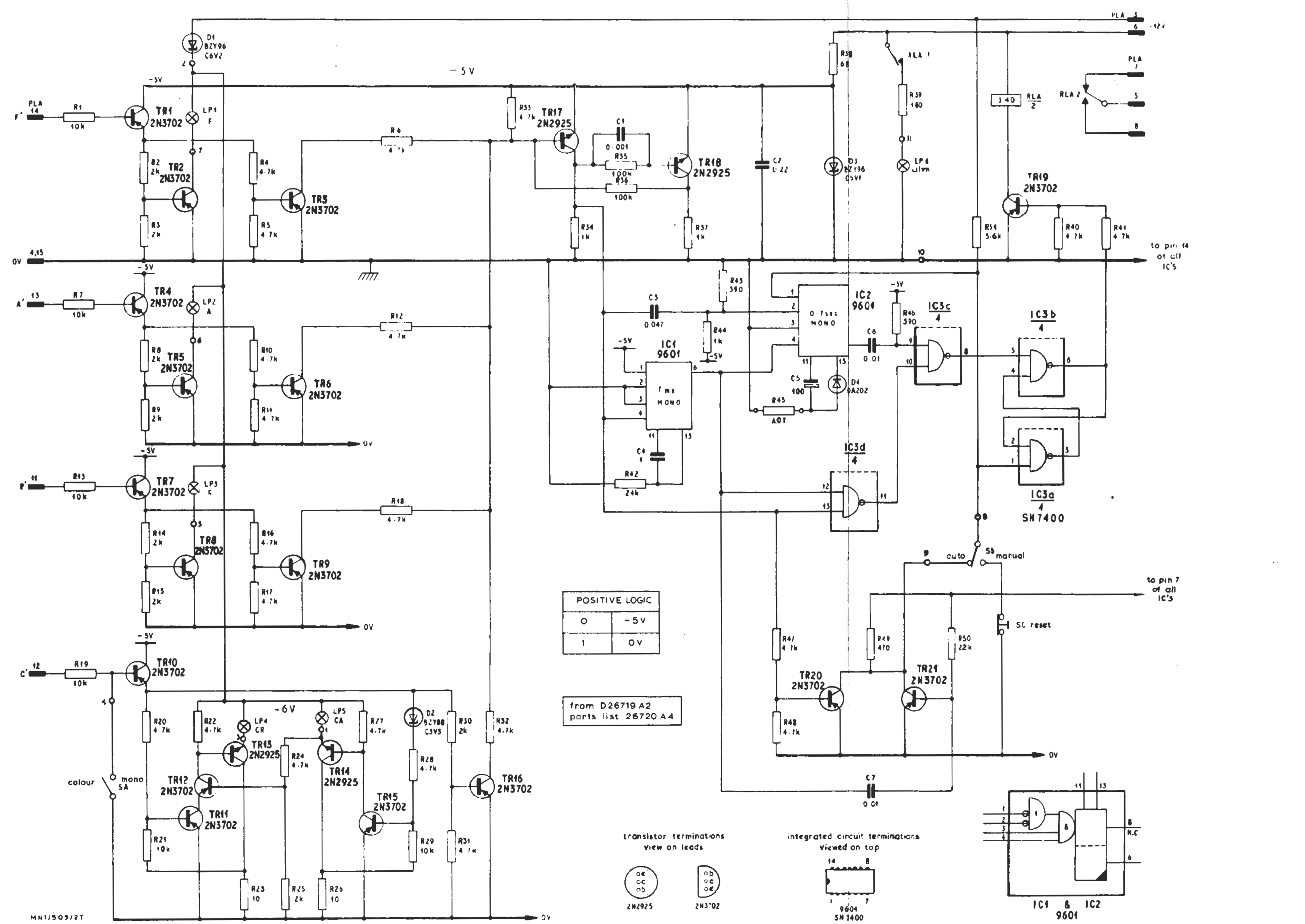

Fig. 2. Circuit of Natlock Error Monitor MN1/509

collector colour-advance and colour-retard instructions are of the same amplitude. The leading edge of the error signal at TR17 collector triggers the 0·7 s monostable IC2 on pin 2.

Inputs 1, 2 and 3 of the 7-ms monstable IC1 are tied to the appropriate supply rails so that IC1 is triggered solely on pin 4 by the trailing edge of an error signal at TR17 collector.

A sync-timing error signal applied to IC1 produces a single 7-ms pulse timed from the end of the error signal (waveform c). This 7-ms pulse plays no part in the operation of the system when a sync-timing error is being received. A colour error, however, has 0 to 1 transitions every 40 ms (waveform b) which re-trigger IC1 producing waveform (d), which is applied to pin 4 of IC2. This monostable circuit would be re-triggered by the 1 to 0 transitions of waveform (b) on pin 2 but, apart from the first, these always occur when waveform (d) on pin 4 is in the 0 state. With a 0 state on pin 4 the monstable cannot be re-triggered and hence for a colour-error input IC2 is triggered only by the first 1 to 0 transition on pin 2.

The error signal from TR17 collector and the output of IC1 are applied to a two-input NAND gate IC3d. The output of this gate is a single positive-going pulse (waveform e) which lasts for the duration of the error signal plus 7 ms regardless of whether a colour error or sync-timing error is being received. This pulse is applied to one input of another NAND gate IC3c.

The 0·7 s negative-going pulse (waveform f) from IC2 is differentiated by C6 and R46 to give waveform (g) which is applied to the other input of IC3c. If the positive going spike of waveform (g) occurs whilst the extended error signal (waveform e) from IC3d is present IC3c gives out a negative going pulse (waveform h). This sets IC3b output into the 1 state which turns off TR19, de-energises the relay and lights the alarm lamp.

IC3a and IC3b are cross-connected to form a set-reset bistable which is reset by a 0 state on pin 1 of IC3a. This point is earthed (1 state) in the *Manual* condition, but when the *Reset* push is operated it is connected to −12 volts via R51. This resets the output bistable which turns on TR19 and pulls in the relay, thereby extinguishing the alarm. It also re-triggers the 0·7 s monostable on pin 1.

In the *Auto* condition the reset input of the bistable is connected to the NAND gate formed by TR20 and TR21. During the period of the extended error signal (waveform e) at least one of these transistors is conducting thereby earthing the reset line. During this period the bistable can be set by a negative pulse from IC3c.

TR20 stops conducting when error signals cease and TR21 stops conducting at the end of the 7-ms period; thus at the end of the extended error signal both transistors are turned off and the reset line drops to −5 volts. This resets the output bistable and re-triggers the 0·7 s monostable.

Diode D4 (connected to pin 13 of IC2) prevents reverse biasing of C5.

A simplified logic diagram of the MN1/509 is shown in Fig. 4.

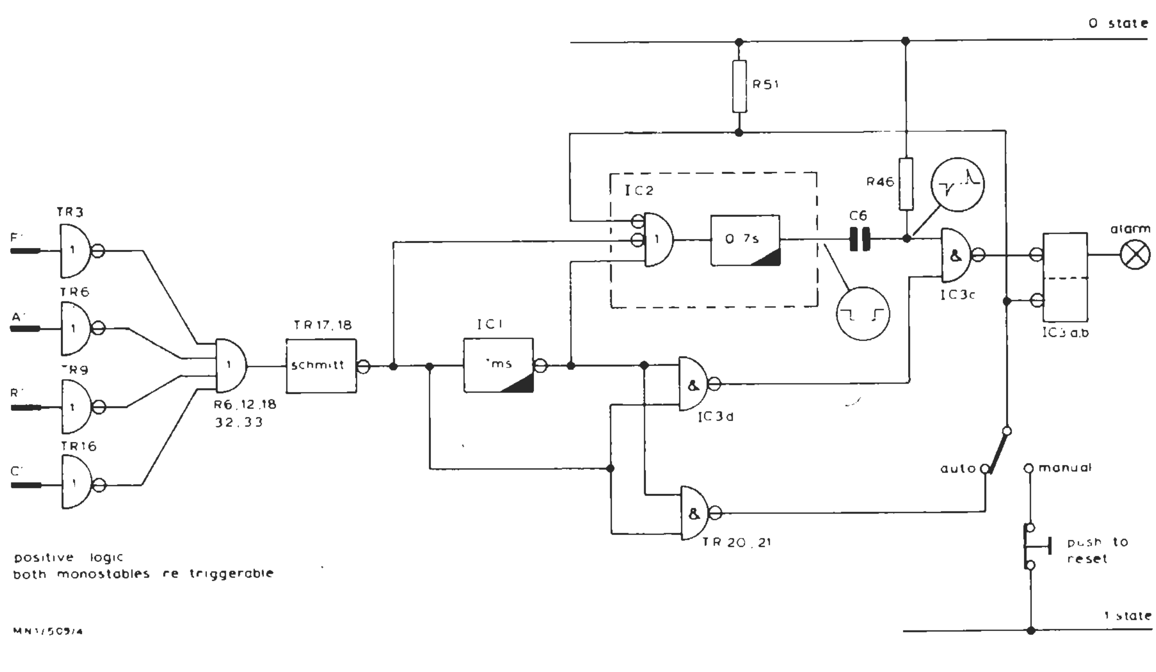

Fig. 4. Logic Diagram for Out-of-sync Detector

Testing the MN1/509

Apparatus Required

12-volt 400-mA d.c. supply.
1-kilohm ¼-watt potentiometer.
AVO Meter.
Dual-trace Oscilloscope with two probes.
Pulse Generator to give 6-volt negative-going square wave at 1Hz to 100 Hz.
Painton 15-pole socket.

Procedure

Voltages and times are ±10% tolerance unless otherwise stated. All voltages are measured relative to PLA15 (chassis).

1. Set front-panel switches to *Manual* and *Colour*.
2. Connect the 12-volt supply to the 15-way socket with pins 3 and 6 negative and pins 4 and 15 positive. The current drawn should be about 160 mA if the alarm lamp is lit and 150 mA if not.
3. Connect the 1-kilohm potentiometer across the 12-volt supply and set the slider to zero volts. Connect the AVO between the slider and chassis.
4. Connect the potentiometer slider to pin 14 of the Painton socket. Gradually increase the volts at pin 14. The *F* lamp should light before pin 14 reaches −1·5 volts.
5. Repeat step 4 with the slider connected to (a) pin 13 when the *A* lamp should light and (b) pin 11 when the *R* lamp should light.
6. Set the potentiometer slider to zero volts and connect it to pin 12 of the Painton socket. Gradually increase the volts at pin 12. The *CR* lamp should light at about −1·5 volts. At about −3·3 volts the *CR* lamp should extinguish and the *CA* lamp light.
7. Switch to *Monochrome* and check that both lamps are extinguished. Switch back to *Colour*.
8. Set the Pulse Generator to give a 20-Hz square wave and connect it to pin 14 of the Painton socket. To operate the MN1/509 the Generator must produce pulses which swing over the range 0 to −5 volts. With a Generator producing only a positive or balanced output it is necessary to d.c. restore the square wave before application to the MN1/509. Check with the oscilloscope that the correct pulses are being applied.
9. Connect one oscilloscope probe to the collector of TR17. Check for a 5-volt square wave.
10. Connect the other oscilloscope probe to pin 6 of IC1. Check for a 4-volt negative pulse of duration 6 to 10 ms starting from the positive going edge of each square wave at the collector of TR17.
11. Connect an oscilloscope probe to pin 6 of IC2. This should be at −5 volts. Remove the square-wave input and the potential at pin 6 should rise to zero volts within 1 second.
12. Set the Pulse Generator to give a 1−Hz square wave. Switch the MN1/509 to *Auto* reset. The alarm lamp should not light.
13. Increase the repetition rate of the square wave. The alarm lamp should light when the duration of the positive portion of the input signal is less than the unstable period of IC1. This should occur at a repetition rate of about 50 to 80 Hz.
14. Repeat step 13 with the input connected to pin 13 and then pin 14 of the Painton socket.
15. Connect the Generator to pin 12 of the Painton socket and reduce its output to 2 volts. Repeat step 13.
16. Apply −5 volts to pin 14 of the Painton socket. The alarm lamp should light after about 0·7 s. Disconnect the −5 volts and the alarm should cancel immediately.
17. Re-apply −5 volts to pin 14 of the Painton socket, switch to *Manual* reset and press the *Reset* push-button. The alarm should cancel, but light again after 0·7 s.

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