MONITOR LINE-UP ('MONLUGE') GENERATOR GE4/543 (GE4/548)

INTRODUCTION

The GE4/543 provides test signals for lining up monochrome and colour picture monitors. It accepts mixed syncs, burst gate and PAL subcarrier and produces the following outputs simultaneously:

(i) Standard (2-step) Pluge waveform
(ii) Greyscale (4-step) Pluge waveform
(iii) Convergence Grille (wide spacing)
(iv) Linearity Grille (fine spacing)
(v) Variable Lift
(vi) Linear 10-level Line Stepwedge
(vii) Linear Line Sawtooth.

All outputs are composite and each output includes a colour burst. The generator is self-powered containing an integral (modified) PS2/83 supplier.

The line sawtooth output can be made non-composite by altering the position of an internal link in the Generator. This link is located on printed board No. 4.

CONSTRUCTION

The Generator is constructed on seven printed wiring cards which are housed in a CH1/59C chassis occupying a C-size space (equal to three standard units). The seven cards and CH1/59C Chassis are together coded GE4/548. The GE4/543 comprises these items plus a back box consisting of a modified PN3A/37C into which the CH1/59C plugs. Mains, inputs and outputs are routed to the Generator via appropriate connectors mounted on the rear of the PN3A/37C back box.

The front panel of the CH1/59C hinges down to reveal the printed wiring boards of which five plug in and are labelled 1 to 5 from right to left. The sixth board houses the power supply and is mounted on the hinged side of the chassis to the right of the plug-in boards. The seventh board, a so-called Interconnection Board, is mounted behind the plug-in board and provides the necessary interconnections between these. The only components mounted on the Interconnection Board are a few decoupling capacitors, a pair of zener diodes associated with the power supply, and the sockets into which the plug-in boards fit. The boards are designated as follows:

Board 1	Line Board
Board 2	Combining Board
Board 3	Field Board
Board 4	Output Board
Board 5	Black Level Generator
Board 6	Power Supply
Board 7	Interconnection Board

An extender board type CH1A/13 is required to gain access to the components on the plug-in boards whilst the Generator is operating.

GENERAL SPECIFICATION

General

Mains Supply	210 to 260 V, 50 Hz.
Power Consumption	170 mA at 240 V a.c. 50 Hz.
Operating Temperature Range	5°C to 45°C.
Weight including Back Box	4·1 kg (9 lb 8 oz) approx.
Crosstalk and Noise rejection on all output signals	better than 40 dB p-p.

Input Signals

Mixed Syncs	2 V p-p ± 6 dB into 3 kΩ approx.
Burst Gate	2 V p-p ± 6 dB into 3 kΩ approx.
PAL Subcarrier	1 V p-p ± 3 dB into 75 Ω

Output Signals

These are listed in the introduction and are all 1 volt p-p composite from an impedance of 75 Ω. Output waveforms are standard with the exception that field blanking starts half a line early at the end of second fields and ends half a line late at the start of first fields. Consequently the familiar half line of video information at the end of each second field and at the start of each first field is absent on all outputs. Precise details of output signals are given below.

Pluge

Pulse Amplitudes

Pedestal level	0·02 V ± 2 mV
Black pulse	0·02 V ± 2 mV below pedestal level
Dark Grey pulse	0·02 V ± 2 mV above pedestal level
Peak White pulse	0·7 V ± 20 mV above black level
Grey pulse	0·47 V ± 20 mV above black level

Pulse Widths

Black pulse	2·33 μs ± 50 ns
Dark Grey pulse	2·33 μs ± 50 ns
Peak White pulse	21 μs ± 200 ns
Grey pulse	21 μs ± 200 ns

Rise and Fall Times
- Blanking: 250 ns ± 50 ns
- All other pulses: 100 ns ± 40 ns

Output Impedance: 75 ohms ± 2%

Grey Scale Pluge

Pulse Amplitudes
- Pedestal level: 0·02 V ± 2 mV
- Black pulse: 0·02 V ± 2 mV below pedestal level
- Dark Grey pulse: 0·02 V ± 2 mV above pedestal level
- Peak White pulse: 0·7 V ± 20 mV above black level
- 1st Grey pulse: 0·448 V above black level adjustable range ± 80 mV
- 2nd Grey pulse: 0·21 V above black level adjustable range ± 80 mV
- 3rd Grey pulse: 0·112 V above black level adjustable range ± 50 mV

Pulse Widths
- Black pulse: 2·33 μs ± 50 ns
- Dark Grey pulse: 2·33 μs ± 50 ns
- Peak White pulse: 11·66 μs ± 100 ns
- 1st Grey pulse: 11·66 μs ± 100 ns
- 2nd Grey pulse: 11·66 μs ± 100 ns
- 3rd Grey pulse: 11·66 μs ± 100 ns

Rise and Fall Times
- Blanking: 250 ns ± 50 ns
- All other pulses: 100 ns ± 40 ns

Output Impedance: 75 ohms ± 2%

Linearity Grille (23 x 23 bars)

Pulse Amplitudes: 0·7 V ± 15 mV

Vertical Pulse Widths: 270 ns ± 50 ns

Horizontal Pulse Widths: 1 Line per field

Rise and Fall Times: 100 ns ± 40 ns

Output Impedance: 75 ohms ± 2%

Linear Stepwedge (10-level)

Waveform Amplitude: 9 steps each of 0·078 V; 10th level 0·7 V ± 35 mV

Preset Adjustment Range: at least ± 7%

Step Amplitude Non-linearity: less than 1%

Rise and Fall Times
- Step Risers: 120 ns ± 30 ns
- Blanking: 200 ns ± 50 ns

Output Impedance: 75 ohms ± 2%

Convergence Grille (11 x 9 bars)

Pulse Amplitudes: 0·7 V ± 15 mV

Vertical Pulse Widths: 270 ns ± 50 ns

Horizontal Pulse Widths: 1 Line per field

Rise and Fall Times: 100 ns ± 40 ns

Output Impedance: 75 ohms ± 2%

Sawtooth

Waveform Amplitude: 0·7 V ± 10 mV

Preset Adjustment Range: at least ± 7%

Non-linearity: less than 1%

Rise and Fall Times: Blanking 200 ns ± 50 ns

Output Impedance: 75 ohms ± 2%

Variable Lift

Waveform Amplitude: Variable 0 to 0·7 V

Rise and Fall Times: Blanking 250 ns ± 50 ns

Output Impedance: 75 ohms ± 2%

Mixed Synchronising Pulses, Blanking and Colour Burst Specification for all Output Waveforms

Mixed Synchronising Pulse Width: Same as input mixed synchronising pulse width ± 100 ns

Mixed Synchronising Rise and Fall Time: 250 ns ± 50 ns

Mixed Synchronising Pulse Amplitude: 300 mV ± 15 mV

Front Porch Width: 1·65 μs ± 250 ns

Line Blanking Width: 12·05 μs ± 250 ns

Field Blanking Width: 25 lines + line blanking for second fields; 25 lines + line blanking for first fields (no half-line waveforms generated)

Burst Amplitude	300 mV ± 15 mV
Burst Start Timing	5·6 μs ± 100 ns from leading edge of line synchronising pulse
Burst Duration	2·25 μs ± 230 ns (10 ± 1 cycles)
Burst Rise Time	250 ns ± 50 ns
Residual Subcarrier on the active line	less than 3 mV p-p
Burst Blanking	as specified for system I 625 line PAL
Relative phase relationship between Bursts on the seven Output Waveforms	**Random**

TEST PROCEDURE

General

Each GE4/543 is aligned on manufacture and because of the inherent reliability of the integrated circuits used the likelihood of further periodic alignment being required is remote, even after a period of years in service. However in the event of components being replaced to repair a fault the small possibility exists that one or more of the output waveforms may change slightly in terms of amplitude or timing. For this reason a comprehensive line-up procedure for the Generator is given in this instruction and it should be used in conjunction with Table 1.

The table indicates the paragraphs of the line-up procedure and the section of the handbook relevant to particular waveforms being out of specification in terms of amplitude or timing. Before making any adjustments check that the power supply is providing the correct voltages.

Whilst a complete line-up of the Generator is possible using the procedure given in this instruction it is envisaged that this will be required only in exceptional circumstances.

Test Equipment Required

1. Oscilloscope with dual-trace high-gain pre-amplifier and two X10 oscilloscope probes. (N.B. for some measurements a single channel low-gain preamplifier is sufficient.)
2. Extender card type CH1A/13.
3. Variable attenuator, 75 Ω, 0 to 0·9 dB in 0·1-dB steps (STC type 74600).
4. Variable attenuator, 75 Ω, 0 to 9 dB in 1-dB steps (STC type 74600).
5. Switchable Subcarrier Rejection Filter FL1/514.
6. Monochrome Picture Monitor.
7. Signal Measuring Unit UN1/511.
8. Non-linearity Filter FL1/509B.
9. Variable **Capacitors** covering the ranges 4 to 40 pF and 4 to 100 pF (e.g. Mullard types 809-07008 and 809-07015).
10. Capacitor bridge covering the range 4 to 100 pF.
11. Miniature carbon potentiometers (for assessing values of A.O.T. resistors) covering the following ranges:
    100k, 68k, 33k, 20k, 15k, 10k, 2·2k.
    (N.B. for any one measurement only one or two of these will be required. In general select a potentiometer approximately twice the value of the A.O.T. resistor value quoted on the circuit diagram.)
12. PAL Vectorscope: Tektronix type 526 or equivalent.
13. AVO or Digital Multimeter e.g. Advance type DMM2.

Alignment Procedure

Note: TP = Test Point.

1. Field Board (board No. 3)

1. Monitor TP.A and the Mixed Syncs input with the oscilloscope. If necessary A.O.T. R8 to make the H.A.D. of the pulses at TP.A within 50 ns of that of the line sync pulses.

2. Line Board (board No. 1)

1. Monitor TP.A and the Mixed Syncs input with the oscilloscope. Adjust the oscilloscope controls so that the whole of the line sync pulse is visible on one trace and the last circulating pulse of one line and first of the next are visible on the other.
2. Adjust R28 to make the time between the last circulating pulse on one line and the first on the next $3\frac{1}{3}$ μs.

3. Black Level Generator (board No. 5)

1. Monitor waveform at TP.L. Displayed pulses should be symmetrical. If necessary A.O.T. R58 to improve symmetry and to reduce overshoots to below 12 mV.
2. Monitor **waveforms at TP.A** and **TP.B**. If necessary A.O.T. R8 to make the H.A.D. of the pulses at TP.B within 50 ns of that of the pulses at TP.A.
3. Monitor waveform at TP.J. Displayed pulses should be symmetrical. If necessary A.O.T. R13 to improve symmetry and to reduce overshoots to below 12 mV.

TABLE 1

Amplitude and Timing Adjustments in the GE4/543

Parameter out of specification	*Relevant paragraphs of line-up procedure*	*Relevant Circuits (Fig. Nos.)*	*Equipment required for re-alignment (this is itemised opposite)*
Sync amplitude incorrect on all outputs	3 (9 & 10)	19	1,2,7,11
Burst amplitude incorrect on all outputs	3 (11)	21	1,2,7,11
Burst amplitude incorrect on one or more, but not all, outputs	4 (1 & 7)	24,25,26, 27,28	1,2,7,9,10
Pluge output level incorrect	5 (1,6,7,8)	15	1,2,3,4,7,11
Greyscale Pluge output level incorrect	5 (9,10,11)	15	1,2,7,11
Sawtooth output level incorrect	4 (1,5) and 5 (1,2)	28 16	1,2,7,11
Stepwedge output level incorrect	4 (1,6) and 5 (1,3,4,5)	28 17	1,2,7,9,10,11
Linearity Grille output level incorrect	4 (1,2)	26	1,2,7,11
Convergence Grille output level incorrect	4 (1,3)	24	1,2,7,11
Variable Lift maximum output level incorrect	4 (1,4)	27	1,2,7,11
Burst 90° incorrect	3 (1,2,3,4,5, 6,7,8)	19,20,21,22	1,2,5,11,12
Front Porch duration incorrect	6 (1,2,3,4)	7	1,2
Line Blanking duration incorrect	6 (1,5,6)	7	1,2
Linearity Grille not central on raster	6 (1,7,8)	7	1,2,6,9,10
Carrier Balance Incorrect	3 (4,5)	21,22	1,2,5

4. Set up the arrangement of Fig. 1a.
5. Switch the filter out of circuit and adjust R73 and R39 for minimum subcarrier along the active lines. Switch the filter into circuit and adjust C50 and C51 for maximum rejection of 2nd and 3rd harmonics.
6. Disconnect the lead from the filter input and connect it to the vectorscope input. Parallel the feeds of subcarrier to the GE4/543 and the vectorscope. Obtain a display of the switched subcarrier and adjust R29 to obtain 90° between the two vectors. The amplitudes of the two vectors should be the same ± 3%.

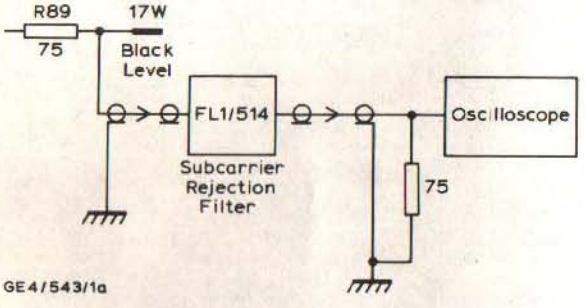


Fig. 1a Circuit for adjusting Subcarrier Harmonic Rejection

7. Repeat Step 5. The residual subcarrier on each active line should now be less than 1 mV p-p.
8. Switch the filter out of circuit and A.O.T. R98 to obtain the best burst shape. Note that the burst and sync pulses as observed at edge connection 17 W are about 6 dB down on normal level.
9. Disconnect the arrangement of Fig. 1a and set up the arrangement of Fig. 1b.
10. Use the UN1/511 to measure the sync pulse amplitude at the output of the Generator (set the UN1/511 to *Measure Sync*). If necessary A.O.T. R92 to make the sync pulse amplitude 300 mV ± 0·1 dB.
11. Transfer the UN1/511 input lead from the stepwedge output to the Linearity Grille output. Measure the burst amplitude using the UN1/511 set to the *Measure Sync* position. This measurement must be made with all cards plugged directly into the chassis: an extender board must not be used. If necessary A.O.T. R97 to make the burst amplitude 300 mV ± 0·1 dB.

4. Output Board (board No. 4)

1. Fit the Output Board (board 4) on to the extender board.
2. Use the UN1/511 to measure the amplitude of the Linearity Grille output (set the UN1/511 to *Measure Picture*). If necessary A.O.T. R1 to make the Linearity Grille amplitude 700 mV ± 0·1 dB.
3. Use the UN1/511 to measure the amplitude of the Convergence Grille output. If necessary A.O.T. R8 to make the Convergence Grille amplitude 700 mV ± 0·1 dB.
4. Transfer the UN1/511 input lead to the Variable Lift output. Set R69 (the lift adjustment control) to give maximum lift. If necessary A.O.T. R61 to make the maximum lift 0·7 mV ± 0·1 dB.
5. Transfer the UN1/511 input lead to the Sawtooth output. Switch the UN1/511 to *Signal*, the oscilloscope input to *d.c.* and measure the steady voltage of the back porch. If it is more than 200 mV from 0 V A.O.T. R48 to bring it as close as possible to 0 V; preferably within 50 mV to allow for possible future drift.

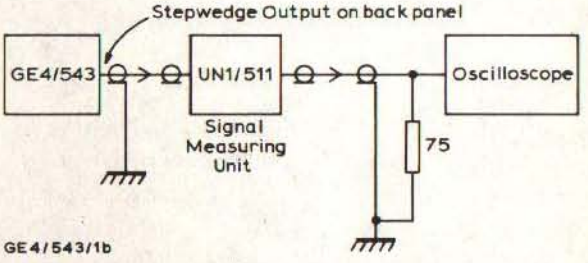


Fig. 1b Circuit for Amplitude Adjustments

6. Transfer the UN1/511 input lead to the Stepwedge output and repeat step 5 adjusting A.O.T. resistor R58 instead of R48.

Continued overleaf

7. Remove the extender board and put the Output Board back into the chassis then use the UN1/511 to measure the burst amplitude on each output in turn. If necessary A.O.T. capacitors as indicated in the table below to make the burst amplitude 300 mV ± 0·1 dB.

TABLE 2

Adjustment of Burst Amplitude

Output Signal	*A.O.T. Capacitor to be adjusted*
Stepwedge	C33
Variable Lift	C38
Pluge	C25
Greyscale Pluge	C19
Sawtooth	C49 if burst amplitude is too low C28 if burst amplitude is too high

5. Combining Board (board No.2)

1. Fit the Combining Board (board 2) on to the extender chassis.
2. Use the UN1/511 to measure the sawtooth amplitude and if necessary adjust R14 (a variable resistor) to obtain a sawtooth amplitude of 0·7 V ± 0·05 dB. If this cannot be achieved by adjustment of R14 it will be necessary to A.O.T. R15.
3. Transfer the UN1/511 input lead to the Stepwedge output and set the UN1/511 to *Signal.*
4. Measure the risetime of the stepwedge risers and if necessary A.O.T. C5 to obtain a risetime of 120 ± 30 ns.
5. Switch the UN1/511 to *Measure Picture* and adjust R35 (a variable resistor) to set the stepwedge amplitude to 0·7 V ± 0·05 dB. If this cannot be achieved by adjustment of R35 it will be necessary to A.O.T. R34.
6. Transfer the UN1/511 input lead to the Pluge output. Measure the amplitude of the peak white pulse and if necessary A.O.T. R105 to bring it to 0·7 V ± 0·1 dB.
7. Connect the two 75-ohm step attenuators in series with the input of the UN1/511 and set them to give an attenuation of 3·9 dB. This reduces the level of the grey pulse from 0·47 V to 0·3 V. The level of this pulse can now be checked using the UN1/511 set to the *Measure Sync* position. If the attenuated grey pulse is more than 0·05 dB from 0·3 V A.O.T. R110 to bring it within this range.
8. Remove the attenuators from the circuit and switch the UN1/511 to *Signal*. Measure the amplitudes of the black pulse and the dark grey pulse on the oscilloscope and if necessary A.O.T. R89 (for the black pulse) and R101 (for the dark grey pulse) to bring them to 0·02 V ± 2 mV.
9. Transfer the UN1/511 input to the Greyscale Pluge output. Use the UN1/511 set to *Measure Picture* to measure the amplitude of the peak white pulse. Set this to 0·7 V ± 0·1 dB by adjusting A.O.T. resistor R72.
10. Switch the UN1/511 to *Signal* and use the oscilloscope to measure the amplitudes of the grey bars on the Greyscale Pluge output. Adjust variable resistors in accordance with table 3 to obtain the correct levels for the grey bars.

TABLE 3

Adjustment of Grey-bar Amplitude

Bar	*Resistor to be adjusted*	*Level (volts from Black level)*
1st (light) grey bar	R116	0·45
2nd grey bar	R121	0·21
3rd (dark) grey bar	R128	0·11

11. Measure the amplitude of the black pulse and dark grey pulse and if necessary A.O.T. R102 and R103 respectively to bring them to 0·02 V ± 2 mV.

6. Timing Adjustments

1. Fit the Line Board (board 1) on to the extender chassis.
2. Connect the terminated oscilloscope to the variable lift output and set the lift to about 50%..
3. Measure the width of front porch and record its value. Subtract this figure from the correct width which is 1·65 μs.
4. If the result is positive move tap B on the pulse circulation delay line one or more taps nearer to the delay line input, i.e. reduce the delay. If the result is negative move tap B one or more taps nearer to the delay line output, i.e. increase the delay. The difference in delay between each tap is 50 ns and so it is possible to set the width of the front porch to within 50 ns, which is the required setting accuracy. Fig. 2 identifies tap B and shows which way to move it to increase the delay.
5. While displaying the Variable Lift output measure the width of the line blanking period and record its value. Subtract this figure from the correct width which is 12·05 μs.
6. If the result is negative move tap C on the pulse circulation delay line one or more taps nearer to the delay line input, i.e. reduce the delay. If the

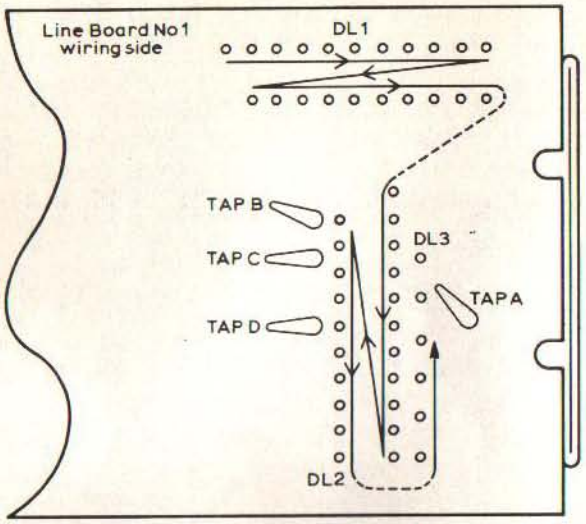


Fig. 2 Delay Line Tap Designations

result is positive move tap C one or more taps nearer to the delay line output, i.e. increase the delay. Fig. 2 identifies tap C and shows which way to move it to increase the delay.

7. Transfer the terminated oscilloscope input lead to the Linearity Grille output. Select one of the 23 pulses (other than the first or last) which form the verticals of the grille waveform and measure its H.A.D. If necessary A.O.T. C3 to make the H.A.D. 270 ns ± 20 ns.

8. Feed the Linearity Grille output to a monochrome picture monitor. Underscan the monitor so that the right and left hand edges of the raster are visible. Adjust the position of tap D on the pulse circulation delay line to centre the grille within the raster. This is most easily achieved by setting tap D for equal blips at the beginning and end of each horizontal line of the grille.

JRWC 5/73

MAINTENANCE

Although the circuitry of the GE4/543 is complex the design is such that many sections of the device each perform a function which is necessary for the correct production of *several* output signals. Consequently the approximate location of many faults can be determined simply by checking all the output signals and noting which are faulty and whether the fault is at line or field rate. Table 4 lists a variety of possible fault symptoms and indicates in each instance the circuitry most likely to be at fault. The list does not, of course, cater for all possible faults but it shows the technique which can be used to localise most faults. The *main functional diagram* of the Generator (Fig. 3) provides a simple explanation of how the device works and helps in the location of faults not listed in the table.

Take care when removing or inserting the plug-in boards or the extender chassis because the boards are mounted close together and it is possible for components on one board to foul the back of the adjacent board. This is particularly the case with boards 1 and 2 where the delay lines on board 1 are very close to the back of board 2. It is advisable to disconnect the mains supply when boards are being removed or inserted.

Several boards (in particular the Combining board, No. 2) have a very high component density and to avoid short-circuits it is advisable to disconnect the mains supply when applying or removing an oscilloscope probe.

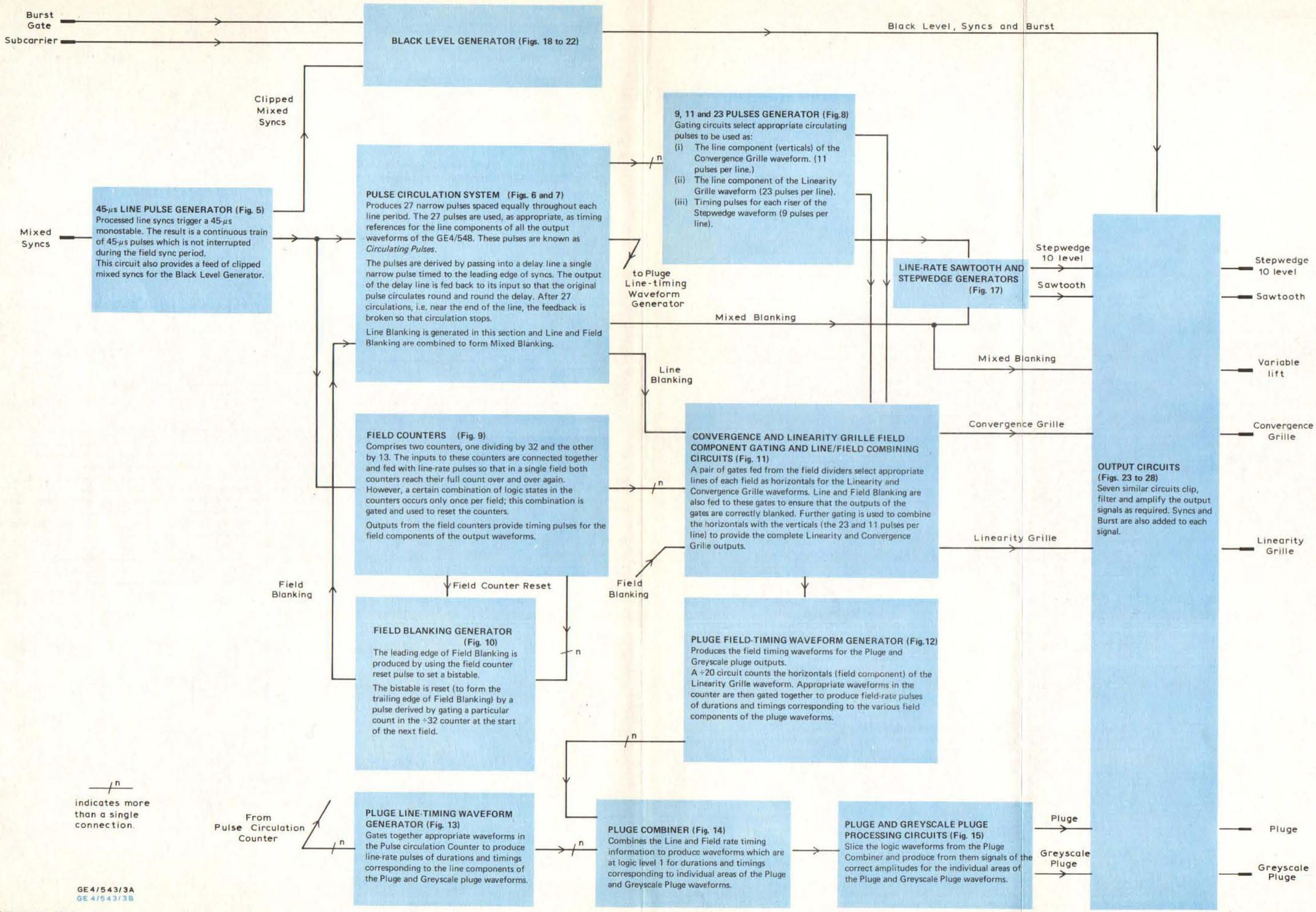
In the event of a fault check the power supply outputs (there are monitoring points along the front edge of the power supply board) before delving into the plug-in boards. A blown fuse does not necessarily cause the output voltages to drop to zero; they may merely be incorrect.

If the power supplies are correct use Table 4 and the main functional diagram (Fig. 3) to help locate the faulty function.

TABLE 4

Fault Identification in the GE4/543

Waveforms Incorrect	*Nature of Fault*	*Probable Area of Fault*	*Board*	*Fig. Nos.*
All	Burst absent	Black Level Generator	Black Level Generator (No. 5)	18, 19, 20, 21, 22
All	Syncs and Burst absent	Black Level Amplifier	Output (No. 4)	23
All	Line Syncs absent, Field Blanking absent or of incorrect duration, No field components of Grille or Pluge outputs.	45-μs Line Pulse Generator	Field (No. 3)	5
All	Line components faulty, Field components O.K.	Pulse Circulation System	Line (No. 1)	6, 7
Both Grille outputs Both Pluge outputs Also Field Blanking on all outputs may be of incorrect duration	Line components O.K. Field components faulty	Field Counters	Field (No. 3)	9
All	Line Blanking of incorrect duration, otherwise O.K.	Line Blanking Generator Note that a small error less than 300 ns can be corrected by adjustment. See *Timing Adjustments* on page 6	Line (No. 1)	7
All	Field Blanking of incorrect duration, otherwise O.K.	Field Blanking Generator	Field (No. 3)	10
Sawtooth	Sawtooth absent or distorted	Sawtooth Generator or Sawtooth output amplifier	Combining (No. 2) Output (No. 4)	16 28
Stepwedge	Stepwedge absent or distorted	Stepwedge Generator or Stepwedge output amplifier.	Combining (No. 2) Output (No. 4)	17 28
	Incorrect number of steps	9 pulses per line generator	Line (No. 1)	8
Greyscale Pluge	Greyscale Pluge absent or Greyscale incorrectly timed or incorrect number of greyscale steps	IC3a, IC4a, IC5a,b,d, IC6a, TR20 to TR23	Combining (No. 2)	13, 14
Pluge, Greyscale Pluge	Black and dark grey bars (at left-hand side of raster) absent or incorrectly timed	IC1, IC6b, IC2a or IC5c	Combining (No. 2)	13, 14
Pluge	Peak White and Light Grey areas absent or incorrectly timed	IC2b, IC3b, IC4b, IC6c, or IC6d	Combining (No. 2)	13, 14
Pluge, Greyscale Pluge	Outputs absent or horizontal transitions incorrectly timed	Pluge Field Timing Waveform Generator	Field (No. 3)	12
Linearity Grille, Convergence Grille	Incorrect number of verticals or verticals absent. (In the latter case the Stepwedge output may also be absent)	9, 11 and 23 pulses Generator	Line (No. 1)	8
Linearity Grille Pluge Greyscale Pluge	All three outputs absent or Pluge and Greyscale Pluge absent and verticals only present on the Linearity Grille Output	IC10b, IC11d	Field (No. 3)	11
Convergence Grille	Convergence Grille absent or verticals only present	IC10a, IC11c	Field (No. 3)	11



GE4/543/3A
GE4/543/3B

Fig.3 Main Functional Diagram of GE4/543

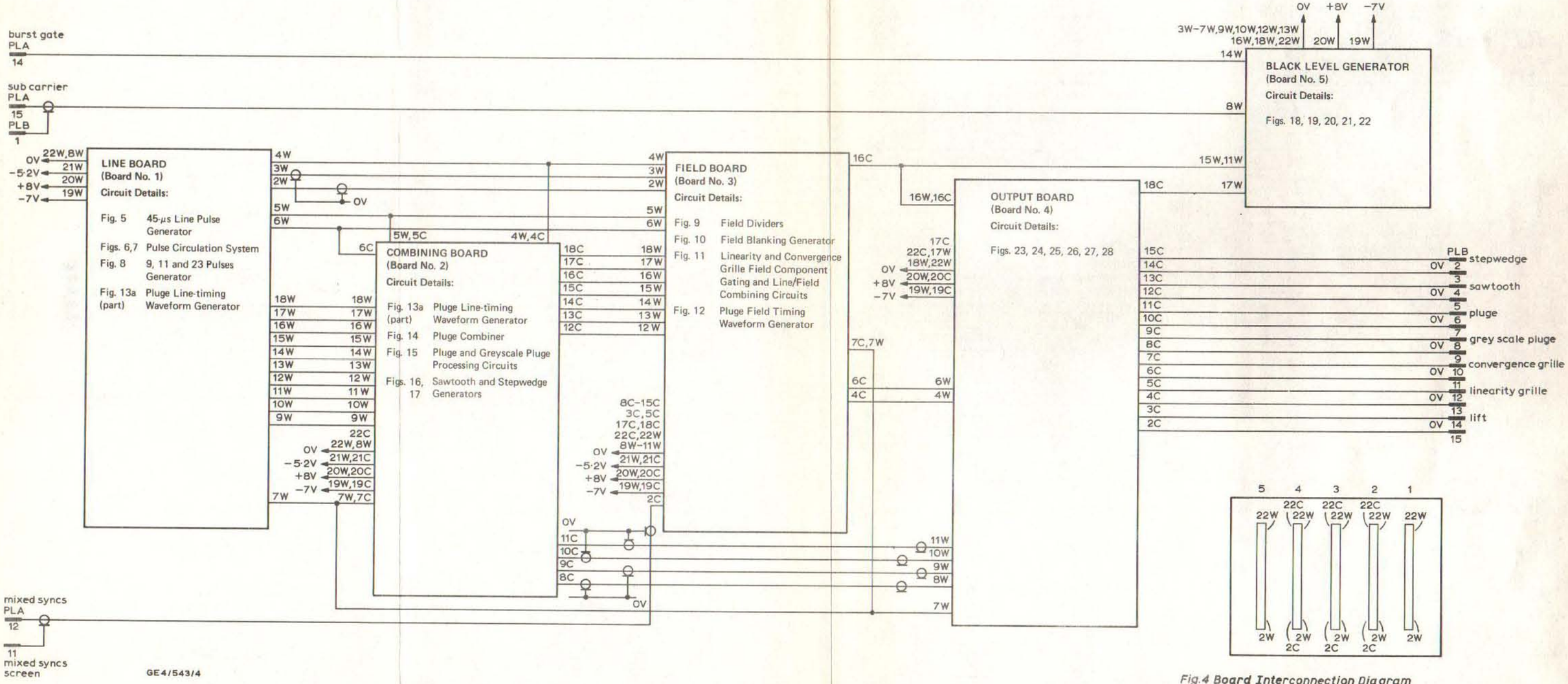
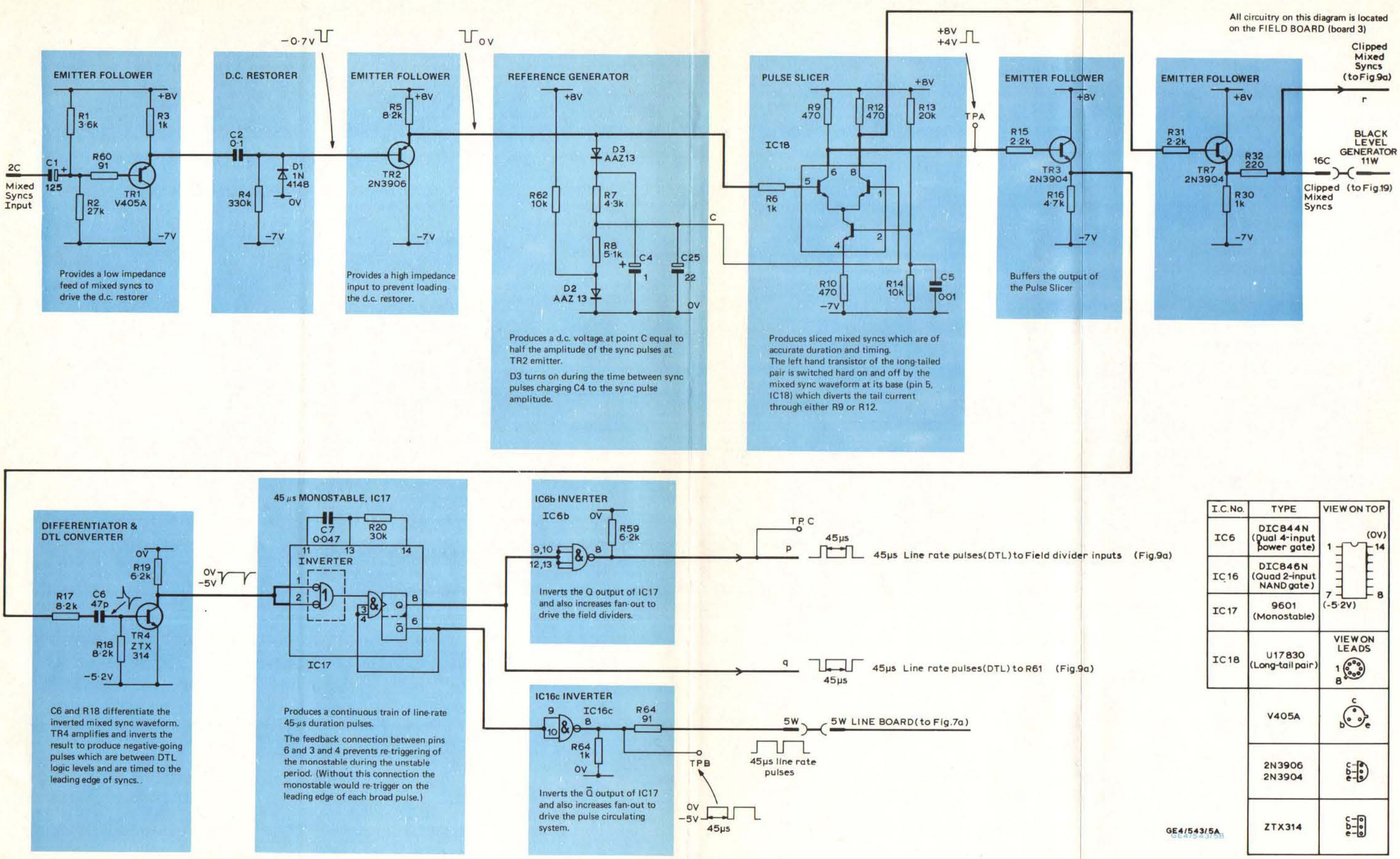


Fig.4 Board Interconnection Diagram

45μs LINE PULSE GENERATOR



I.C.No.	TYPE	VIEW ON TOP
IC6	DIC844N (Dual 4-input power gate)	(0V) 1 14 7 8 (-5·2V)
IC16	DIC846N (Quad 2-input NAND gate)	
IC17	9601 (Monostable)	
IC18	U17830 (Long-tail pair)	VIEW ON LEADS 1 8
	V405A	c b e
	2N3906 2N3904	c b e
	ZTX314	c b e

GE4/543/5A

Fig.5.Circuit Diagram of 45μs Line Pulse Generator

PULSE CIRCULATION SYSTEM

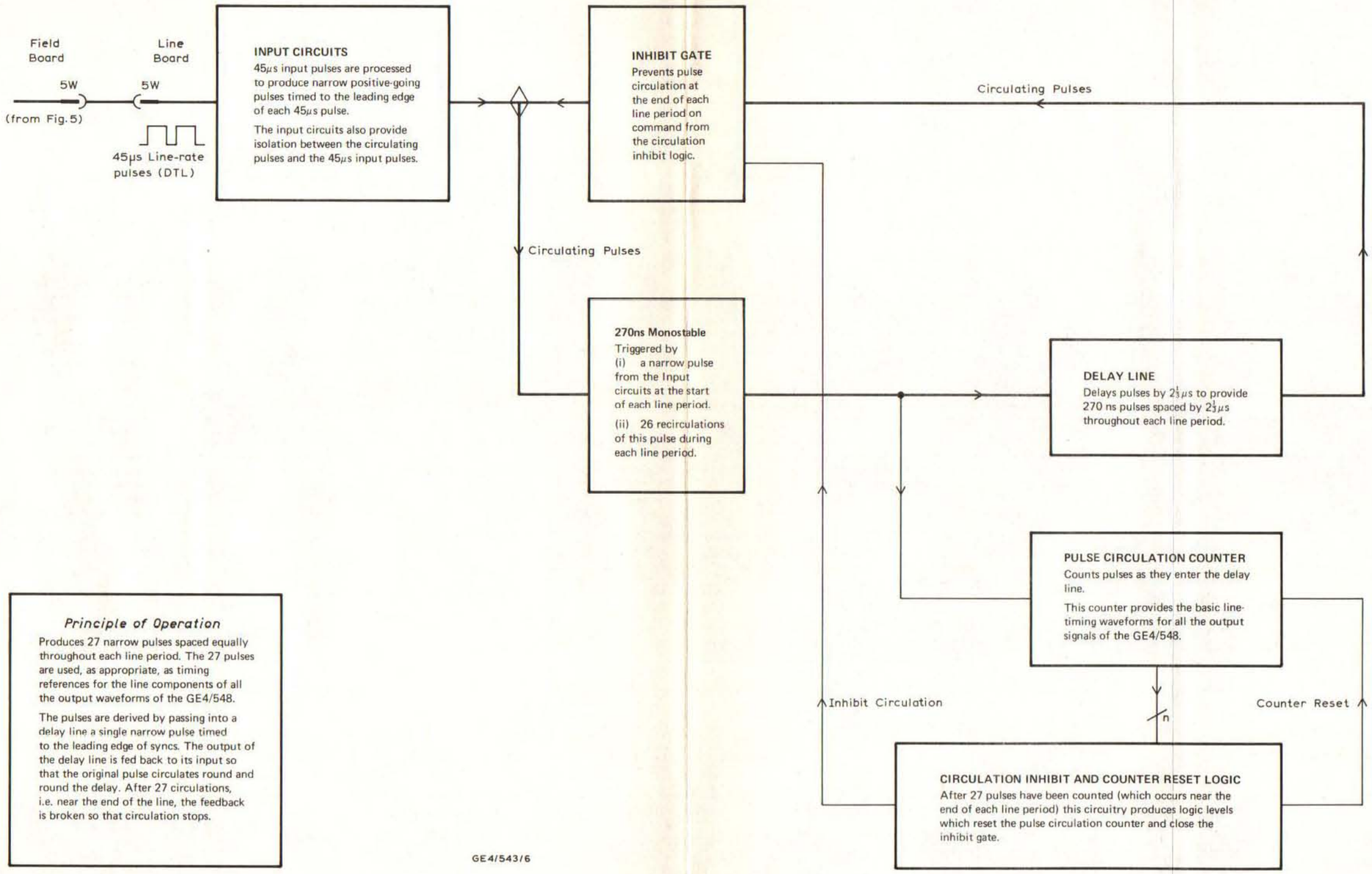


Fig. 6 Simplified Functional Diagram of Pulse Circulation System

Principle of Operation

Produces 27 narrow pulses spaced equally throughout each line period. The 27 pulses are used, as appropriate, as timing references for the line components of all the output waveforms of the GE4/548.

The pulses are derived by passing into a delay line a single narrow pulse timed to the leading edge of syncs. The output of the delay line is fed back to its input so that the original pulse circulates round and round the delay. After 27 circulations, i.e. near the end of the line, the feedback is broken so that circulation stops.

GE4/543/6

All circuitry on this diagram is located on the LINE BOARD (board 1)

45µs 0V -5V

FIELD BOARD 5W (from Fig 5) 5W 45µs line rate pulses (DTL)

DIFFERENTIATOR

R1 1·8k C1 68p R5 2·7k R6 5·6k 0V -5·2V

differentiates 45 µs line-rate pulses to give +ve and -ve going spikes

R2 2k

ISOLATOR

IC1c IC1d

prevents delayed pulses at the output of IC1a from reaching TR1 and erroneously re-setting IC2.

-0·8V -1·6V

INHIBIT GATE IC1a

IC1a

A 0 state on pin 2 opens the gate and allows level 0 pulses from the delay line output to pass back to the input of the delay line via IC3.

A 1 state on pin 2 holds the output at 0 and thus inhibits pulse circulation.

-0·8V -1·6V 270ns Circulating pulses

DTL TO MECL LOGIC CONVERTER

45µs MECL

R3 2k R7 300 R53 91 TR1 2N3906 R8 2k 0V -5·2V

AMPLIFIER

+8V R14 1·1k C5 0·1 R18 1k R15 180 R12 10k C4 1 R13 91 TR2 2N3906 R16 91 TR3 2N3906 R19 470 R17 1k -7V

Provides a low-impedance source of 270 ns pulses from IC3a for driving the delay line

TPB R52 1k 270ns 2⅓ µs 0V -2V

DELAY LINE

DL1 501KAT1005F in 0 to 1000ns 0V

DL2 501KAT1005F in 20 0 to 1000ns 0V C14 36p

DL3 501BPT3006C in 20 0 to 300ns 6 0V R23 3·6k C15 20p R30 510 tap A

tap C tap D tap B Delay Line Outputs

Three 'chocolate block' delay elements together provide a delay of 2·3 µs. Note that the total delay in the pulse circulating system is 2⅓ (2·333 µs). The 33 ns not provided by the delay elements comprises the cumulative delay of TR2, TR3, TR7, etc. and the delay provided by the 'Fine Circulation time' adjustment.

EMITTER FOLLOWER

0V R27 18k D4 1N4148 R32 91 TR7 BC109 R35 4·3k -5·2V

Noise spikes at D4 cathode are generally of insufficient amplitude to bring D4 into conduction. D4 thus reduces noise on the circulating pulse path.

DELAY ADJUSTMENT

R31 100 R28 2k C21 68p 0V

R28 sets the circulation delay to exactly 2⅓ µs

270 ns MONOSTABLE

C3 A.O.T. 51p R9 2·7k IC3a 6 S Q 2 5 R Q̄ 1 R10 2k

Astable period set by R9 and C3. +ve going spikes on pin 5 produce level 1 pulses of duration 270 ns at pin 1.

-ve going spikes on pin 5 have no effect.

DIFFERENTIATOR

C2 68p R4 10k -5·2V

differentiates the outputs of IC1d and IC1a to give +ve and -ve going spikes

R11 1k TP.A 270ns 2⅓ µs -0·8V -1·6V

PULSE CIRCULATION COUNTER

IC4 to IC8 form a ripple-through down counter which counts 270 ns pulses as they are re-circulated through the delay.

IC4 IC5 IC6 IC7 IC8 (J Q K Q̄ R) Ā A B̄ B C̄ C D̄ D Ē E

RECIRCULATION INHIBIT BISTABLE

IC2 8.9. 10.11. K 3.4. 5.6. J Q 13

The leading edge of each 45 µs pulse sets Q to 0 which opens gate IC1a. Q is set back to 1 (which closes IC1a) by a count of 27 in the pulse circulation counter.

EMITTER FOLLOWER

delay line tap B D2 IN4148 R24 1k R25 91 TR5 BC109 R26 4·3k 0V -5·2V

delay line tap C D1 IN4148 R21 18k R20 91 TR4 BC109 R22 4·3k 0V -5·2V

SELECT 5th CIRCULATION

Ē D̄ C B̄ Ā 10 9 8 6 5 4 IC12 1

IC13 SELECT 27th CIRCULATION

Ā B̄ C̄ D̄ Ē 5 4 6 8 9 IC13 10 11

Produces logic 1 on pin 1 and logic 0 on pin 11 when the counter has counted 27 pulses

IC11c

10 9 IC11c 8

Pin 9 goes to level 0 on the 27th circulation. A level 0 pulse appears on pin 10 approx 1·6 µs later, when the 27th pulse reaches tap B on the delay line. Thus the output of IC11c is a level-1 pulse of duration 270 ns occurring once per line approx 1·6 µs after the start of the 27th circulation

COUNTER RE-SET CIRCUIT

IC3b R Q̄ 9 13 C22 220p S Q 8 12 0V R39 750 R40 3·9k 1 2 3 IC11a 0V

The 270 ns level-1 pulse from IC11c sets the Q output of IC3b to 0. This negative-going edge is differentiated by C22, R29, R30 to produce a negative spike which is inverted by IC11a. IC11a output is thus a +ve pulse timed 1·6 µs after the start of the 27th circulation. This pulse is used to re-set the counter.

IC3b is reset by the output of IC12 when the 5th circulation on the next line reaches tap D on the delay line.

T.P.C

Inverted Field Blanking to IC14a (Fig 8a)

Inverted Field Blanking 6W FIELD BOARD 6W (from Fig 10a)

IC1b LINE/FIELD BLANKING COMBINING GATE

IC1b 5 4 6 R37 910 R38 91 C4 220p 0V

T.P.D

Mixed Blanking MECL 7W OUTPUT BOARD 7W (to Fig 27) COMBINING BOARD 7W (to Fig 16)

Inverted Line Blanking FIELD BOARD 4W (to Fig 11)

Combines inverted Line Blanking from IC3b and inverted Field Blanking (see section 6) to produce a standard Mixed Blanking waveform between MECL logic levels.

Inverted Line Blanking to IC10 (Fig 8a)

Positive Logic	
0	−1·5V to −2V
1	−0·7V to −0·85V

All logic elements are MECL

TRUTH TABLE

A B NOR OR

A	B	OR	NOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

IC No	TYPE	BASE view on top
IC1, 11	MC1010P (quad 2-input NOR Gate)	(0V) 1 14 7 8 (-5·2V)
IC2, 4, 5, 6, 7, 8	MC1013P (a.c. coupled J-K Bistable)	
IC3	MC1015P (Dual R-S Bistable)	
IC13	MC1001P (Single 6-input OR/NOR Gate)	

TYPE	BASE view on leads
2N3906	c b e
BC109	c b e

GE4/543/7A
GE4/543/7B

Fig. 7a. Circuit Diagram of Pulse Circulation System

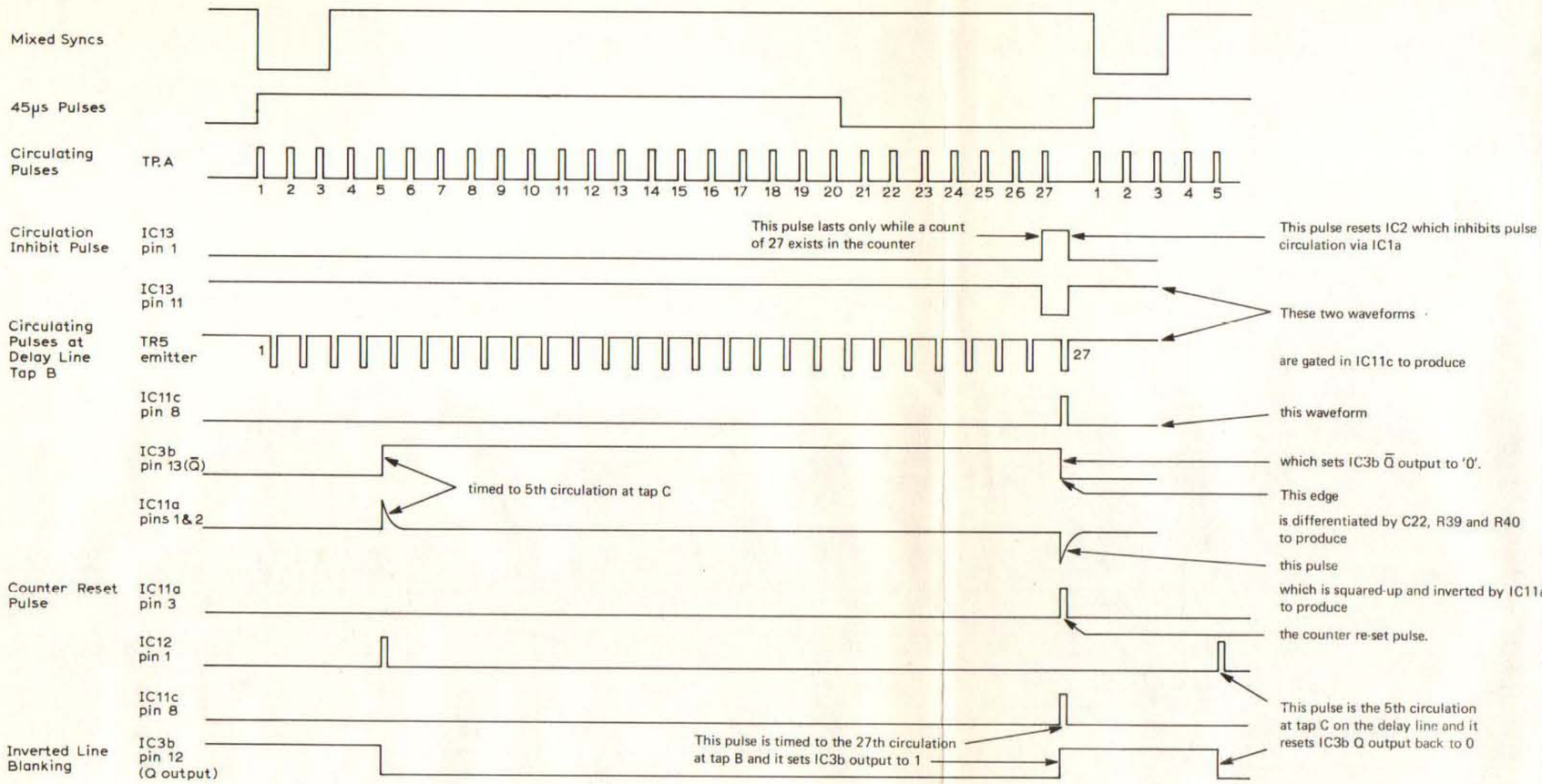


Fig. 7b. Waveforms in the Pulse Circulation System

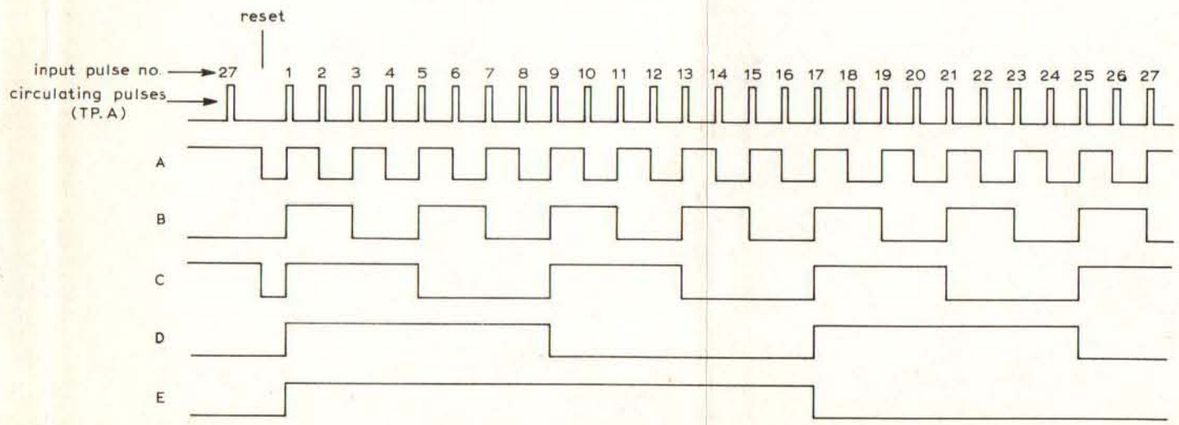
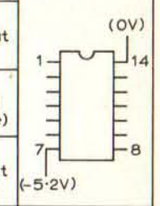


Fig. 7c. Waveforms in the Pulse Circulation Counter

GE4/543/8

9,11 and 23 PULSES GENERATOR

All circuitry on this diagram is located on the LINE BOARD (board 1)

Circuit No.	Type	view on top
IC9 IC11	MC1010P (Quad 2-input NOR gate)	
IC10	MC1013P (a.c. coupled J-K bistable)	
IC14	MC1007P (Triple 3 input NOR gate)	
TR6	BC109	view on leads 
D3	1N4148	

Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

+ve logic	
0	−1·5 to −2 volts
1	−0·7 to −0·85 volts

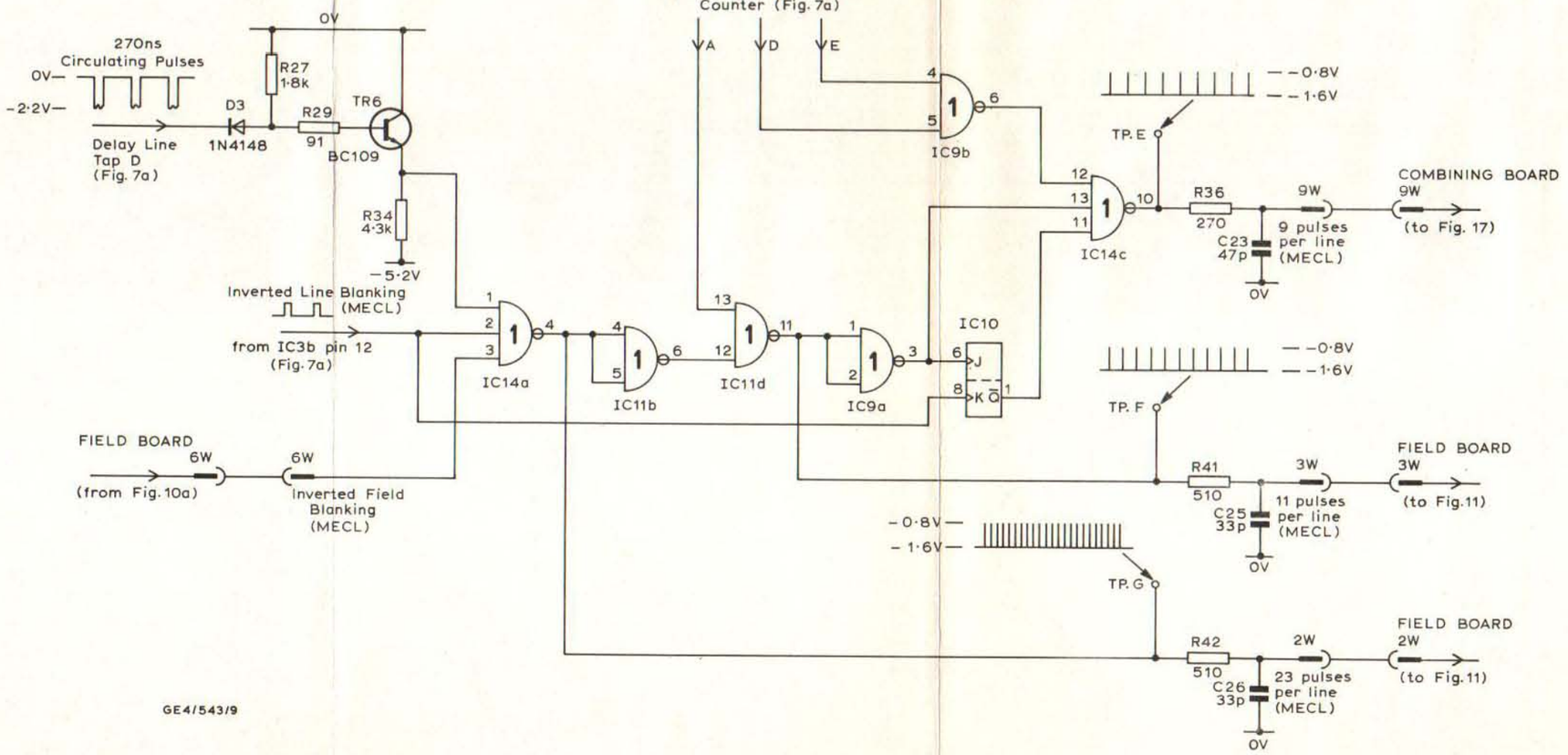


Fig. 8 a. Circuit Diagram of 9, 11 and 23 Pulse Generator

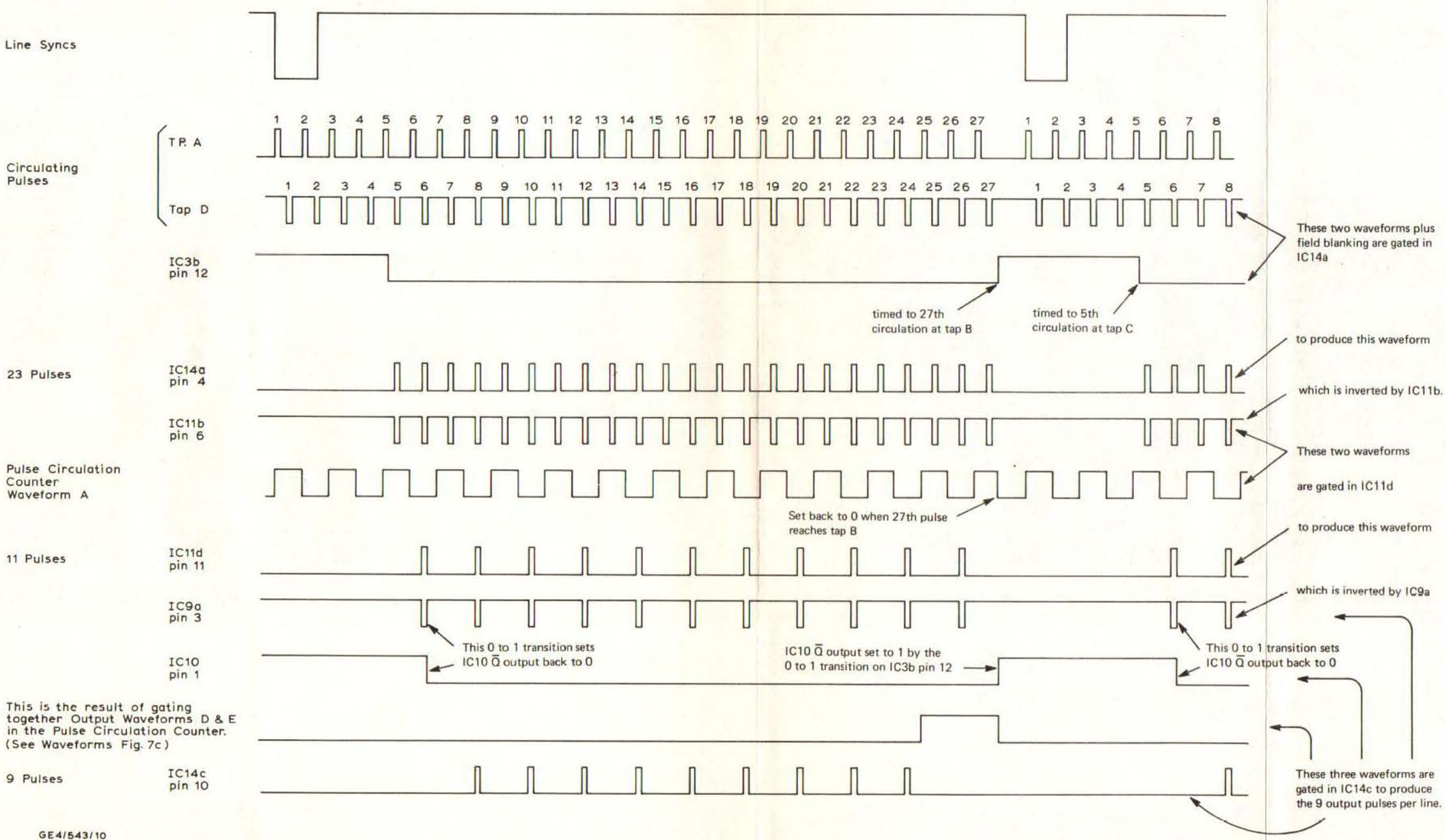


Fig. 8b Waveforms in the 9,11 and 23 Pulses Generator

FIELD COUNTERS

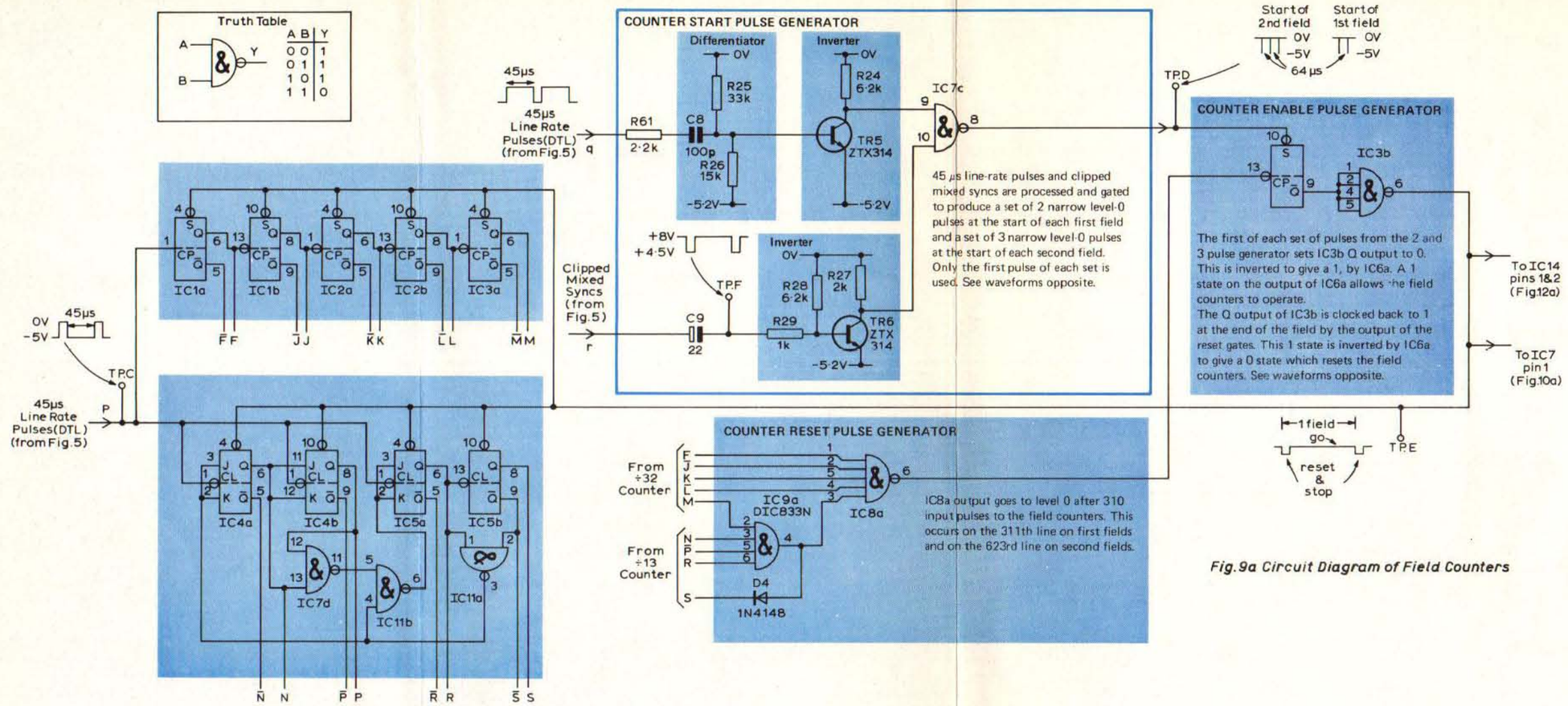


Fig.9a Circuit Diagram of Field Counters

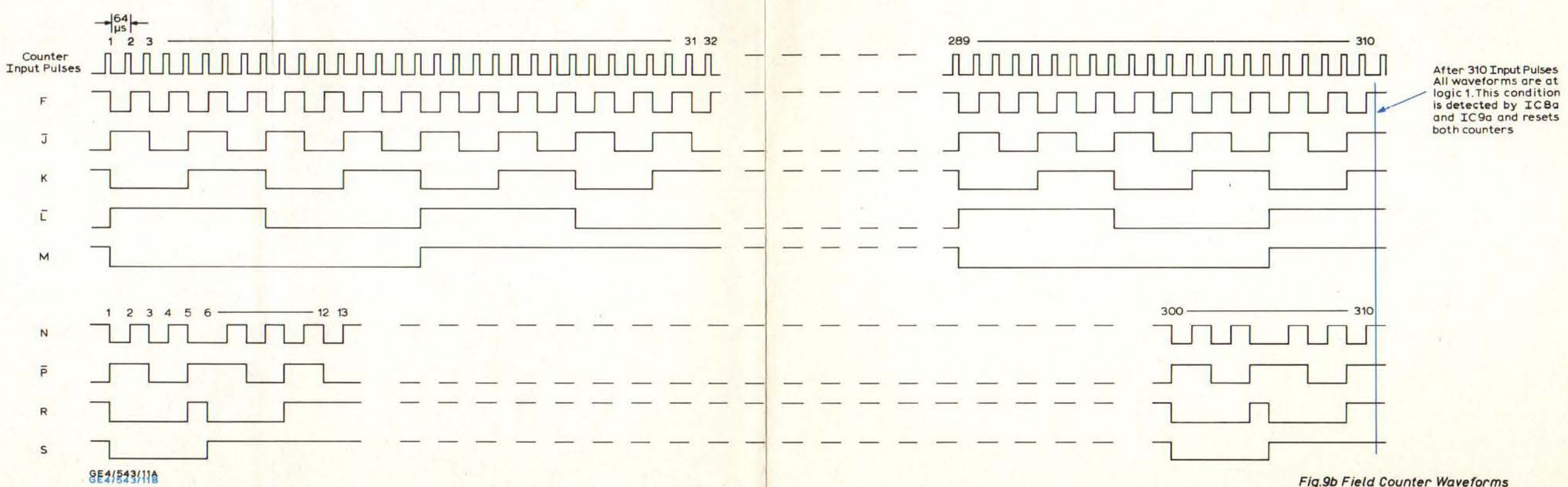


Fig.9b Field Counter Waveforms

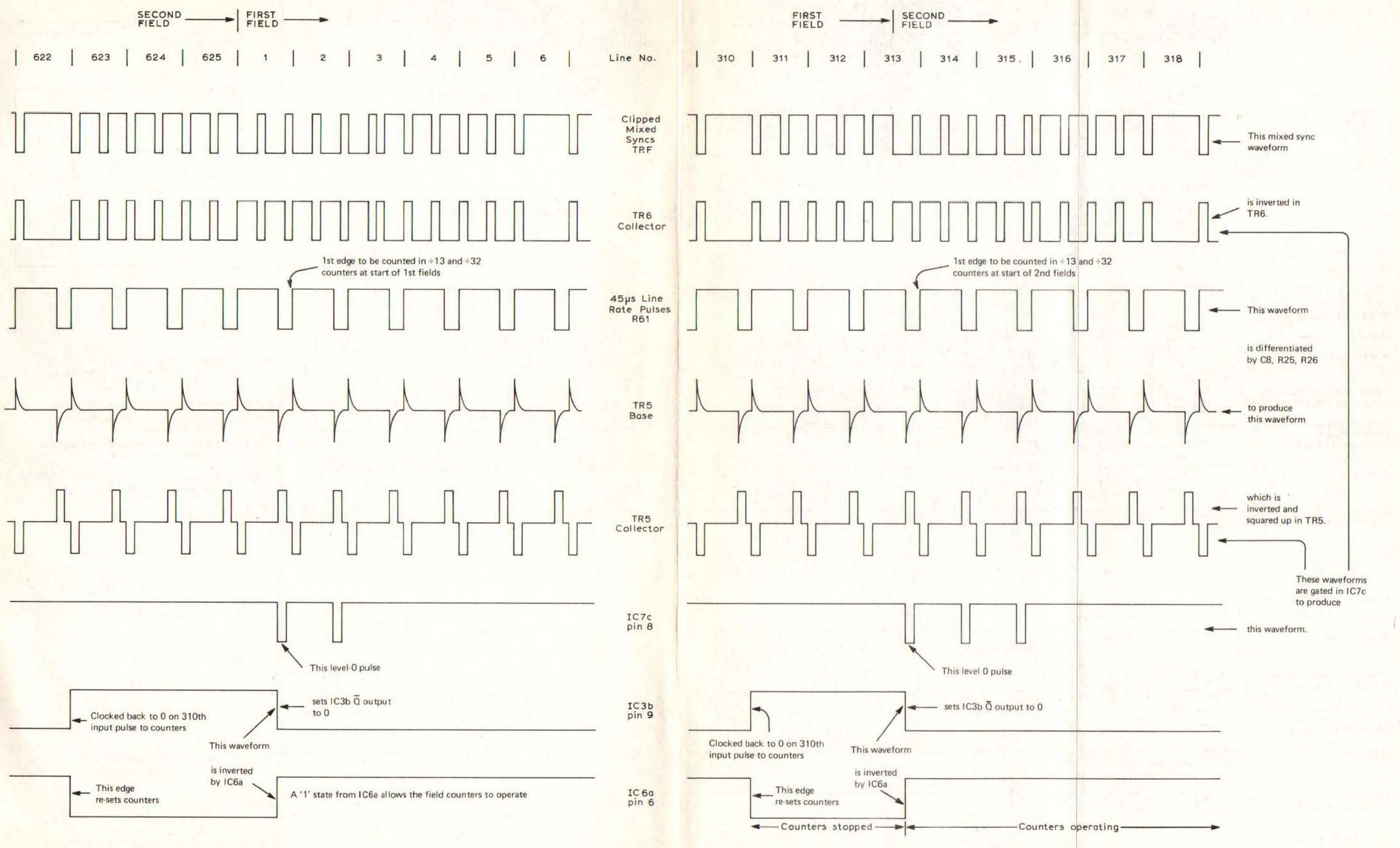
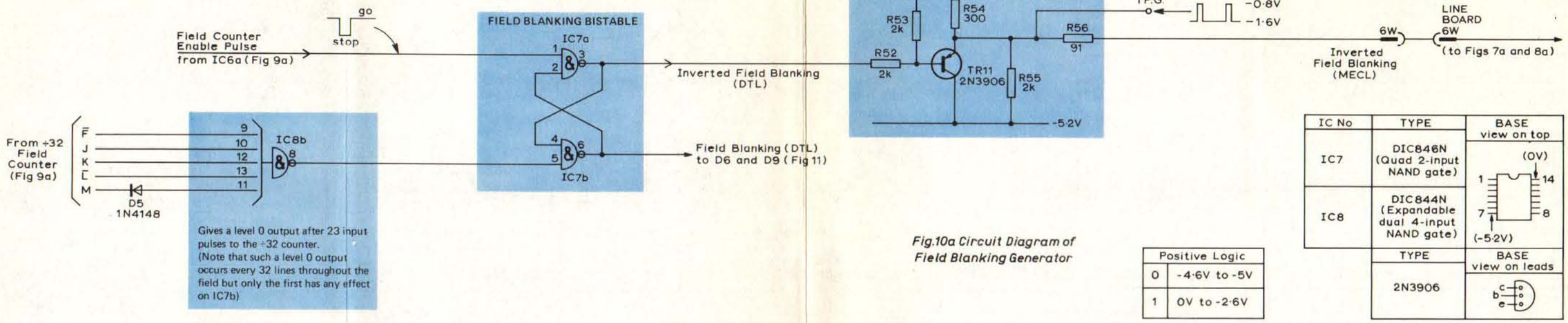


Fig. 9c Field Dividers Start/Enable Pulse Generator Waveforms

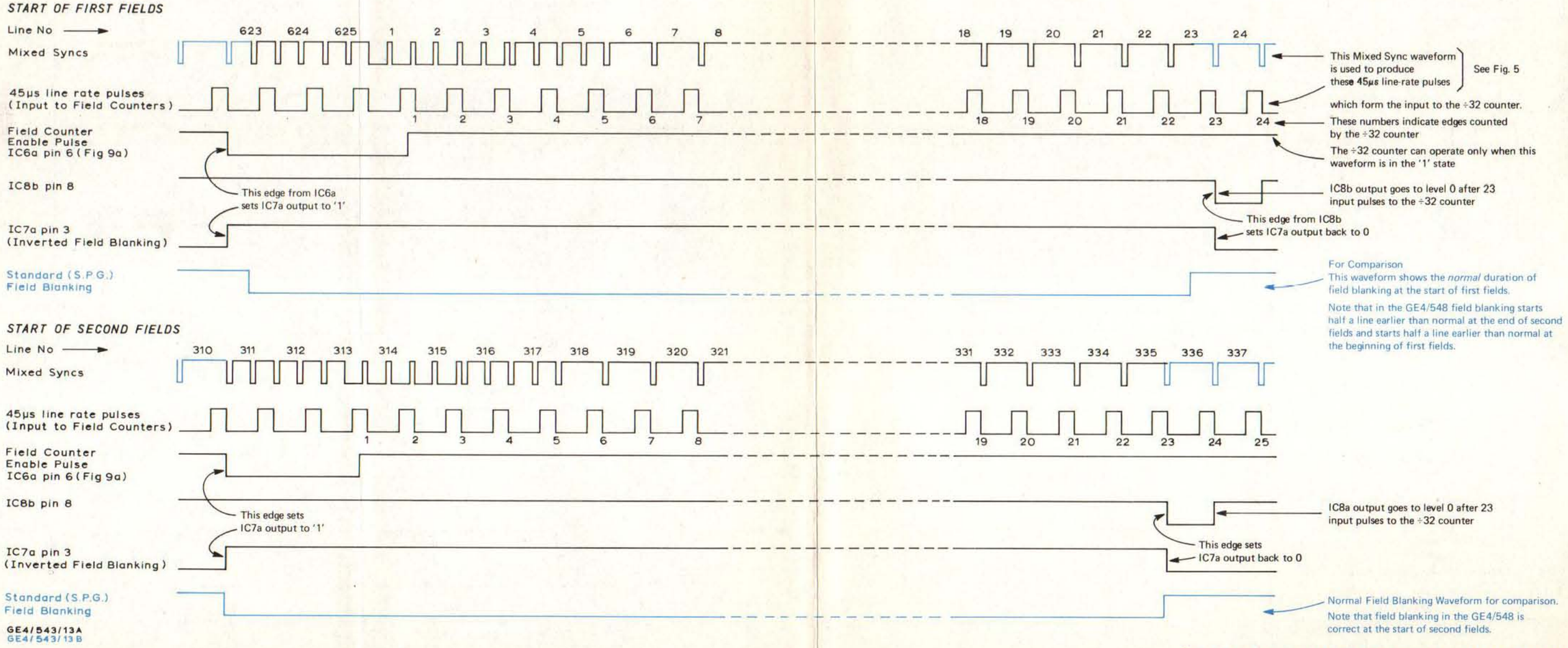
FIELD BLANKING GENERATOR



IC No	TYPE	BASE view on top
IC7	DIC846N (Quad 2-input NAND gate)	(0V) 1 14 7 8 (-5·2V)
IC8	DIC844N (Expandable dual 4-input NAND gate)	
	TYPE	BASE view on leads
	2N3906	c b e

Positive Logic	
0	-4·6V to -5V
1	0V to -2·6V

Fig.10a Circuit Diagram of Field Blanking Generator

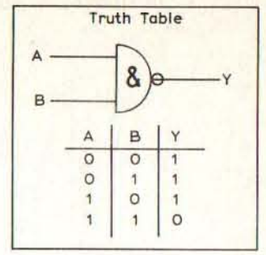


Note: Blue sections of MS waveforms indicate active lines

Fig.10b Field Blanking Generator Waveforms

LINEARITY & CONVERGENCE GRILLE FIELD COMPONENT GATING AND LINE/FIELD COMBINING CIRCUITS

All circuitry on this diagram is located on the FIELD BOARD (board 3)



LINEARITY GRILLE FIELD COMPONENT GATE
Gives a level 0 output on the 10th input pulse of each cycle of the ÷13 counter. There are thus 23 output pulses (each of 1 line duration) from IC10b spaced 13 lines apart throughout each field. These pulses form the horizontals of the Linearity Grille waveform.

Field Blanking from IC7b (fig. 10a)
-0·8V
-1·6V
(Inhibits production of grille field components during Field Blanking)

from ÷13 Field Counter (Fig. 9a)
R
S
$\overline{P}$
$\overline{N}$
12
13
9
10
11
IC10b
R34 6·2k
0V

D6 1N4148
D7 1N4148

52µs
0V
-5V
0·83ms

IC13 pin 1 (page 24)

LINEARITY GRILLE COMBINING GATE
Combines the field component (from IC10b) and the line component (23 pulses per line from the line board) of the Linearity Grille waveform. (Note: this gate effectively acts as a *NOR* gate for level-0 pulses)

12
13
IC11d
11
R58 1k
C28 10p
0V

4C
Linearity Grille (TTL)
OUTPUT BOARD 4W
(to Fig.26)

LINE BOARD 2W
(from Fig. 8a)
2W
23 pulses per line
-0·8V
-1·6V

0V
R49 47
R65 91
TR10 2N3906
R51 1k
R50 240
-5·2V
INVERTER AND MECL TO TTL CONVERTER

Note: Diodes D6, D7, D8, D9 and D10 enable extra inputs to be applied to IC10b pin 11 and IC10a pin 3. The diodes provide isolation between the extra inputs.

LINE BOARD 4W
(from fig. 7a)
4W
Inverted Line Blanking (MECL)

0V
R43 47
TR8 2N3906
R45 1k
R44 240
-5·2V
INVERTER AND MECL TO TTL CONVERTER

D10 1N4148
D9 1N4148

Circuit No.	Type	view on top
IC10	DIC844N (Expandable dual 4-input NAND gate)	(0V) 1 14 7 8 (-5·2V)
IC11	DIC7400N (Quad 2-input NAND gate)	
2N3906		view on leads c b e

The Line Blanking input to IC10a and IC10b is necessary to suppress the output of these I.C.'s during Line Blanking period.

CONVERGENCE GRILLE FIELD COMPONENT GATE
Gives a level 0 output on the 6th input pulse of each cycle of the ÷32 counter. There are thus 9 output pulses (each of 1 line duration) from IC10a spaced 32 lines apart throughout each field. These pulses form the horizontals of the Convergence Grille waveform.

from ÷32 Field Counter (Fig. 9a)
K
$\overline{M}$
$\overline{L}$
$\overline{J}$
F
3
1
2
4
5
D8 1N4148
6
IC10a

52µs
0V
-5V
2ms

CONVERGENCE GRILLE COMBINING GATE
Combines the field component (from IC10a) and the line component (11 pulses per line from the line board) of the Convergence Grille waveform. (Note: this gate effectively acts as a *NOR* gate for level-0 pulses.)

9
10
IC11c
8
R57 1k
C27 10p
0V

6C
Convergence Grille (TTL)
OUTPUT BOARD 6W
(to Fig. 24)

LINE BOARD 3W
(from fig. 8a)
3W
11 pulses per line
-0·8V
-1·6V

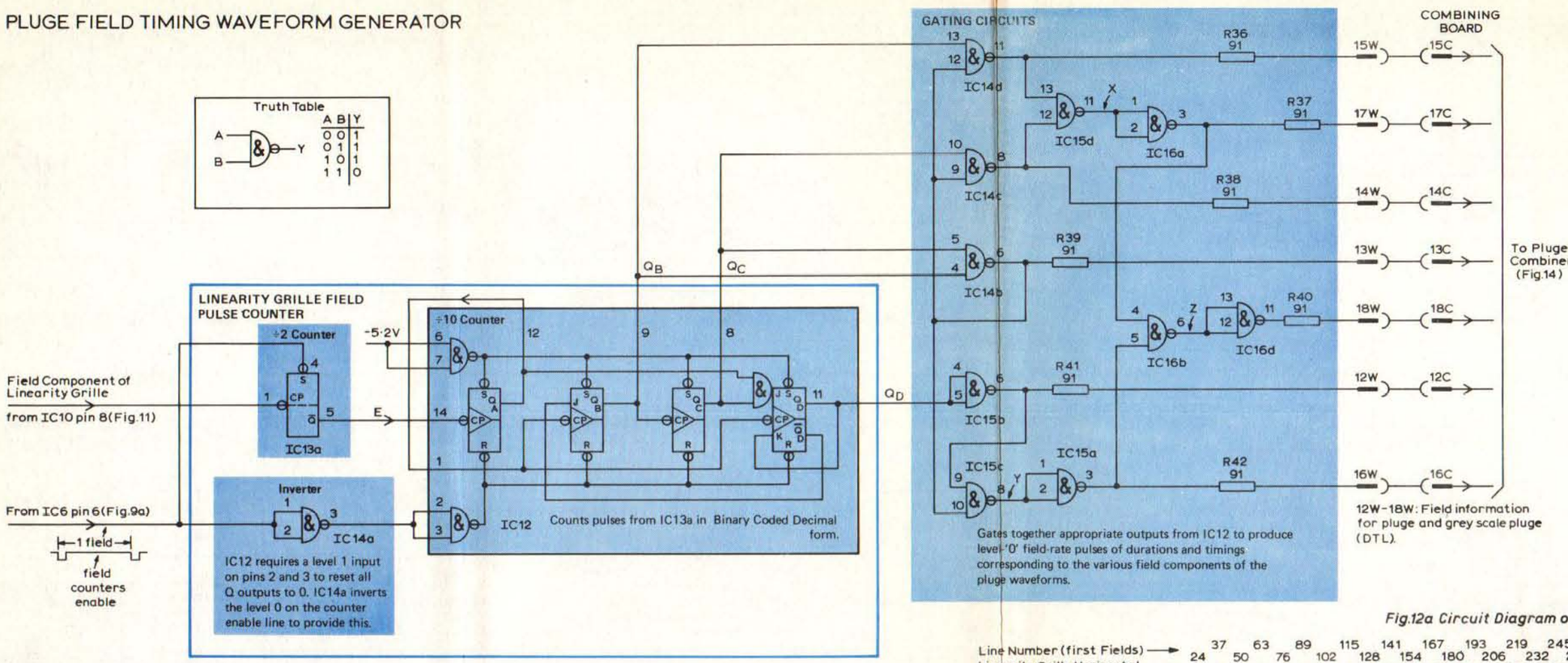
0V
R46 47
R63 91
TR9 2N3906
R48 1k
R47 240
-5·2V
INVERTER AND MECL TO TTL CONVERTER

+ve logic	
0	-4·6 to -5 volts
1	0 to -2·6 volts

GE4/543/14A
GE4/543/14B

Fig 11. Linearity and Convergence Grille Field Component Gating and Line/Field Combining Circuits.

PLUGE FIELD TIMING WAVEFORM GENERATOR



All circuitry on this diagram is located on the FIELD BOARD(board.3)

IC No	TYPE	VIEW ON TOP
IC12	DIC7490N Decade Counter	1, 14, 7, 8 (0V) (-5·2V)
IC13	DIC856N Dual J-K Bistable	(0V) 1, 14, 7, 8 (-5·2V)
IC14, 15,16	DIC846N Quad 2-input NAND gate	

Fig.12a Circuit Diagram of Pluge Field Timing Waveform Generator

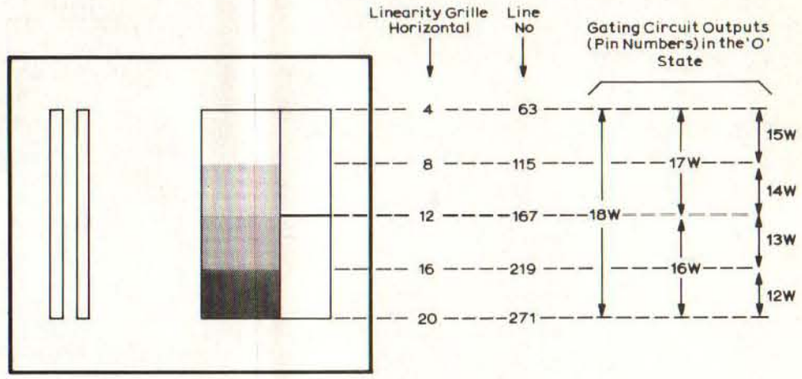


Fig.12b Diagram Relating Gating Circuit Output Waveforms to the Pluge and Greyscale Pluge Displays

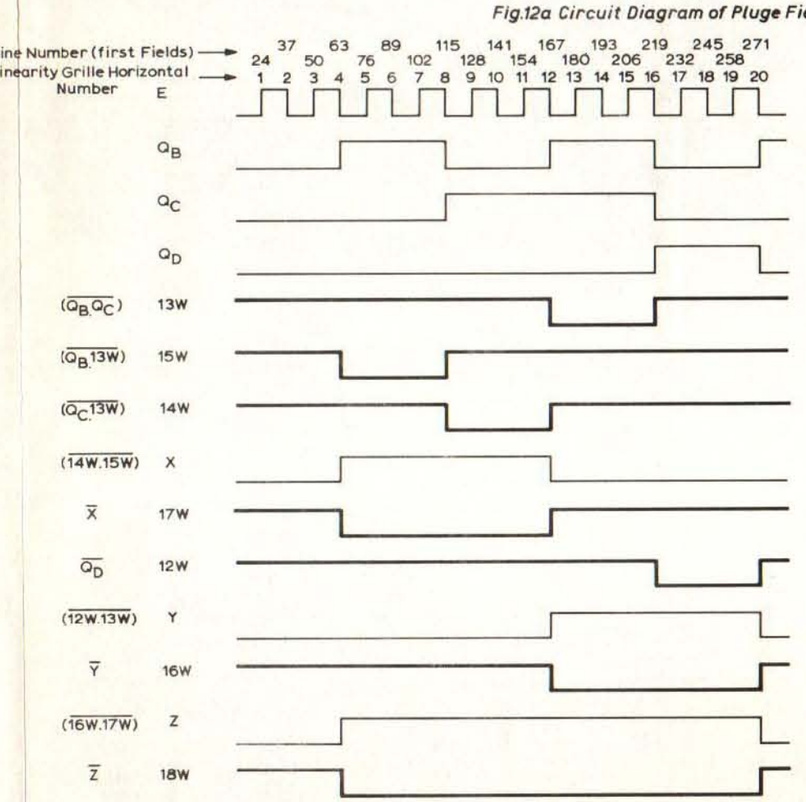
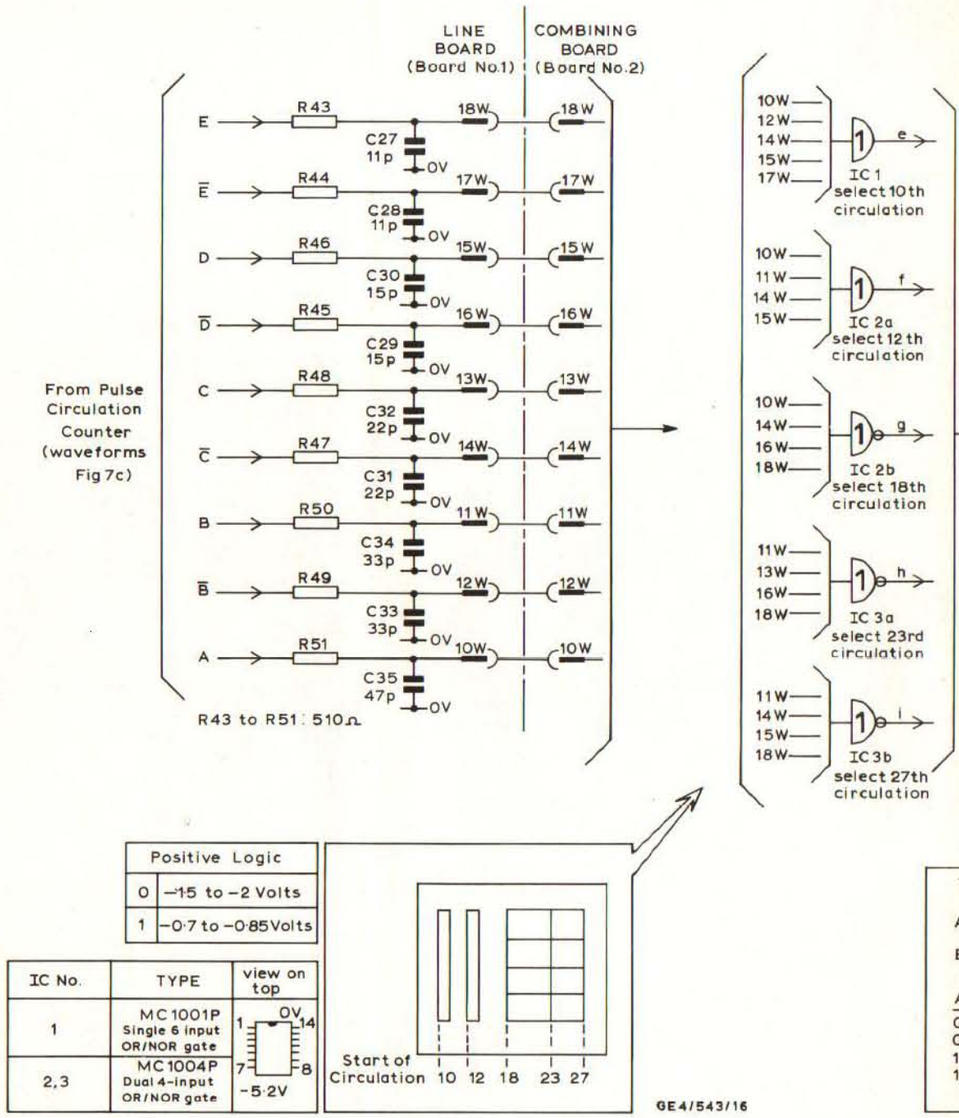


Fig.12c Waveforms

GE4/543/15A
GE4/543/15B

PLUGE LINE-TIMING WAVEFORM GENERATOR



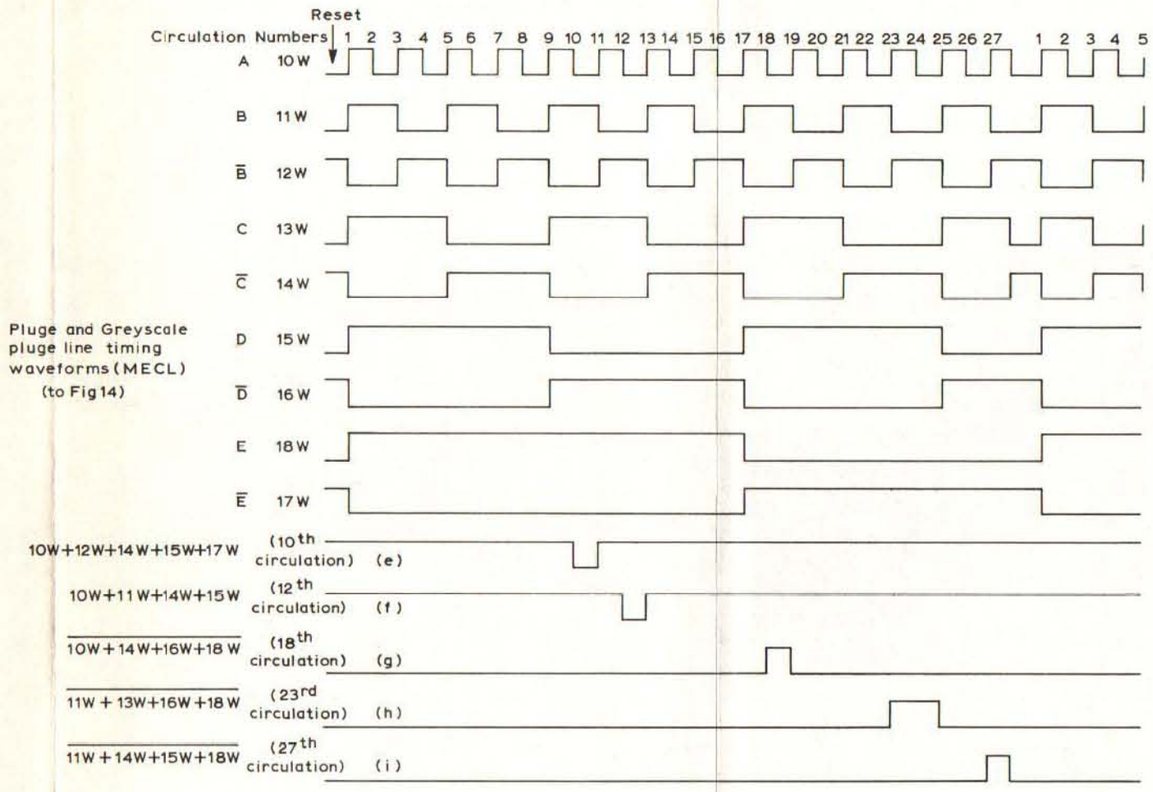
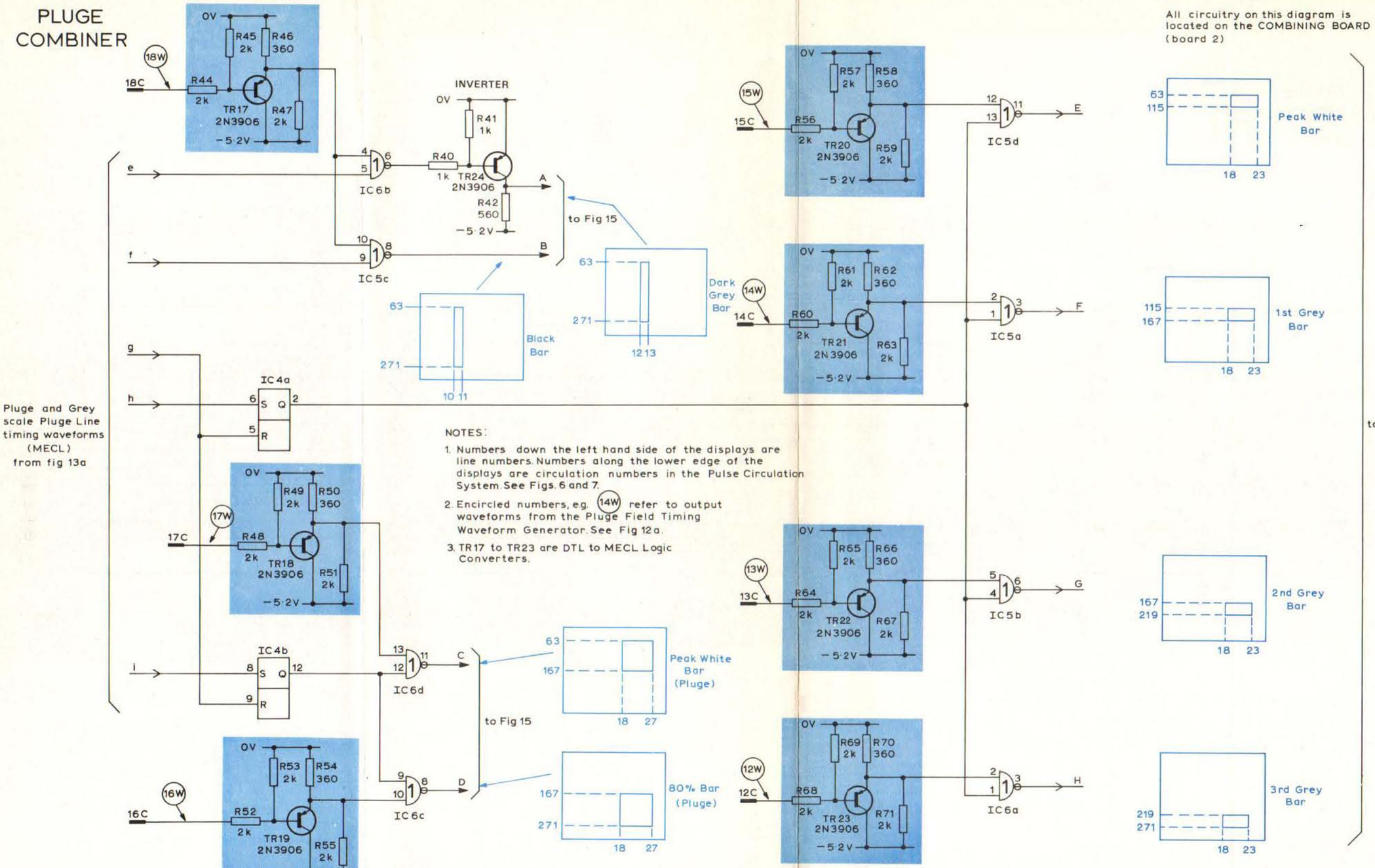


Fig 13. Circuit Diagram of Pluge Line timing waveform Generator.

PLUGE COMBINER

All circuitry on this diagram is located on the COMBINING BOARD (board 2)



Pluge and Grey scale Pluge Line timing waveforms (MECL) from fig 13a

NOTES:

1. Numbers down the left hand side of the displays are line numbers. Numbers along the lower edge of the displays are circulation numbers in the Pulse Circulation System. See Figs. 6 and 7.
2. Encircled numbers, eg. (14W) refer to output waveforms from the Pluge Field Timing Waveform Generator. See Fig 12a.
3. TR17 to TR23 are DTL to MECL Logic Converters.

IC No.	TYPE	VIEW ON TOP
IC 5,6	MC1010 P Quad 2-input NOR Gate	OV, 1, 14, 7, 8, −5·2V
IC 4	MC 1015 P Dual R-S Bistable	
	2N3906	View on leads: c b e

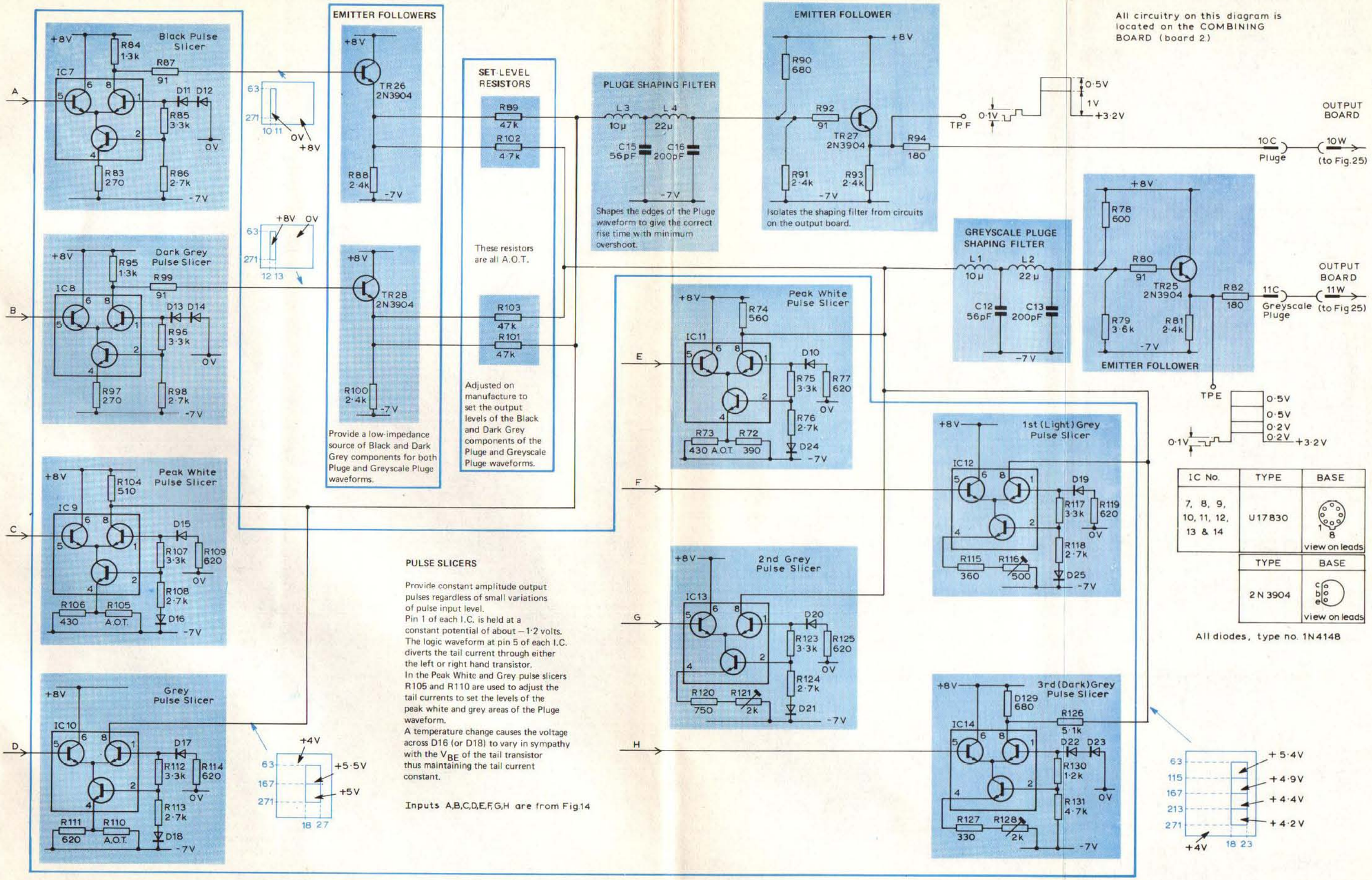
	Positive Logic
0	−1·5 to −2 Volts
1	−0·7 to −0·85 Volts

Fig 14. Circuit Diagram of Pluge Combiner.

GE4/543/17A
GE4/543/17B

PLUGE AND GREYSCALE PLUGE PROCESSING CIRCUITS

All circuitry on this diagram is located on the COMBINING BOARD (board 2.)



IC No.	TYPE	BASE
7, 8, 9, 10, 11, 12, 13 & 14	U17830	view on leads

TYPE	BASE
2 N 3904	view on leads

All diodes, type no. 1N4148

GE4/543/18 A
GE4/543/18 B

Fig. 15. Pluge and Greyscale Pluge Processing Circuits

PULSE SLICER

Provides pulses of duration equal to the H.A.D. of the mixed blanking pulses at TP.A.

Diodes D6 and D7 set the base voltage of TR2 to −1·2 volts, i.e. midway between the logic levels applied to TR1 base.

A logic 1 state of TR1 base diverts all the tail current through TR1 and TR2 is turned off.

A logic 0 state at TR1 base turns TR1 off and diverts the tail current through TR2.

Note: The Pulse Slicer is common to the Sawtooth and Stepwedge Generators.

EMITTER FOLLOWER

Provides a low-impedance source of sliced mixed-blanking to drive the switch transistor, TR5.

SWITCH

Each Mixed Blanking Pulse from TR3 emitter turns TR5 on which discharges C2 in the sawtooth generator.

D2 prevents TR5 from saturating; if saturation were permitted the resulting charge storage in TR5 would produce an unwanted step at the start of each sawtooth.

SAWTOOTH GENERATOR

C3 maintains a constant bias on TR6 base which produces a constant collector current from TR6.

This constant current produces a linear rise in voltage across C2. When TR5 turns on C2 is discharged rapidly (through TR5, R12 and R13). When TR5 turns off C2 starts to recharge and the linear rise in voltage is repeated.

TR7 is an emitter follower with a high input impedance which minimises loading of C2.

D3 and D4 are temperature compensating diodes.

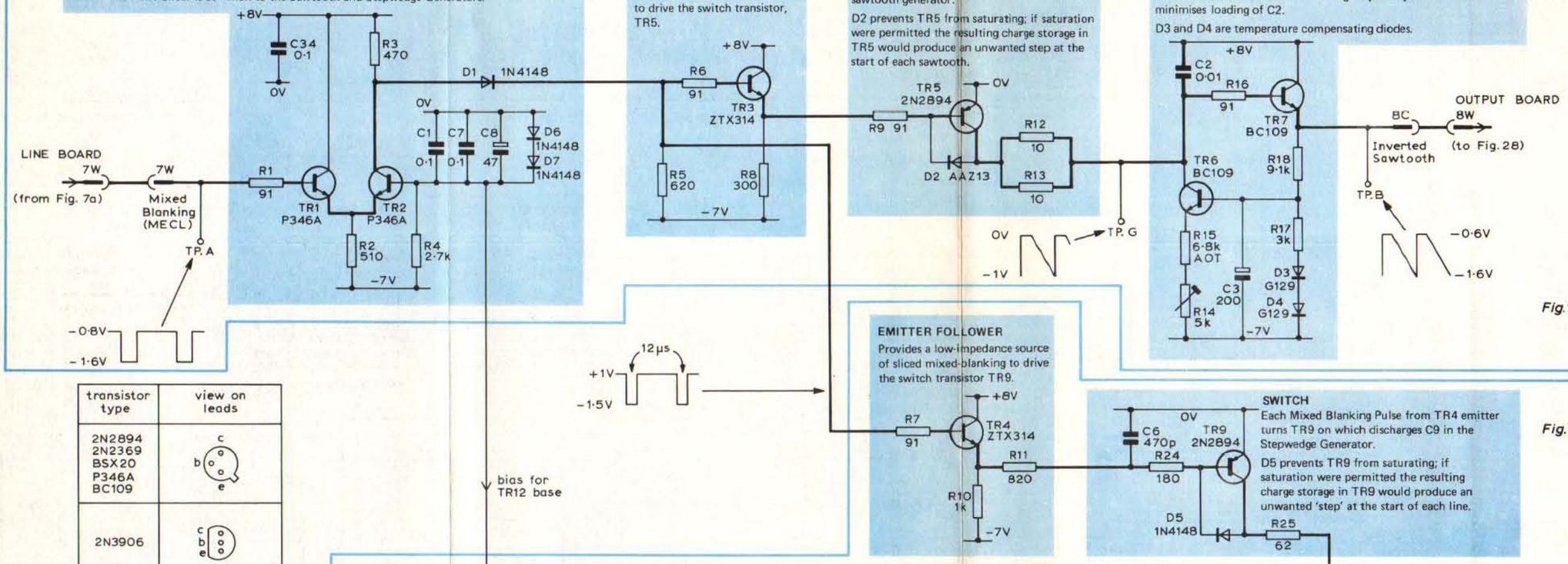


Fig.16 Circuit Diagram of Sawtooth Generator

transistor type	view on leads
2N2894 2N2369 BSX20 P346A BC109	
2N3906	
ZTX314	
2N4303	

EMITTER FOLLOWER

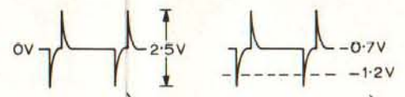
Provides a low-impedance source of sliced mixed-blanking to drive the switch transistor TR9.

SWITCH

Each Mixed Blanking Pulse from TR4 emitter turns TR9 on which discharges C9 in the Stepwedge Generator.

D5 prevents TR9 from saturating; if saturation were permitted the resulting charge storage in TR9 would produce an unwanted 'step' at the start of each line.

Fig.17 Circuit Diagram of Stepwedge Generator



CLIPPER

D6 and D7 set the base of TR12 to −1·2V.

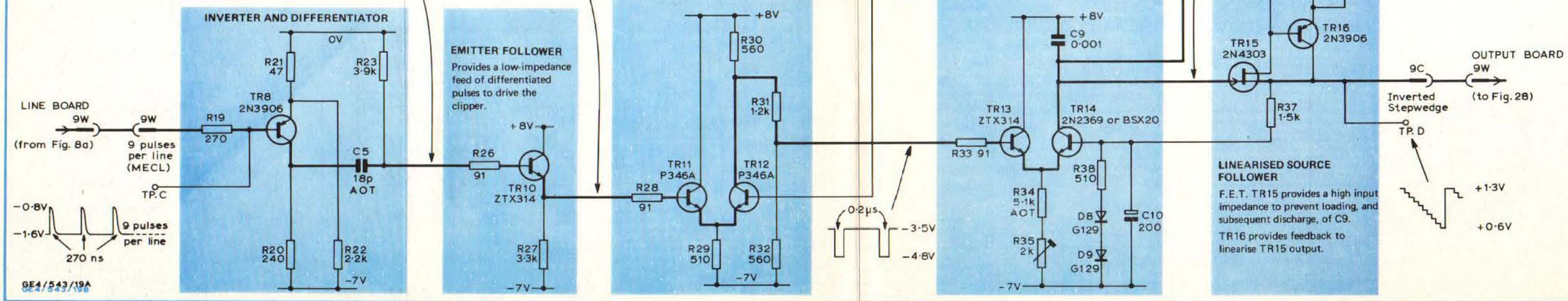
Normally TR11 conducts all the current from R29 and so TR12 is non-conducting, but negative-going spikes at TR11 base turn TR11 off and TR12 on.

TR12 output is thus 9 negative-going pulses per line.

STEPWEDGE GENERATOR

Each negative-going pulse at TR13 base turns TR14 on and passes a discrete amount of charge into C9. The charge on C9 (and hence the p.d. across it) increases with each successive input pulse producing an inverted stepwedge waveform across C9.

D8 and D9 provide temperature stabilisation. R35 adjusts the current available to charge C9 and therefore adjusts the stepwedge amplitude.



BLACK LEVEL GENERATOR

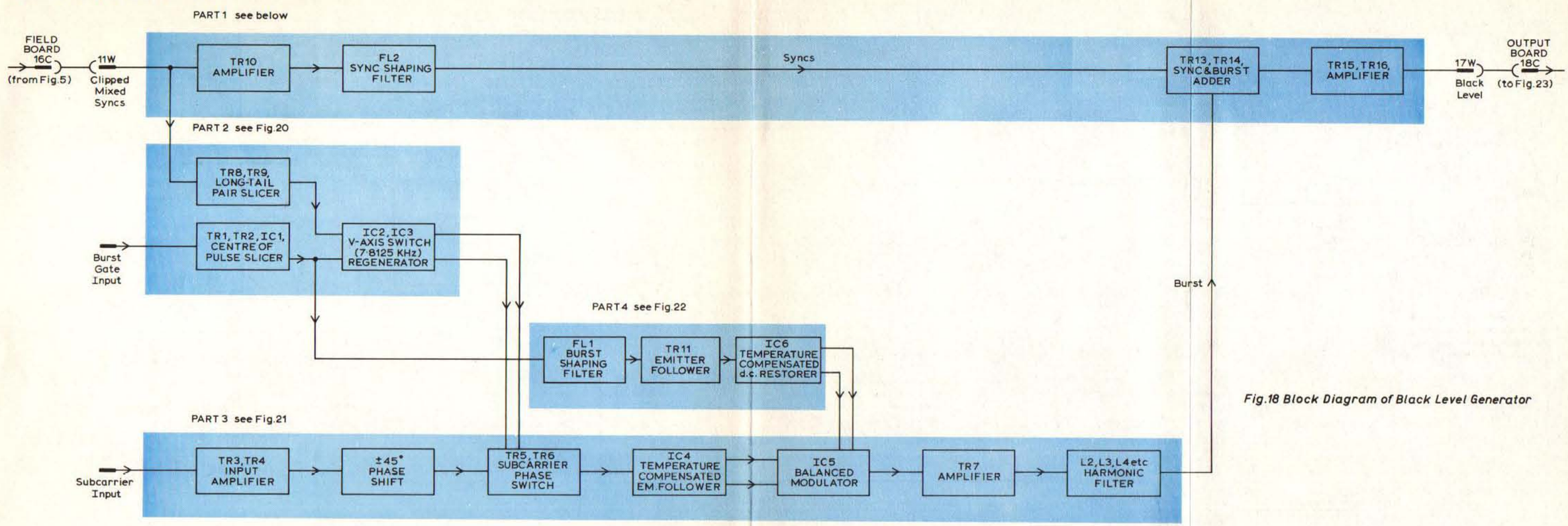
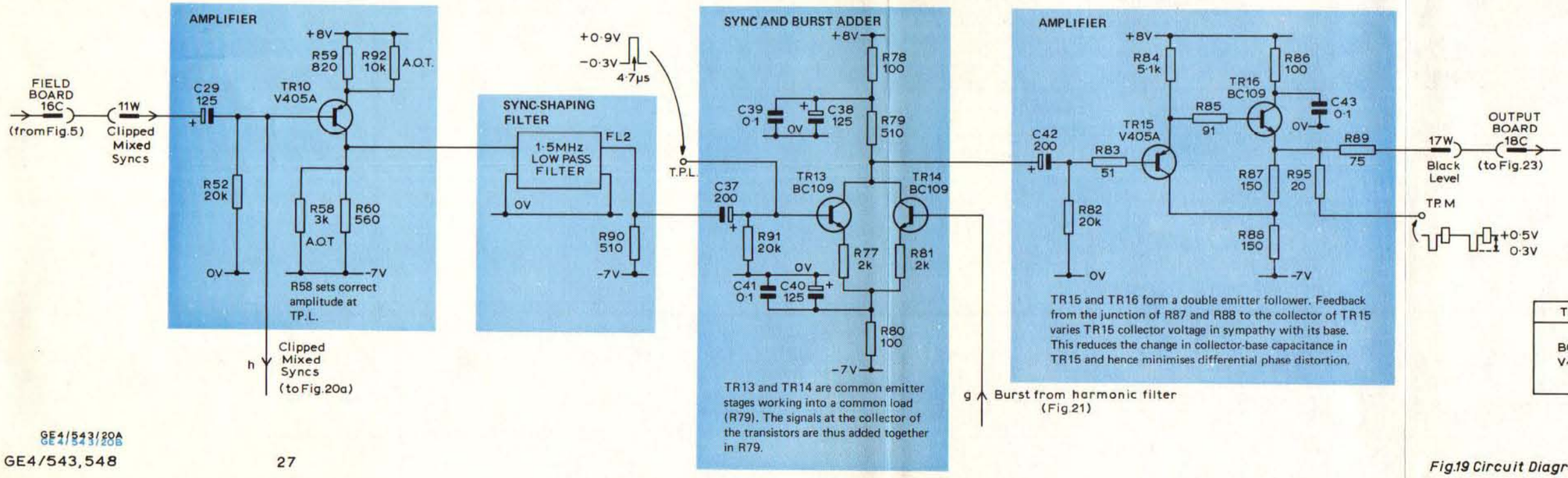


Fig.18 Block Diagram of Black Level Generator



TYPE	BASE
BC109 V405A	VIEW ON LEADS c e b

Fig.19 Circuit Diagram of Black Level Generator - Part 1

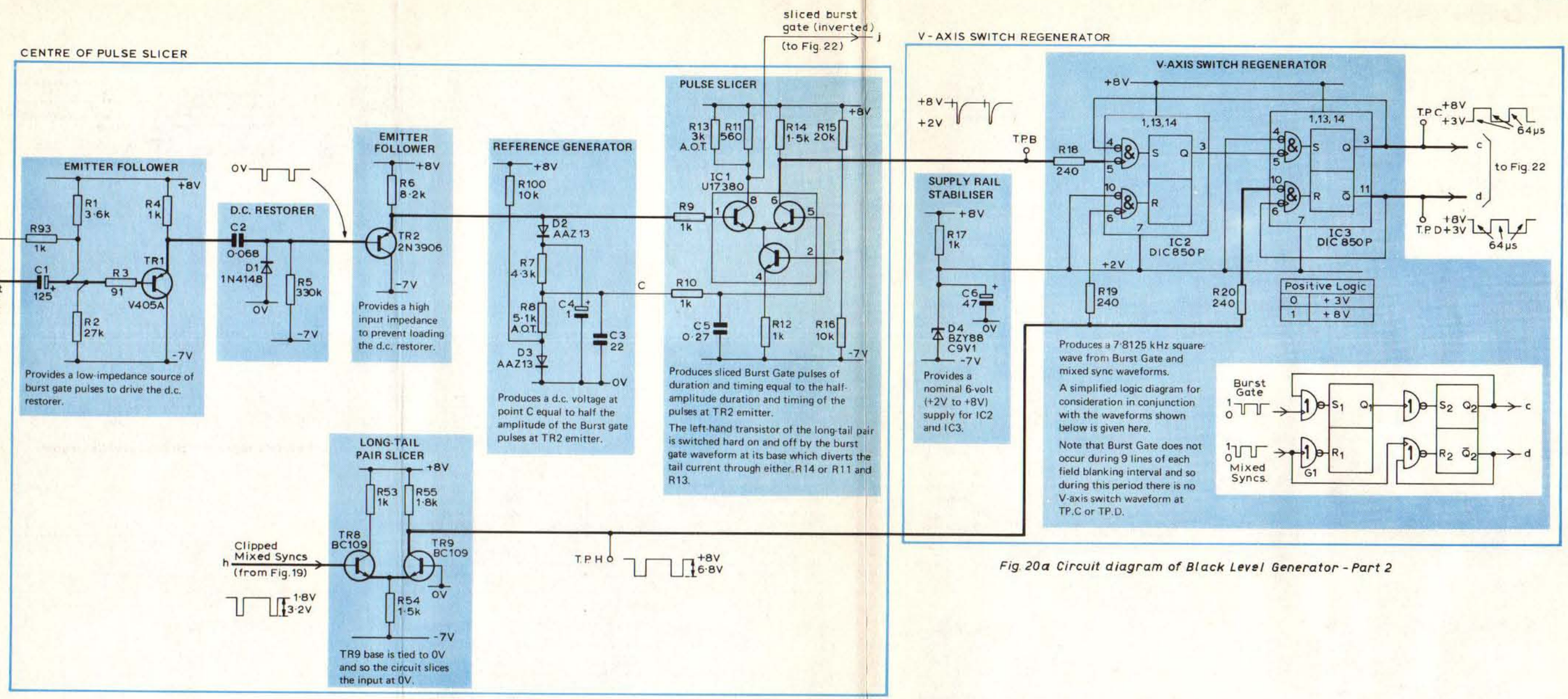


Fig. 20a Circuit diagram of Black Level Generator - Part 2

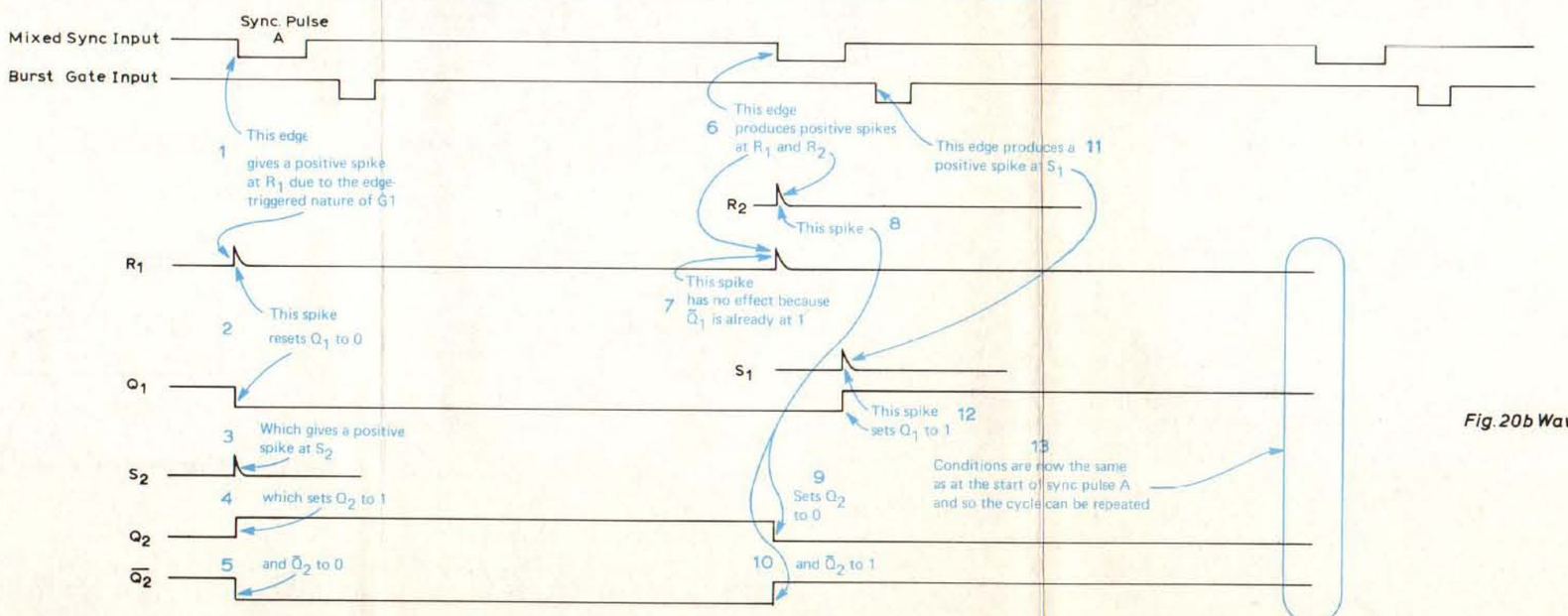


Fig. 20b Waveforms in the V.A.S. regenerator

INPUT AMPLIFIER

A double emitter follower providing a low-impedance feed of subcarrier for the ±45° phase-shift circuit.

Feedback from the junction of R24 and R25 to the collector of TR3 varies TR3 collector voltage in sympathy with its base. This reduces the change in collector-base capacitance in TR3 and hence minimises differential phase distortion.

±45° PHASE SHIFT

C9, C13, R28 and R29 provide a phase shift of +45°.

C10, R27 and C14 provide a phase shift of −45°.

Signals at TR5 and TR6 collectors are thus 90° different in phase.

SUBCARRIER PHASE SWITCH

Antiphased V-axis switch waveforms switch TR5 and TR6 alternately to provide alternate lines of +45° and −45° subcarrier.

L1 is the load across which the switched subcarrier is developed; an inductor is used rather than a resistor to prevent a change in d.c. conditions as the transistors switch.

TEMPERATURE COMPENSATED EMITTER FOLLOWER

Provides subcarrier at pin 1 and a steady d.c. potential at pin 7. These feed the *subcarrier* input of the balanced modulator, IC5.

Variation of the d.c. potential at pin 7 relative to that at pin 1 adjusts the carrier balance in the modulator.

As the temperature changes the d.c. conditions at pins 1 and 7 change together; this ensures that the carrier balance does not change with temperature.

IC No.	TYPE	VIEW ON LEADS
IC5	LIC 796 G (equiv. to Motorola M1596)	1 10
IC4 IC6	SL301A	1 8
	BC109 V405A	c b e
	BF115	c s e b

Fig. 21. Circuit Diagram of Black Level Generator - part 3

BALANCED MODULATOR

C48 and R98 provide feedback to improve the shape of the burst at the output of the modulator.

AMPLIFIER

HARMONIC FILTER

Filters off 2nd and 3rd harmonics from the Balanced Modulator output.

BURST-SHAPING FILTER

EMITTER FOLLOWER

Provides a low-impedance feed of shaped inverted burst gate pulses to drive the d.c. restorer.

TEMPERATURE COMPENSATED D.C. RESTORER

Provides shaped burst gate pulses at point k and a steady d.c. potential at point e.

In order to maintain correct carrier balance in the modulator the d.c. conditions at points e and k must be the same. The potential at point e is set by the resistor chain R72 to R76 and the forward volt drop across IC6b. The potential at point k can be matched to this by adjustment of R73.

The volt drop across IC6a changes with temperature thus altering the potential at point k, but this is matched by a similar alteration in the potential at point e due to the change in volt drop across IC6b.

Note that IC6 comprises a pair of transistors which are connected as diodes in this application.

Fig. 22. Circuit Diagram of Black Level Generator - part 4

GE4/543/22A
GE4/543/22B

OUTPUT BOARD CIRCUITS

No.	TYPE	BASE view on leads
TR2,3,5,6	2N3904	c b e
TR1,4	2N3906	
IC1,2,3	U17830	1 8

IC No.	TYPE	BASE View on Top
4,5,6,7, 8,9,10,11	58CPX00 233BAA	Mark on IC indicates pin 1; 1 10; 20 11

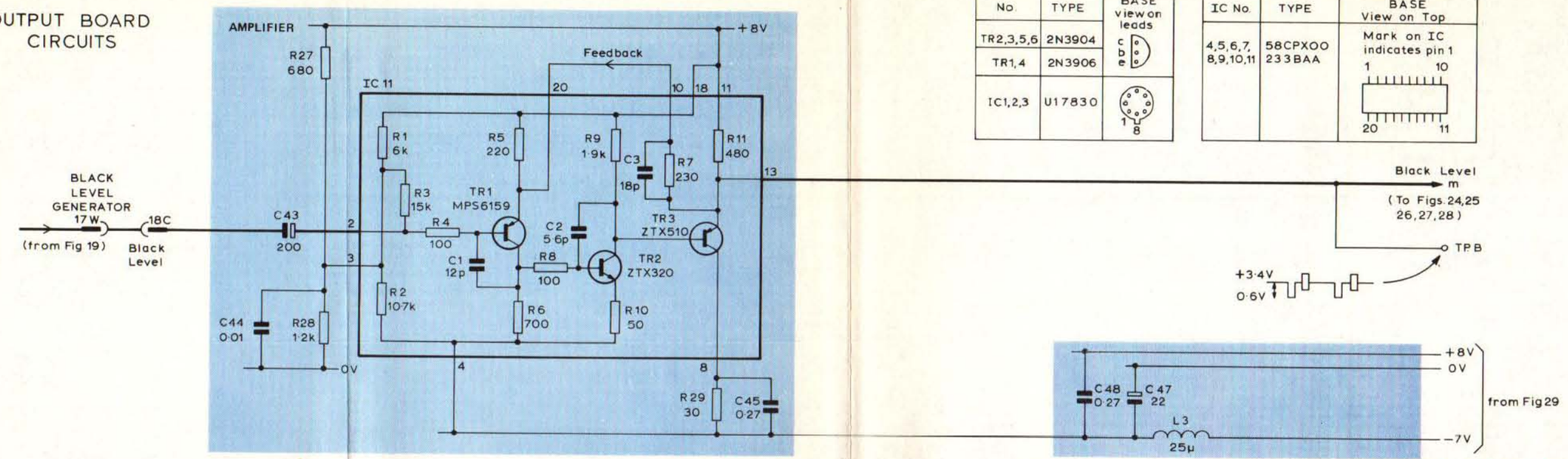


Fig 23. Black Level Amplifier Circuit

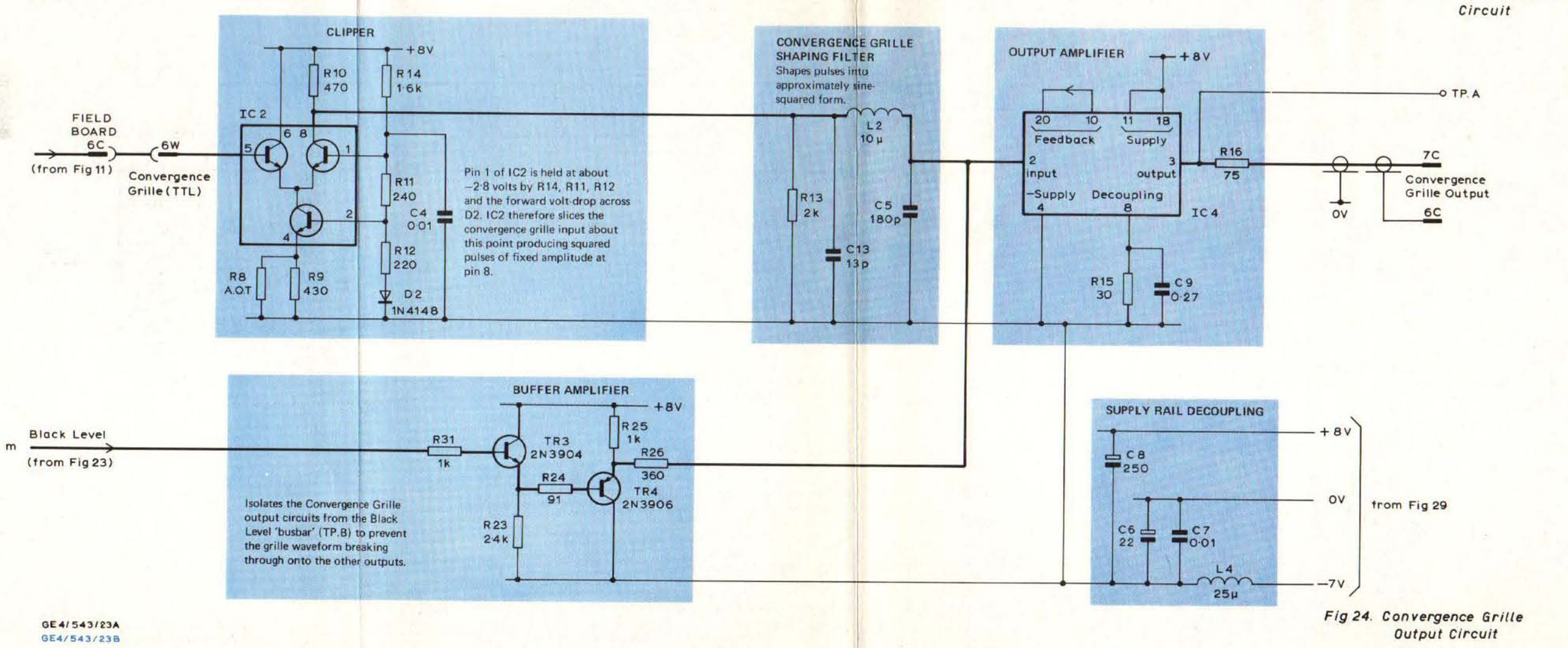


Fig 24. Convergence Grille Output Circuit

GE4/543/23A
GE4/543/23B

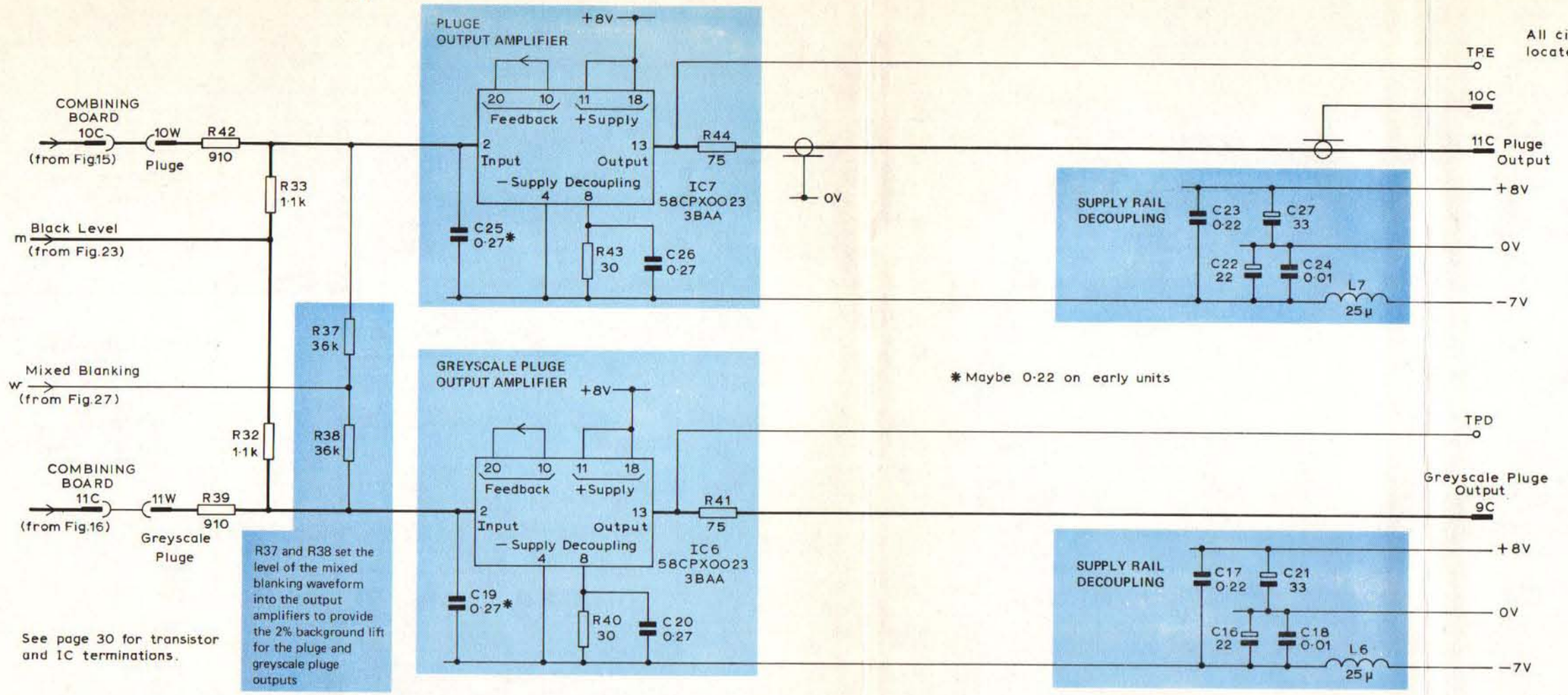


Fig.25 Pluge and Greyscale Pluge Output Circuit

Fig.26 Linearity Grille Output Circuit

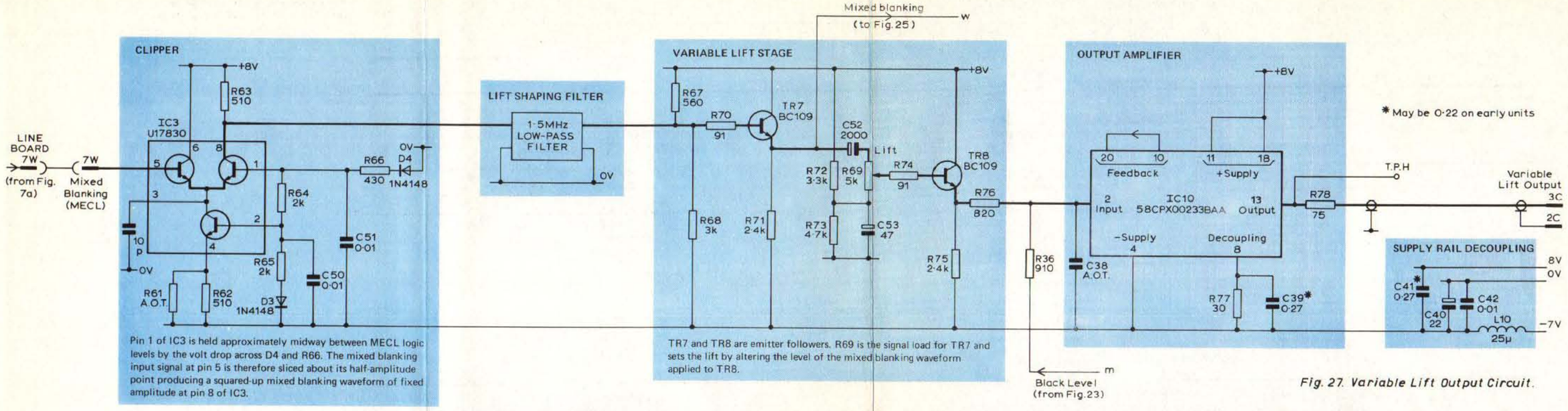
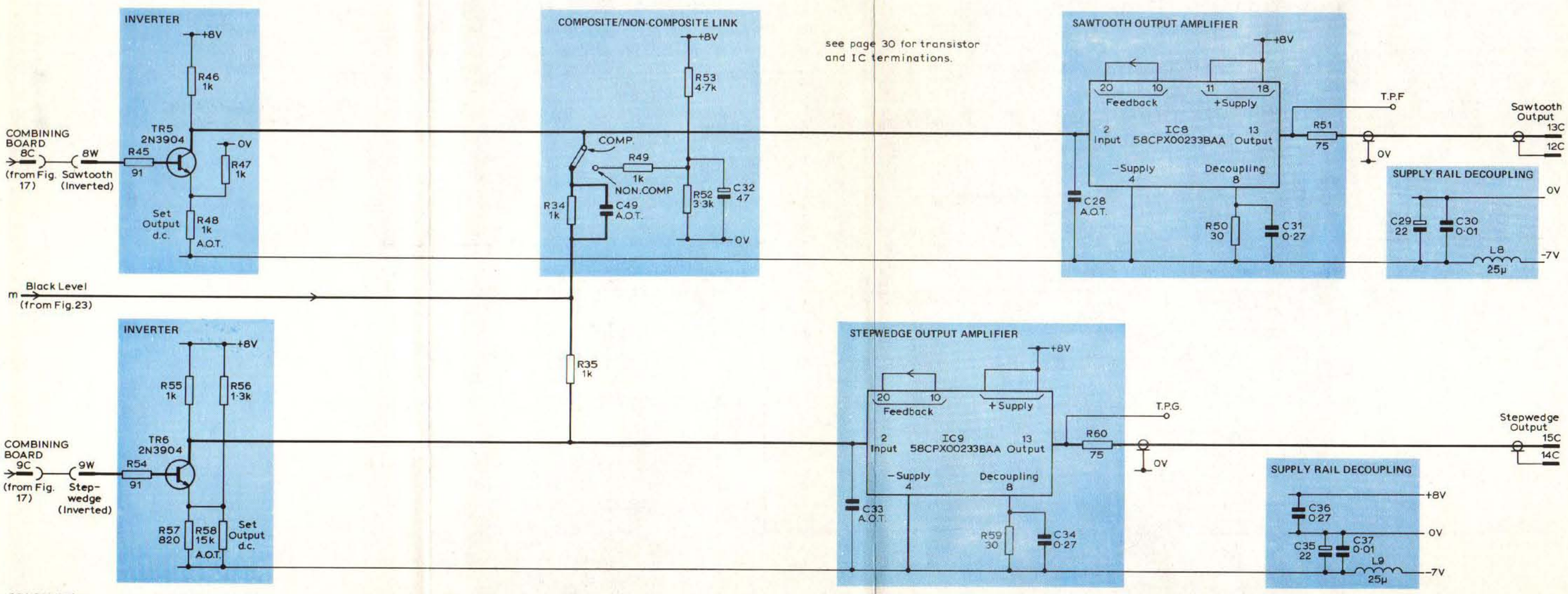


Fig. 27. Variable Lift Output Circuit.

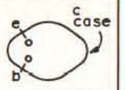
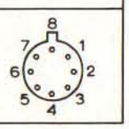
see page 30 for transistor and IC terminations.



GE4/543/25A
GE4/543/25B

Fig. 28. Sawtooth and Stepwedge Output Circuits.

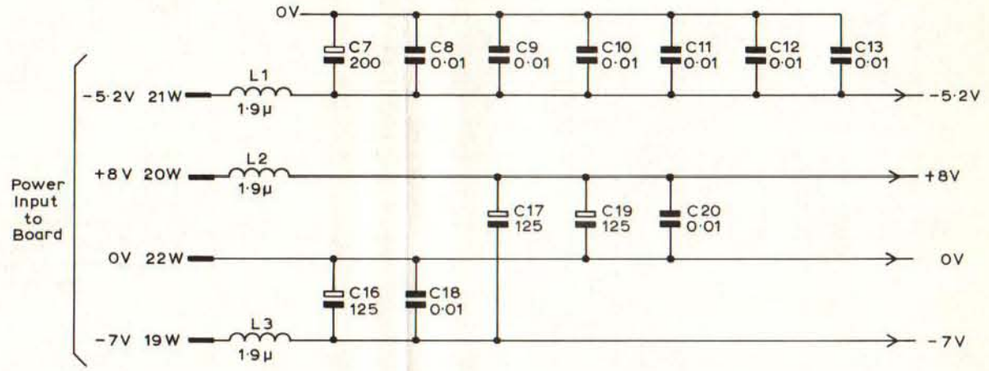
POWER SUPPLY

Circuit No	Base view on leads
BC109	
BFY52	
2N3055	
U17830	

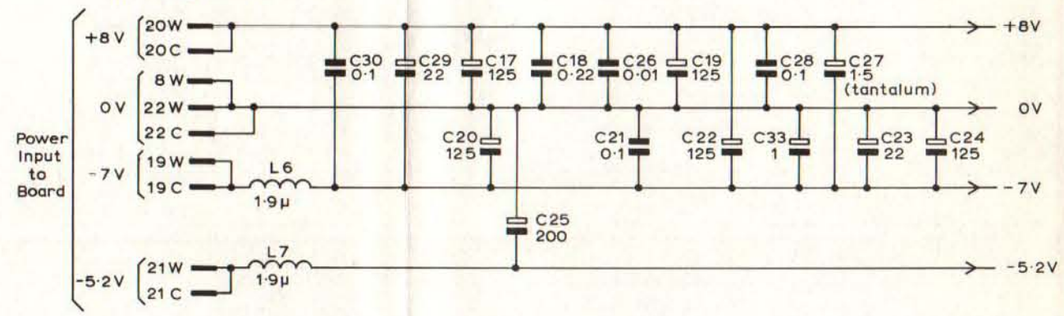
GE4/543/26A
GE4/543/26B

Fig 29. Circuit Diagram of Power Supply

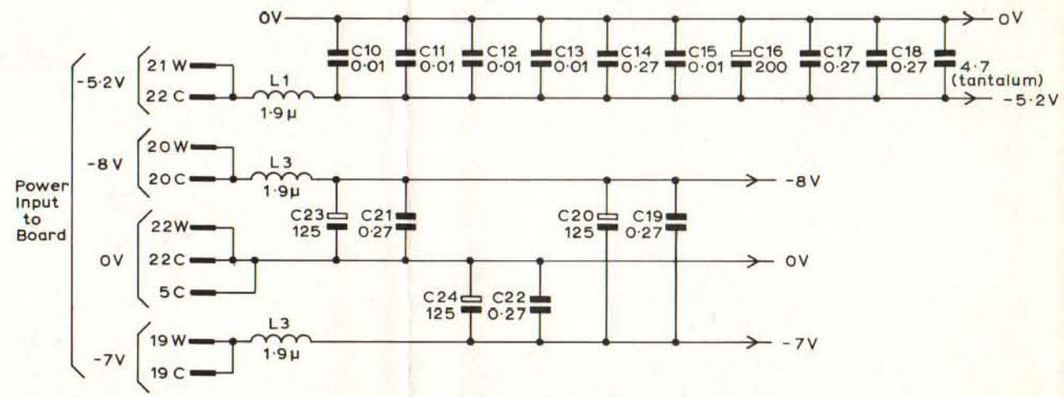
Line Board (No.1)



Combining Board (No.2)

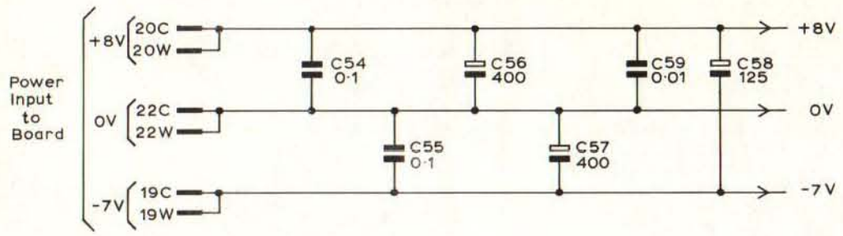


Field Board (No. 3)

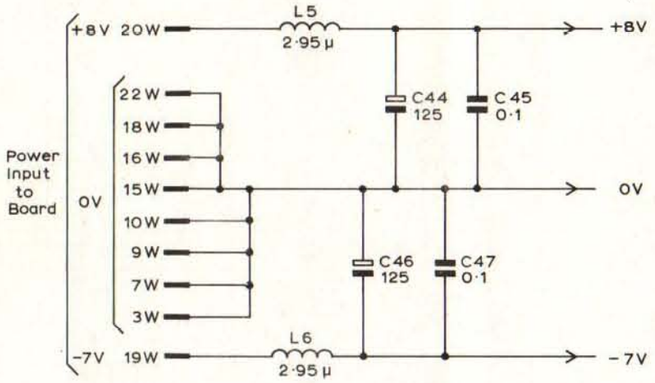


GE4/543/30

Output Board (No.4)



Black Level Generator (No.5)



Interconnection Board (No. 7)

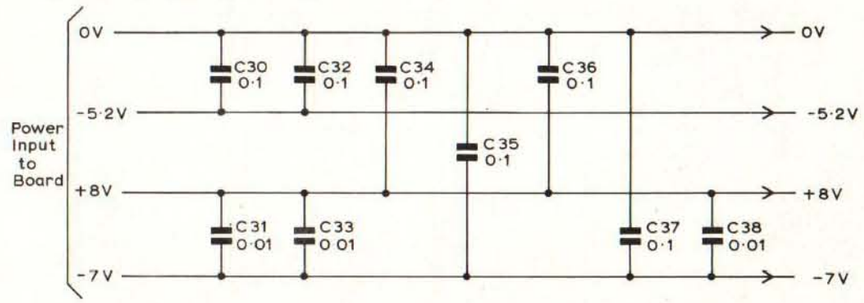


Fig.30. Board Decoupling Circuits