GATE PULSE GENERATOR GE2/574

Introduction

The GE2/574 accepts mixed-sync pulses and provides a field-frequency output of positive-going gating pulses[1]. The output occurs during the field-blanking period on the later part of one line or two lines as determined by the setting of the *Line Selection* and *One Line/Two Line* switches.

Three monitor outputs are provided (for odd fields, even fields and all fields). These outputs can be used to trigger an oscilloscope at the beginning of the selected line.

The unit contains also a PS2/22B 12-volt Power Supplier; this is normally used to power a crystal oven[2]; the power required by the Gate Pulse Generator section of the GE2/574 (at +6 volts and −6 volts) is provided by an associated unit[3]. However, if the GE2/574 is to be used by itself, the PS2/22B can be modified (see Test Procedure) and used to power the Gate Pulse Generator.

General Specification

Chassis	CH1/12A
Index peg positions	22 and 43
Pulse Generator	
Mixed-sync input	2 V p-p
Input impedance	high w.r.t. 75 ohms
Gate pulse output	2 V p-p positive-going across a 75-ohm load
Output impedance	75 ohms
Monitor outputs	2 V p-p across a high-impedance load
Monitor output impedances	470 ohms
Power Requirements	± 6V, 75 mA d.c.
Power Supplier	
Mains input	220—250 V, 50 Hz
Power Output	12 V d.c. isolated, 0·5 A max

Circuit Description

A block diagram of the unit is given in Fig. 1 and a circuit diagram in Fig. 2. The waveforms present at various points in the circuit under normal operating conditions are shown in Fig. 3. The *And* and *Nand* (*Nand* = *And* plus inverter) gates in the circuit provide outputs only when negative-going voltages are present on both inputs; i.e. they use negative logic.

The mixed-sync input signal to the unit is applied, via an emitter-coupled amplifier comprising transistors TR1 and TR2, to emitter follower TR3. From TR3 the signal is fed, via a differentiating network and a diode which removes the positive-going spike, to the base of TR4. Transistors TR4 and TR5 form a line-rate monostable multivibrator. The duration of the unstable state is such that the stage does not respond to the twice-line-frequency pulses present during the field-sync and equalising-pulse periods; thus the output of the stage does not contain a field component.

The line-frequency waveform developed at the collector of TR5 is fed via inverter TR6 to one input of a two-input *Nand* gate formed by D3, D4 and TR7. The other input to the gate consists of sync pulses from the collector of TR2 and the two voltages are simultaneously negative only during certain of the field-sync pulses (twice on even fields and three times on odd fields as shown in Fig. 3, waveforms 1 and 2). When both inputs are negative, the gate diodes are reverse-biased and transistor TR7 is cut off. Thus a positive-going field-interval pulse train consisting of two or three line-frequency pulses (see Fig. 3, waveform 3) appears at the collector of TR7. This pulse train is applied via emitter-follower TR8 to amplifier-inverter stage TR9. Transistor TR9 drives the monostable delay multivibrator formed by transistors TR10, TR11 and TR12, and the start of the delay is initiated by the trailing edge of the last pulse in each pulse train. The duration of the delay depends on the setting of the *Line Selection* switch.

The positive-going field-frequency pulse developed at the collector of TR10 is differentiated and applied to the base of TR13. Transistors TR13 and TR14 form a monostable stage which provides a delay of one line and the output from the collector of TR14 is applied to *Nand* gate 2 in conjunction with mixed-sync pulses from the collector of TR2. Thus the gate is operated for one line-sync period in each field. The inverted sync-pulse developed at the collector of TR15 is differentiated and fed to the One-line/Two-lines monostable multivibrator formed by transistors TR16 and TR17. Transistor TR17 provides a negative-going field-frequency output with a duration either of 70—75 μs or of 140—150 μs, depending on the position of switch SB, and this pulse drives *Nand* gate 3 in conjunction with line-frequency pulses derived from the

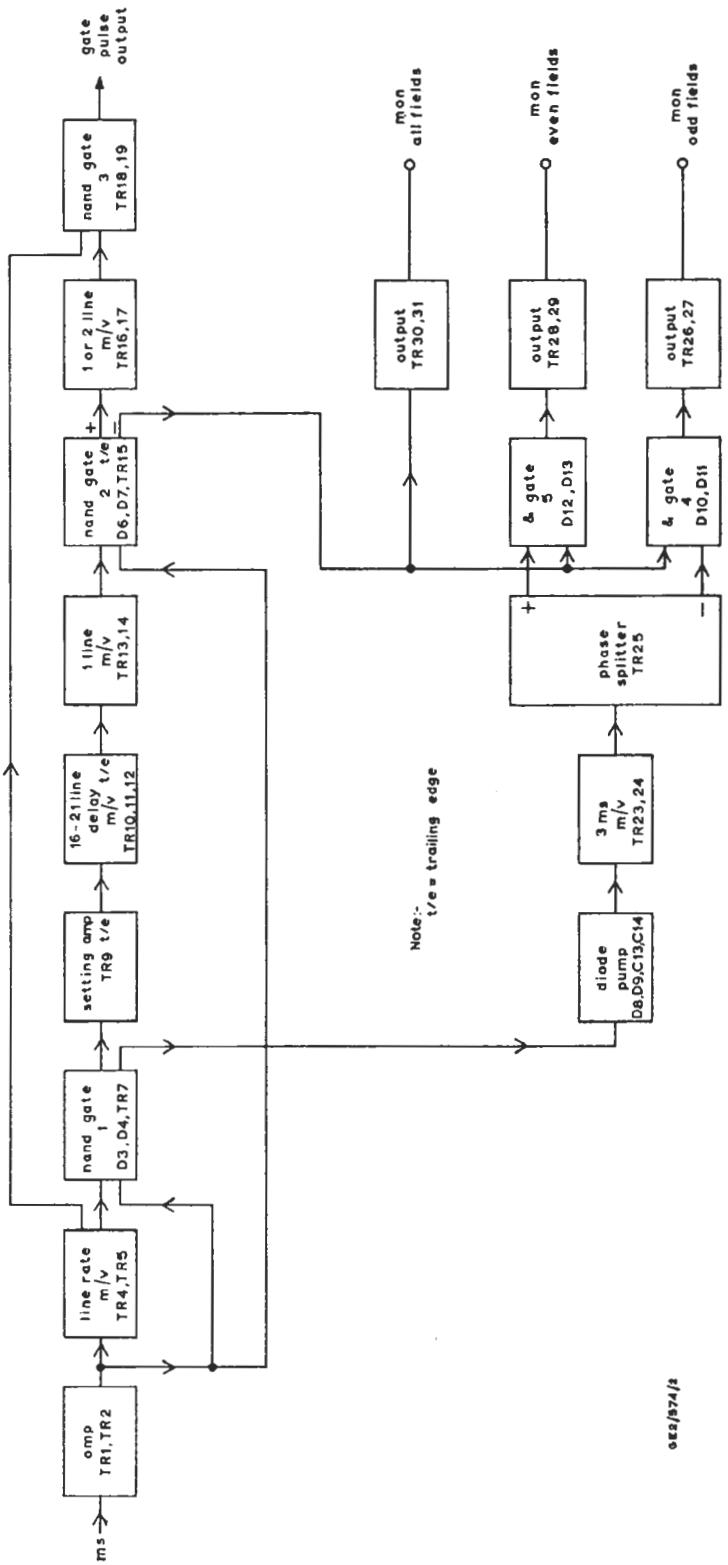

Fig. 1 Block Diagram of the Gate-pulse Generator GE2/574

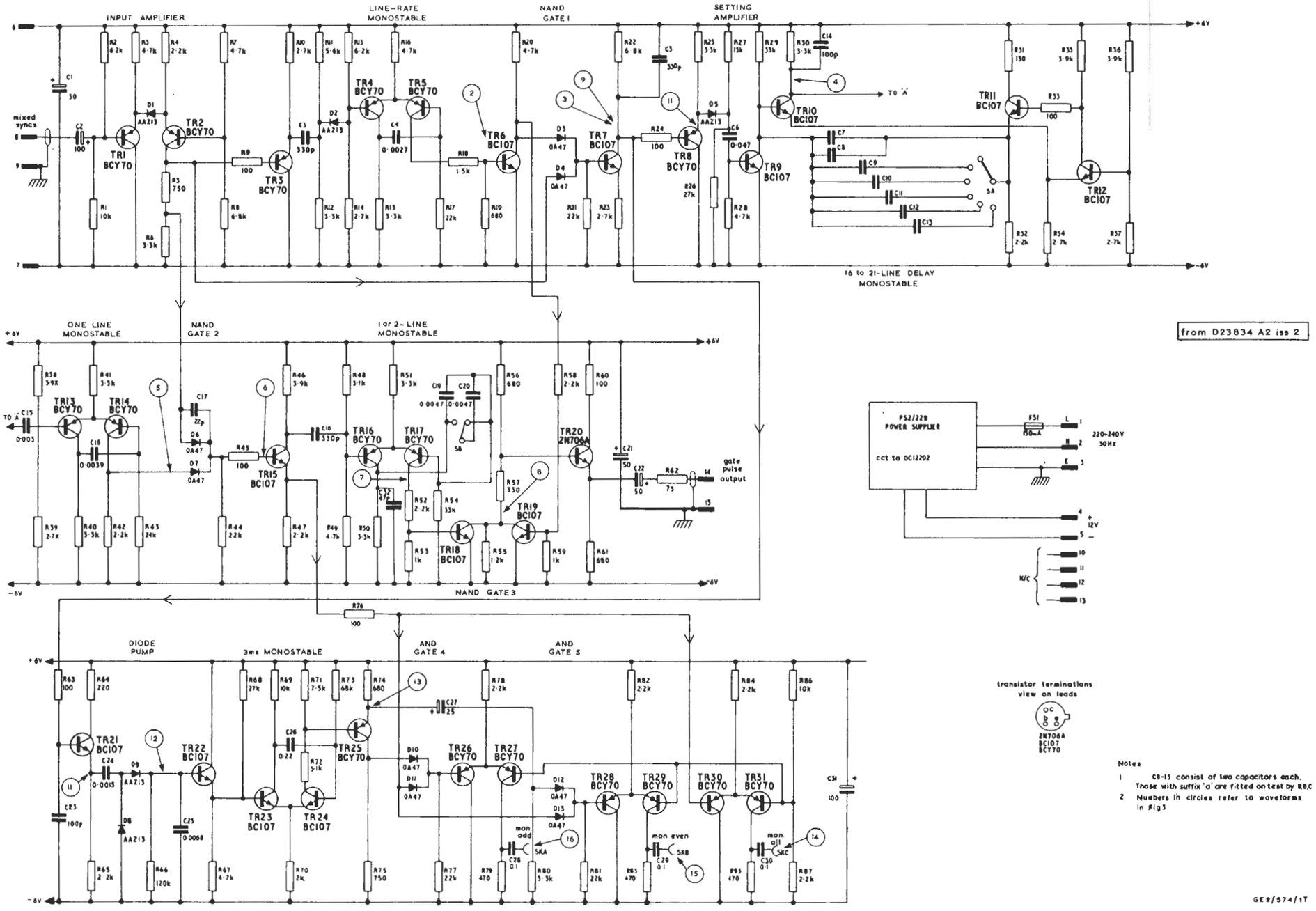

Fig. 2 Circuit of the Gate-Pulse Generator GE2/574

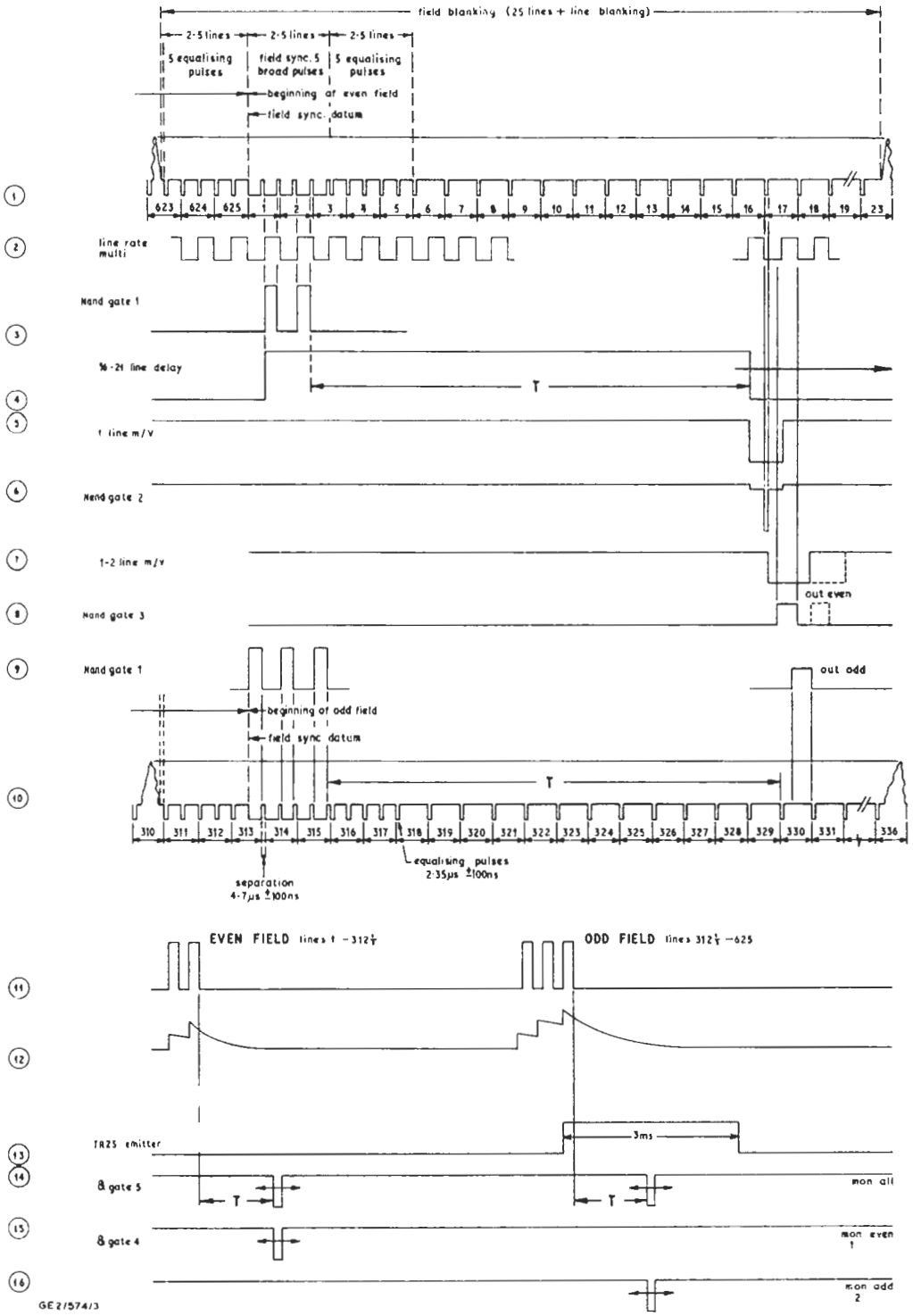

Fig. 3 Waveforms in the Gate-pulse Generator GE2/574

collector of TR6. The gate output consists of either one or two positive-going field-frequency pulses (depending on the position of switch SB) and this signal is applied via emitter-follower TR20 to the *Gate Pulse* output of the unit.

In addition to feeding TR8, the field-interval pulse trains which are produced during field-sync periods by *Nand* gate 1 are applied via TR22 to a diode-pump circuit comprising C24, D8, D9 and C25. The amplitude of the output is dependent on the number of pulses (two or three) which are applied to the pump circuit during each field-sync period. During even fields, only two pulses are received and the resultant output has insufficient amplitude to trigger the subsequent three-millisecond-delay multivibrator formed by transistors TR23 and TR24. During odd fields, three pulses are received by the pump circuit and the output of the circuit is of sufficient amplitude to change the state of the multivibrator. Thus the three-millisecond multivibrator is triggered only on odd fields.

When the multivibrator is in its unstable state, the phase-splitter TR25 is cut off and the negative potential present at the collector of TR25 is applied to *And* gate 4 in conjunction with the emitter potential of TR15. The gate produces an output only during the selected line period on odd fields. This output is fed, via the long-tailed pair amplifier comprising transistors TR26 and TR27, to the *Mon. Odd* output socket.

The potential present at the emitter of TR25 is applied to *And* gate 5 in conjunction with the output from the emitter of TR15. During the selected line period on odd fields the emitter potential of TR25 is positive and the action of the gate is inhibited. Thus the gate operates only during the selected line period on even fields. The gate output is fed via the long-tailed pair output amplifier comprising transistors TR28 and TR29 to the *Mon. Even* output socket.

Transistors TR30 and TR31 form a long-tailed pair stage which provides an output whenever the emitter potential of TR15 is negative-going. Thus the stage provides an output during the selected line period on both odd and even fields and this is applied to the *Mon. All* output socket.

Test Procedure

The GE2/574 normally forms part of a larger unit[1] from which it derives power supplies and a sync-pulse input signal. If the GE2/574 is tested by itself the connector shown in Fig. 4 will be required

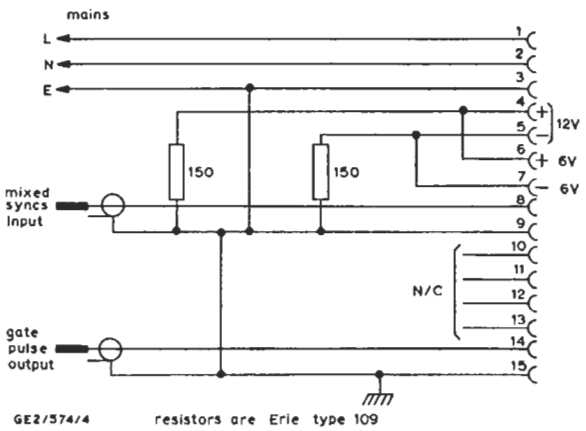

Fig. 4 Test Connector for the GE2/574

to derive power supplies at ±6 volts from the built-in PS2/22B Power Supplier; additionally, a feed of mixed-sync pulses will be required. Note that the unit has a high-impedance input; therefore if an unterminated feed of sync pulses is used it must be attenuated to reduce the input level to 2 volts peak-to-peak.

Equipment Required

Model 8 Avometer.
High-grade double-beam oscilloscope with delaying sweep facilities and two high-impedance probes.
0—9 dB precision attenuator.

Checks

The waveforms referred to below are all given in Fig. 3.

1. Check that the potentials between pin 4 and chassis and between pin 5 and chassis are +12 V and −12 V respectively.
   Check that the potentials between pin 6 and chassis and between pin 7 and chassis are +6 and −6 volts respectively.
2. Check that the sync input level is 2 volts (±0·2 volts) peak-to-peak.
3. Set the *Line Selection* switch to *17* and the *One Line/Two Line* switch to *One Line*.
4. Use a high-impedance probe to monitor the signal at the base of TR6.
   Check that a line-frequency waveform (see waveform 2) is present and that no field components are visible. Check that the duration of the negative-going portion of the waveform is 33 to 34 μs. Alter the level of the sync input signal by +3 dB and −3 dB and check that in

both instances the waveform at the base of TR6 remains unchanged.

5. Monitor the signal at the collector of TR10 and check that a field-frequency pulse (see waveform 4) is present. The trailing edge of the pulse should be steady and should occur about 16 lines after the start of the field.
   Monitor at the emitters of transistors TR8 and TR21 and check that a two-three pulse field-separation signal (see waveform 11) is present.
6. Monitor at the anode of D7 and check that the pulse duration is 60 µs ±3 µs.
   Use the double-beam facility of the oscilloscope to compare this pulse with the mixed-sync input pulse present at the beginning of line 17 (even fields) or line 330 (odd fields). The mixed-sync pulse should occur in the centre (±5 µs) of the 60-µs pulse. If it does not, the value of C8 must be adjusted.
7. Repeat step 6 for lines 18 to 22. If pulse-timing errors are present, adjust the appropriate capacitors accordingly.
8. Check that the pulse duration at the collector of TR17 is 70 to 75 µs with the *One Line/Two Lines* switch in the *One Line* position, and 140 to 150 µs with the switch in the *Two Lines* position.
9. Check that a 2-volt peak-to-peak (±5%) positive-going, field-frequency pulse is present at pin 14 when the output is terminated in 75 ohms.
   Observe the output waveform while operating the *Line Selection* and *One Line/Two Lines* switches to check that the switches function correctly.
10. Check that the waveform present at the base of TR22 is as shown in waveform 12. Check that a once-per-picture pulse with a duration of 3 to 5 milliseconds (see waveform 13) is present at the emitter of TR25.
11. Check that monitor pulses (as shown in waveforms 14, 15 and 16) appear at the appropriate test points and check that these pulses have an amplitude of 2 volts peak-to-peak.

References to Typical Associated Equipment

1. Remote Signal Analyser EP1/508.
2. Burst-locked Oscillator OS1/502.
3. Sync Separator UN1/540.

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