

WAVEFORM TIMING GENERATOR GE2/540

Introduction

The GE2/540 provides seven separately delayed trigger pulses from a negative-going input pulse which can occur at field-rate, line-rate, or at random. It is suitable for use on any television standard but requires selection of timing capacitors for each standard.

The unit is mounted on a CH12A chassis with index pegs 15 and 23.

General Specification

Input Signal Level (Negative going trigger pulses)	2 volts p-p
Input Impedance	75 ohms or greater than 2 kilohms
Output Pulses (across greater than 2 kilohms)	approx. 2 volts negative
Range of Delay	6 μ s to greater than 100 μ s
Temperature Range	5° to 45°
Variation of Delay within Temperature Range	less than $\pm 1\%$
Power Requirements	40 mA at -12 V stabilised

Circuit Description

The circuit diagram is given in Fig. 1 where only two of the seven trigger circuits are shown.

The negative-going input pulse is first differentiated and then amplified and inverted. It is then used to trigger the delay multivibrators TR4/TR5 etc. With reference to circuit A transistor TR5, which is normally conducting, is turned off and a positive going pulse appears at the collector. This pulse, the duration of which depends on C6 and RV1, is differentiated by C7 in conjunction with

R17 and R18 and the input circuit of the following unit^{1,2}. The positive-going component is suppressed by D5. If required, blanking pulses from the collector of TR3 can be added at this point. Thus, at the output there appears a negative pulse delayed with respect to the leading edge of the input pulse. The pulses at the other outputs are generated in the same way but with individual delays as required by the associated units.

When the unit is used as part of the GE4M/518A Test Line Signal Generator and Inserter, only 5 of the 7 circuits are required and the values of C6, C9 and the corresponding capacitors, C12, C15 and C18 in the next 3 circuits are given in Table 1 along with the delays of the negative-going output pulses.

TABLE 1

Circuit	Capacitor		Delay
A	C6	430 μ F	16.5 μ s
B	C9	470 μ F	18.5 μ s
C	C12	620 μ F	23.5 μ s
D	C15	1100 μ F	43.5 μ s
E	C18	1500 μ F	58.5 μ s

Maintenance

Routine maintenance is not required but the amplitude of the output pulses and their timings should be checked occasionally.

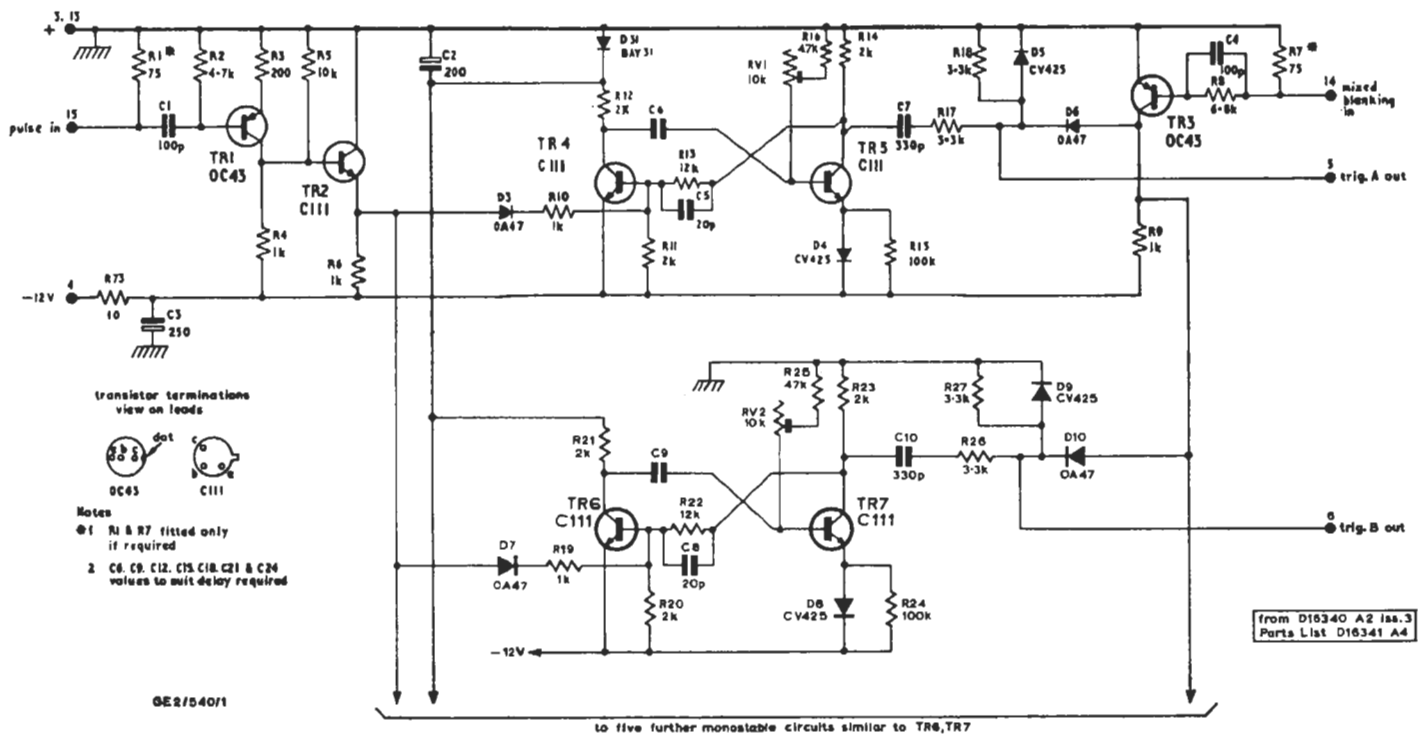
References

1. GE4/516 Pulse and Bar Generator
2. GE2/517 Staircase and Pedestal Generator
3. GE4M/518A Test Line Signal Generator and Inserter.
4. Designs Department Specification 9.64(66)

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See overleaf for Fig. 1.

Fig. 1 Circuit of the Waveform Timing Generator GE2/540



transistor terminations
view on leads



- Notes
- 1 R1 & R7 fitted only if required
 - 2 C6, C9, C12, C15, C18, C21 & C24 values to suit delay required

GE2/540/1

from D15340 A2 Iss.3
Parts List D16341 A4

to five further monostable circuits similar to TR6,TR7