SWITCH PULSE GENERATORS GE2/520 AND GE2/520A

GE2/520,A 1

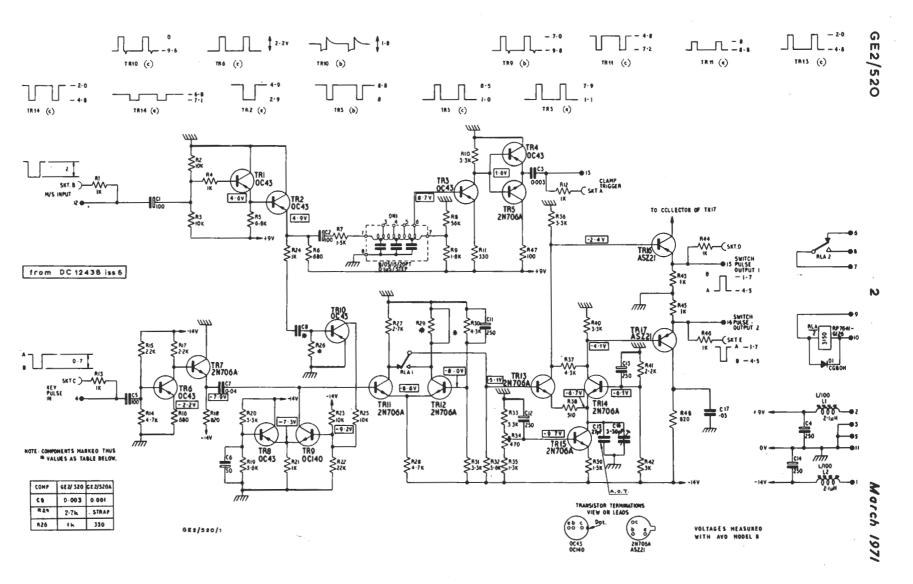


Fig.1. Circuit of the Switch-pulse Generator GE2/520, A

#### Introduction

The GE2/520 accepts a keying waveform and mixed sync-pulses; it produces two clamped keying waveforms of opposite polarity and a clamp trigger pulse.

The GE2/520 is constructed on a CH1/12A chassis with index-peg positions 7 and 13.

# Circuit Description

The circuit of the GE2/520 is given in Fig. 1. Mixed sync-pulses, delayed by a network DN1 and inverted by transistor TR4, are fed to a complementary emitter follower output stage. The output is fed to the load via a capacitor so as to differentiate the output waveform for low values of load resistor.

Mixed sync-pulses are also fed via transistor TR10 to the base of a switching transistor TR9 causing its emitter-collector impedance to drop to a value of a few ohms during the sync-pulses. This clamps the inverted keying waveform at the base of transistor TR11. Transistors TR11 and TR12 form part of a long-tailed pair giving complementary outputs, one of which is selected by means of relay contact RLA-1. Capacitors C9 and C10, connected across the collector loads, slow up the rise-time of the outputs. The selected output is fed to a long-tailed pair used as a phase splitter. Transistor TR15 provides a high-

impedance source (long-tail) for transistors TR13 and TR14. Potential divider R34 and capacitor C16 are adjusted to give minimum transients on an external switched waveform.

The complementary outputs of transistors TR13 and TR14 are each fed to an emitter follower output stage.

# GE2/520A

GE2/520A differs in that:

- (a) C10 is short-circuited.
- (b) C8 is 0.001  $\mu$ F.
- (c) R26 is 330 ohms.

Thus one of the output keying-waveforms is removed.

#### Test Procedure

Routine maintenance is not required and there are no operational controls to be adjusted. The presets R14 and C16 are set during the line-up of the parent unit, e.g., PA18/518 or PA18/522. It is convenient to check the unit when it is plugged into the parent unit; the waveforms as indicated in Fig. 1 should be obtained.

### Reference

1. Designs Department Specification No. 8.157(64)

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