CHROMINANCE EQUALISER EQ5/517

Introduction

The EQ5/517 accepts four one-volt p-p composite colour-video signals and a d.c. control signal; it produces an output composite video signal at −15 dB. The magnitude of the chrominance component in the output signal is controlled by the d.c. signal.

The equaliser is built on a CH1/12A chassis with index pegs in positions 11 and 38.

General Specification

Inputs	Four composite colour-video signals at 1 volt p-p (0 dB). D.C. chrominance-control signal.
Output	One composite video signal at −15 dB.
Input and Output Impedance	75 ohms.
Power Requirements	+12 and −12 volts d.c.

Principle of Operation (Fig. 1)

The EQ5/517 has an amplitude/frequency characteristic which can be varied without affecting the group delay/frequency characteristic of the link in which the equaliser is placed. The principle of operation is indicated in Fig. 1. A video input E_{in}, vector OA, is delayed by a time t seconds, vector OB. A proportion of a correcting signal E_c is added to the delayed input signal E_t to give the required amplitude/frequency characteristic. The theory of operation is given in more detail at the end of this Instruction.

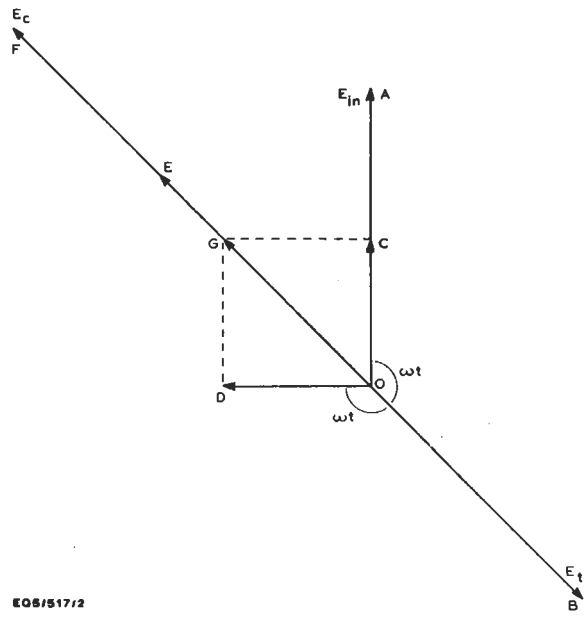

Fig. 1 Vector Diagram Showing the Principle of Operation of the EQ5/517

General Description (Figs. 1 and 2)

Fig. 2 is a block diagram of the equaliser. The encircled letters on the diagram refer to the vectors shown in Fig. 1.

Four video inputs are applied to the unit. The signals, represented by vectors OC, OD and OE, are derived as shown and applied to an adding network. The output of this network is the correction signal.

The correction signal is fed through two parallel paths to another adding network. One path includes a variable attenuator and the other path includes an inverting amplifier. The variable attenuator is controlled by the d.c. signal and hence positive, zero or

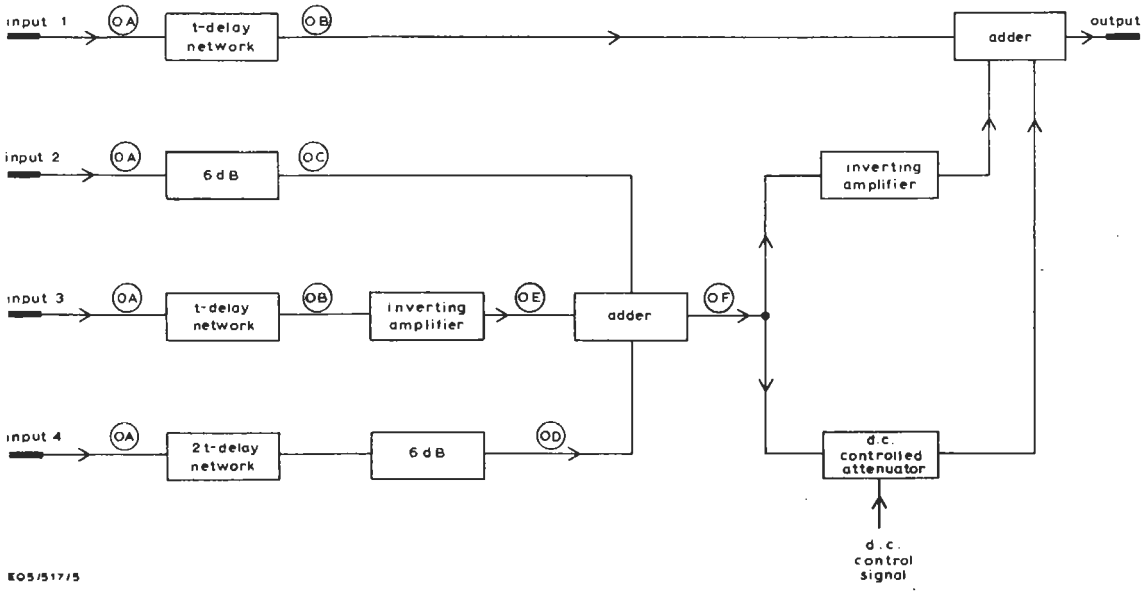

Fig. 2 Block Diagram of the EQ5/517

negative values of correction signal can be added to the delayed input signal, vector OB, to give the equalised signal.

Circuit Description (Fig. 3)

Fig. 3 is a circuit diagram of the EQ5/517.

Three of the video input signals are passed through delay networks* which are adjusted to take into account the inherent delays in amplifying stages in the equaliser. Transistors TR1, TR2, TR3 and TR4, TR5, TR6 compose two separate inverting amplifiers. Each amplifier consists of three stages, a common-base, a common-emitter and an emitter-follower. A 3·3-μF capacitor provides some phase correction.

The d.c. control signal is applied to pin PLA6; pin PLA7 is normally connected to chassis. Transistors TR7 and TR9 form a long-tailed-pair differential amplifier and transistor TR8 provides a constant current source. The current through transistor TR9 is varied by the control signal and measured by meter ME1. Resistor R39, in the emitter circuit of transistor TR8, allows the nominal value of the d.c. controlled attenuator to be adjusted.

The d.c. controlled attenuator is placed between two similar non-inverting amplifiers TR10, TR11 and TR12, TR13. These are each two-stage direct-coupled negative-feedback circuits.

The working value of the attenuator is controlled by a variable resistor. This resistor comprises a cadmium-selenide photoconductive element and a miniature incandescent lamp; both items are sealed in a TO-5 transistor case. The electrical conductivity of the element varies with the incident illumination. A voltage of between zero and four volts d.c. applied to the lamp makes the cell resistance vary from about 350 megohms to 200 ohms.

Fixed attenuation and summation are achieved by simple resistive circuits.

Maintenance

Table 1 is a list of voltages measured with no signal input using an Avometer Model 8. Readings of under one volt were made on the 2·5-volt d.c. scale and other measurements on the 25-volt d.c. scale.

TABLE 1

Transistor	*Emitter*	*Base*	*Collector*
TR1	0·66	0	–7·2
TR2	–7·5	–7·2	3·3
TR3	2·7	3·3	7·8
TR4	0·68	0	–6·6
TR5	7·2	–6·6	2·4
TR6	1·7	2·4	8·2
TR7	–1·1	–0·35	7·2
TR8	–3·4	–2·7	–1·1
TR9	–0·65	0	5·1
TR10	6·3	5·7	–4·5
TR11	–5·2	–4·5	0·1
TR12	5·9	5·2	–4·5
TR13	–5·2	–4·5	–0·7

* Delay Networks with Complex Conjugate m Values: Designs Department Technical Memorandum 9.19(61).

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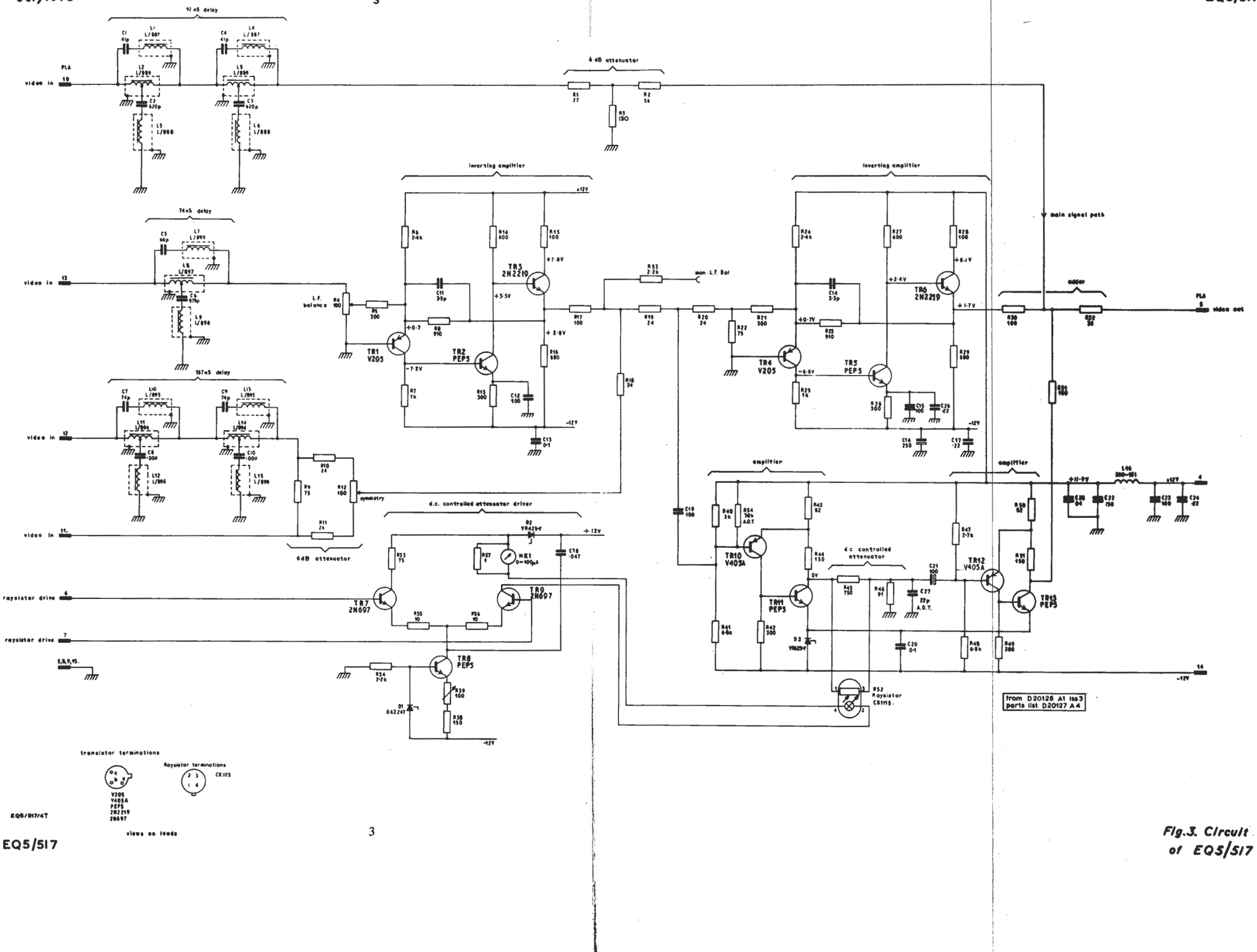

EQ5/517

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Fig.3. Circuit of EQ5/517

Test Procedure

The equaliser is tested as part of its parent unit.

Theory of Operation (Figs. 1 and 4)

The correcting signal has three components, shown in Fig. 1. These are:

(a) An undelayed signal of magnitude $E_{in}/2$, vector OC.

(b) A signal of magnitude $E_{in}/2$ delayed by 2t seconds, vector OD.

(c) A signal of magnitude E_{in} delayed by t seconds and reversed in phase, vector OE.

The resultant of these three components is the correcting signal E_c, represented by vector OF. The correcting signal does not have a component at right-angles to the delayed input signal E_t and therefore has no effect upon the phase/frequency-characteristic of the equaliser, which is a straight line with a uniform delay of t seconds.

If a proportion k of the correcting signal is added to E_t, the output of the equaliser is either increased or reduced in magnitude depending upon the sign of k. The magnitude of the output signal is given by

$$E_{out} = E_t + kE_c.$$

It can be shown that

$$E_{out}/E_{in} = 1 - k + k \cos \omega t.$$

The value of t for the EQ5/517 is 83 ns. Fig. 4 shows the function E_{out}/E_{in} plotted against frequency for three different values of k. At a frequency of 4·43 MHz a k value of −0·6 gives an h.f. boost of 6 dB, the response is flat if k is 0, and when k is 0·22 the response is reduced by 4 dB.

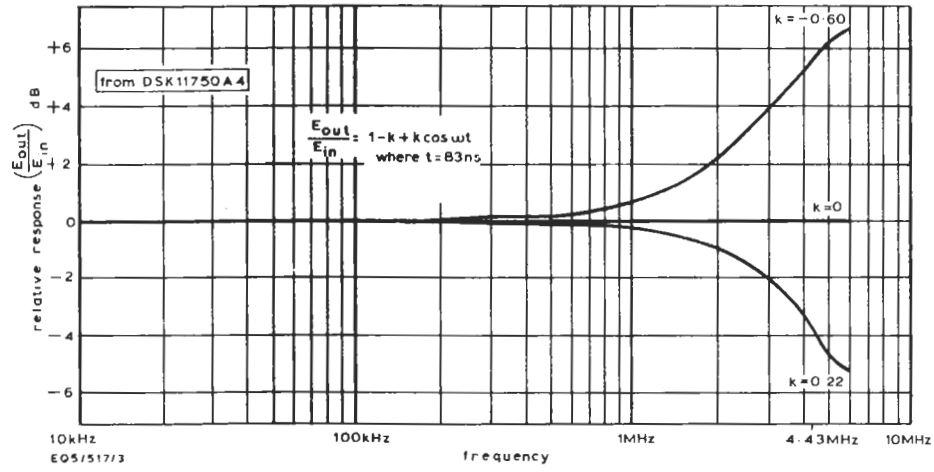

Fig. 4 Theoretical Response of the EQ5/517

References to Typical Associated Equipment

1. Automatic Chrominance Equaliser EQ12L/501.
2. Stabilising Amplifier AM18L/519.
3. Colour Signal Stabiliser Equipment EP1M/513.

MJR/KHG 6/69
LPB 2/72