SOUND IN SYNCS CODER CD2M/505

Introduction

The CD2M/505 accepts a 625-line video signal and an audio signal; it produces a video-plus-sound signal in which pulse-coded sound information is carried in the line-sync interval of the video waveform.

The audio signal is applied to a compressor which, together with an expander in the associated decoder[1], forms a compandor system which improves the audio signal-to-noise ratio. The action of the compandor is controlled by a line-frequency pilot-tone signal which is added to the audio signal prior to compression. After compression the audio signal is sampled at twice-line frequency and the samples are converted into ten-bit pulse-code-modulation signals. Alternate p.c.m. samples are stored for half a line and the samples are then inserted, two at a time, into the following line-sync pulse by means of a bit-interleaving process. A marker pulse is added to each two-sample pulse group before the insertion takes place.

A simplified block diagram of the coder is given in Fig. 1. Power supplies are provided by a mains-powered PS2L/94 Power Supplier.

The coder consists of the following plug-in units mounted on a PN3/23 chassis:

Sound-in-syncs Video Processing Amplifier	AM1/578
Sound-in-syncs Audio Limiter	AM6/9
Band-stop and Pre-emphasis Filter	FL1/32
Sound-in-syncs Audio Input Unit	FL1/36
Sound-in-syncs Pilot Tone Generator	GE1/546
Sound-in-syncs Sync Separator Unit	UN16/514
Sound-in-syncs Timing Oscillator	UN23/521
Sound-in-syncs Timing Gates	UN23/522
Sound-in-syncs Shift Register	UN23/527
Sound-in-syncs Counter and Clock Unit	UN23/528
Sound-in-syncs Sample and Hold Unit	UN23/530

together with an FL4/566 Filter which is wired in series with the output.

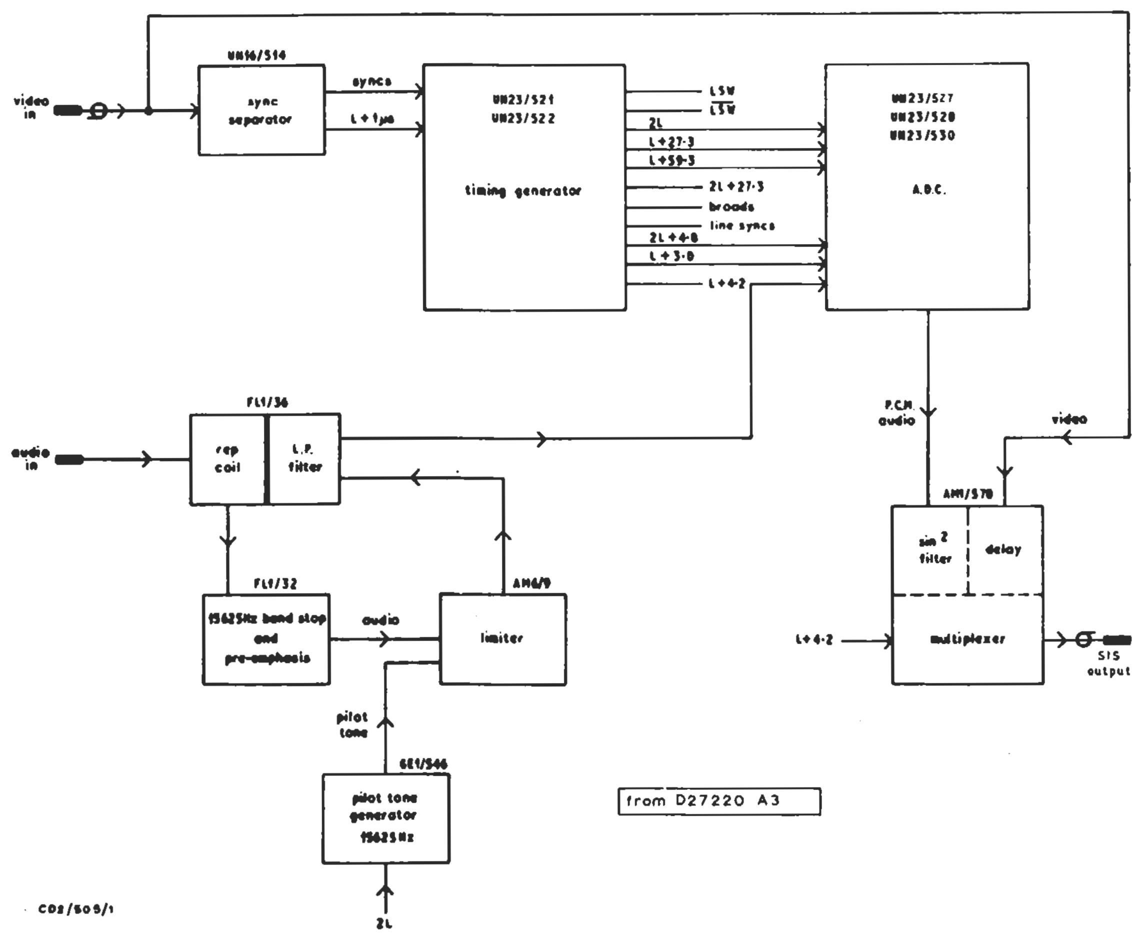


Fig. 1 Block Diagram of the CD2/505 Coder

General Specification

Audio

Input Amplitude	zero level peaking to 8 dBm
Input Impedance	600 ohms, balanced
Sampling Rate	twice line frequency (31·25 kHz nominal)
Code	10-digit binary
Pre-emphasis	modified CCITT characteristic
Pilot Tone Frequency	line frequency (17·625 kHz)
Pilot Tone Level	−20 dB relative to peak audio

Video

Input Amplitude	1V p-p nominal
Input Impedance	75 ohms ±3%
k-rating for 2T pulse	less than 0·5%
Differential Phase Distortion	less than 0·15°
Differential Gain Distortion	less than 0·5%
Line-time Tolerance	±1·5 μs for changes occurring over more than 50 lines, −1 μs for line-by-line variations

Reserve Line Drive

Input Amplitude	2V p-p negative-going
Input Impedance	10 kilohms

Combined Output Signal	1V p-p nominal

Logic

The logic circuits of the coder use T.T.L. and M.E.C.L. integrated circuits. T.T.L. and M.E.C.L. logic levels are shown in Fig. 2.

General Description

The following description deals briefly with the coder as a whole. For more detailed information on individual units see the appropriate Instructions.

Audio Signal Path

The audio input signal is routed via a repeater coil and an attenuator pad in the FL1/36 unit to the FL1/32 unit. This unit contains a combined band-stop and pre-emphasis network which removes audio components in a band of frequencies centred on 15·625 kHz, and then pre-emphasises the signal in a network which has a response similar to that of the standard CCITT characteristic. The pre-emphasised audio signal is passed to an AM6/9 limiter; this is a fast-acting device and its variable-gain characteristic is such that it maintains a constant output level if the audio input exceeds a pre-determined amplitude. The pre-emphasis applied earlier to the signal ensures that limiting is normally initiated by the high-frequency components of the signal.

Pilot tone is added to the audio signal at the input to the AM6/9 and is modulated by the compression

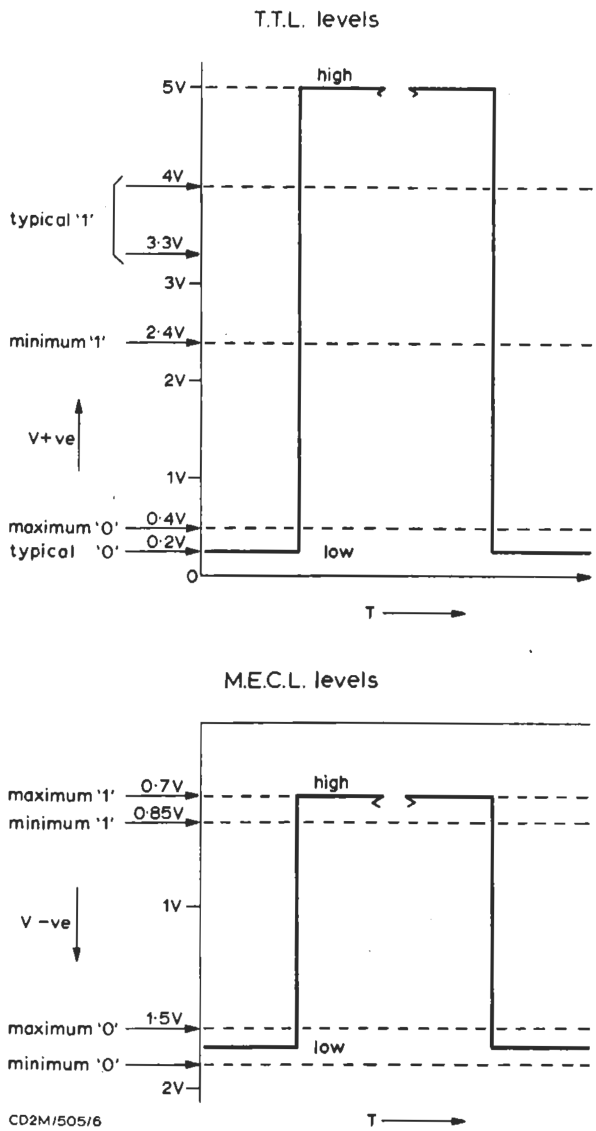


Fig. 2 S.I.S. Logic Levels

of the signal; it thus carries compression information to the expander in the associated decoder. From the AM6/9 unit the signal is routed back to the FL1/36 where it is passed through a low-pass filter to remove components above 15·625 kHz.

Timing-pulse Generator

The process of analogue-to-digital conversion and the subsequent insertion of the coded sound signal into the video signal, require a number of pulse waveforms which must be synchronised with the video signal and accurately timed. These waveforms are derived from the UN23/521 Timing Oscillator which is driven by separated sync pulses.

The oscillator is started by the leading edge of separated syncs and provides an output, at a frequency of approximately 10 MHz, which is used to clock a counter. When the count reaches 630 (i.e. 63 μs after the start) both counter and oscillator are stopped until the arrival of the next sync pulse; during this period the counter is reset to zero. The action of stopping the counter starts a ramp generator, and the resultant ramp waveform provides an oscillator-correction voltage which ensures that the period between the counter stopping and the arrival of the next sync pulse is maintained at 1 μs. The various outputs of the counter are gated in the UN23/522 unit to provide the pulse waveforms required by the other units of the coder.

Analogue to Digital Conversion

Analogue-to-digital conversion of the audio signal is carried out by means of a ramp generator and a counter, and the subsequent interleaving of alternate coded samples is carried out in a shift register (see Instruction GP.1). A simplified block diagram of the analogue-to-digital converter is shown in Fig. 3 and a more detailed diagram in Fig. 4. The units involved are the UN23/530, UN23/528 and UN23/527.

The compressed audio signal is sampled, the sample is stored on a capacitor and applied to a comparator which also accepts the output of the ramp generator. When the timing pulse generator (described earlier) is triggered by the leading edge of a separated sync pulse, it generates a pulse which starts both the counter and the ramp. The count continues until the ramp amplitude equals that of the stored sample, whereupon the comparator produces a pulse which stops both ramp generator and counter. The number held in the counter is then transferred to alternate stages of the shift register and the sequence repeated for the next sample so that, at the end of two sample periods, the shift register contains two coded samples. The digits of the samples are interleaved by storing similarly-numbered digits from each sample in adjacent stages of the register. The register is fed with line-frequency shift pulses and thus one read-out is provided for every two coded-sample inputs. The circuit of the register is such that one sample of each pair is complemented during the reading out process, additionally the register adds a marker pulse to each two-sample pulse group.

Digit/Video Multiplexing

The video and coded sound signals are both applied to the AM1/578 processing amplifier where the video signal is clamped at the bottom of syncs and the digits of the coded sound signal are given a sine-squared shape. The sound pulse groups are then inserted into the sync pulse periods of the video waveform by means of a gating circuit. If the video signal fails, it is replaced by a feed of standby sync pulses from the UN16/514 unit.

Maintenance and Alignment

The waveforms present at the test points on the front panels of the plug-in units, for normal operating conditions, are shown in Fig. 5. Adjustments which affect the coder as a whole are detailed below. Maintenance and alignment information for individual units is given in the relevant Instructions.

Operational Adjustments

To maintain optimum performance, the following adjustments should be made if some plug-in units are changed; see also Table 1. (If these adjustments are not carried out the coder will continue to operate, but with impaired performance.)

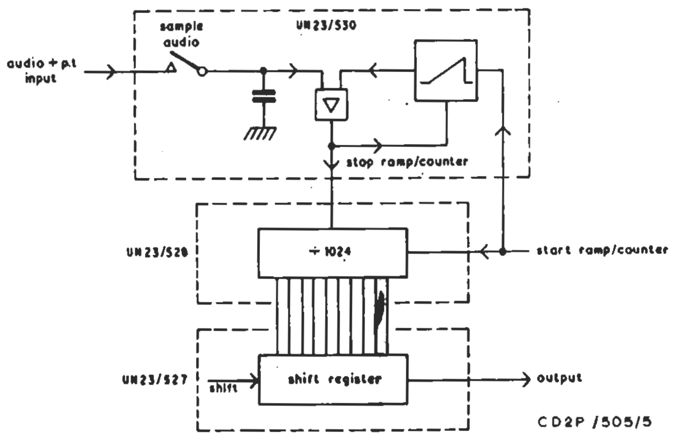


Fig. 3 Simplified Block Diagram of the Analogue-to-Digital Converter

TABLE 1

Unit Changed	*Adjustment Required*
AM1/578	1
AM6/9	2,3
FL1/36	3
GE1/546	3
UN23/530	4

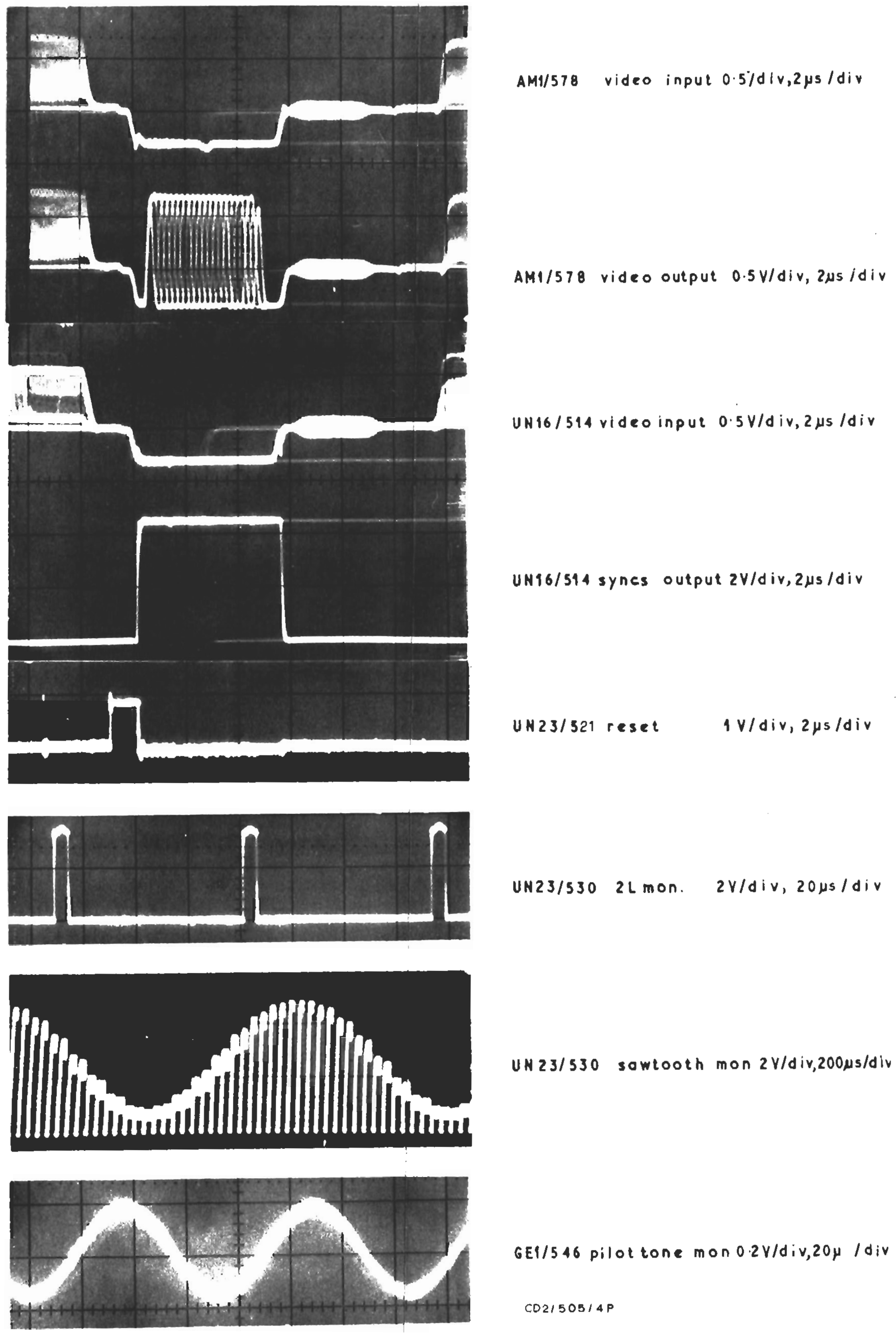


Fig. 5 Waveforms

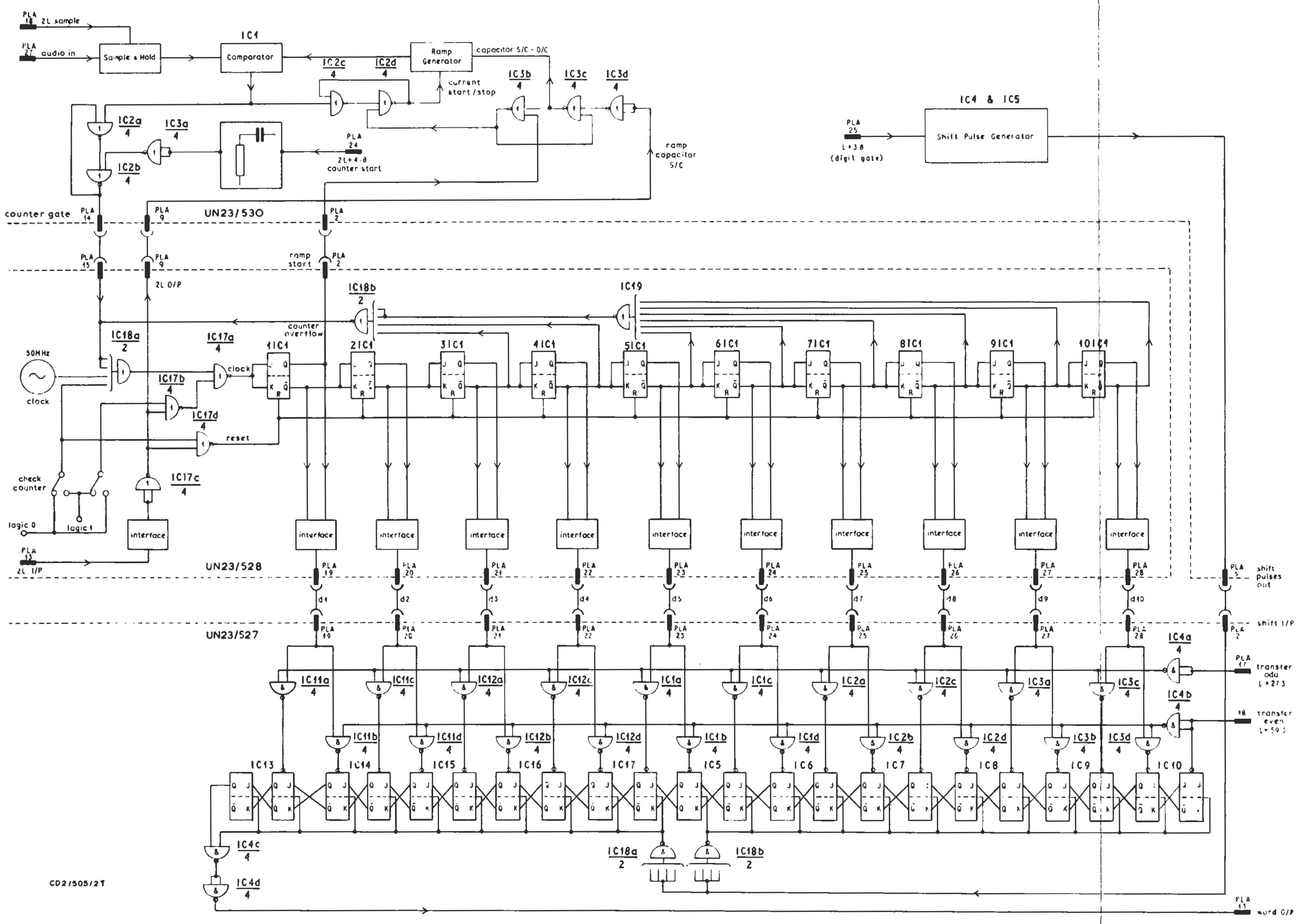


Fig. 4 Detail Block and Logic Diagram of the Analogue-to-Digital Converter

1. Pulse-to-sync-sit Timing Adjustment (AM1/578)

(i) Monitor the video output of the coder with an oscilloscope and remove the UN23/530 unit. Adjust R26 so that the bottom of the re-inserted sync pulses is at the same level as the original sync pulses. Replace the UN23/530 unit.

(ii) Measure the time between the half-amplitude point of the leading edge of syncs and the half-amplitude point of the leading edge of the first sound pulse. This should be 450 nano-seconds. If it is not, adjust the taps on the AM1/578 delay line until the correct figure is obtained.

2. Audio Level Adjustments (AM6/9)

(i) Place the AM6/9 unit on an extender board and monitor test point TP1 with an oscilloscope probe. Apply a 1-kHz signal at a level of 0 dB w.r.t. 1 mW (±0·1 dB) to the audio input of the coder. Adjust R56 until the signal at TR1 is about 100 milli-volts peak-to-peak, see Fig. 6(a).

(ii) Remove the UN23/530 unit from the coder assembly. Connect the *Audio to ADC Mon.* test socket on the front panel of the FL1/36 filter to the 600-ohm input of an accurately-calibrated ATM1 Audio Test Meter, or an equivalent device. Adjust R33 on the AM6/9 unit to obtain a meter reading of +5·5 dB w.r.t. 1 mW (±0·1 dB). Replace the UN23/530 unit.

3. Pilot Tone Level and Phase (GE1/546)

(i) Connect an audio test meter as in adjustment 2(ii). Remove the UN23/530 unit and remove also the audio input to the coder. Place the GE1/546 unit on an extender board and adjust R17 to obtain a meter reading of −14·5 dB w.r.t. 1 mW (±0·1 dB). Replace the UN23/530 unit and the audio input to the coder.

(ii) Connect the *Audio to ADC Mon.* socket on the front panel of the FL1/36 to one input of a dual-trace oscilloscope, taking care to observe the correct polarity. Connect the *2L Mon.* test socket which is located on the front panel of the UN23/530 unit to the other input of the oscilloscope. Trigger the oscilloscope from separated syncs (available at a test socket on the UN16/514 unit) and adjust R4 on the GE1/546 unit so that the pulse obtained from the UN23/530 unit is coincident with the positive and negative peaks of the sine wave obtained from the FL1/36 filter. It may be necessary to change link LK1 on the GE1/546 unit from C2 to C3 to achieve this.

4. Adjustment of Sample-and-Hold Ramp (UN23/530)

(i) Remove the FL1/36 filter from the coder assembly. Use an extender board and a 15-way Painton socket to feed 400-Hz tone at +7 dB w.r.t. 1 mW into pins 3* and 4 of the coder connector into which the FL1/36 normally plugs. Set the oscilloscope timebase to 0·5 ms/cm and monitor the *Mon. Sawtooth* test socket (SK B) on the UN23/530 unit. Adjust R39 on the UN23/530 unit so that the modulation of the sawtooth train is just 100%; i.e. until the sawtooth and audio components of the oscilloscope display have the same amplitude, as shown in Fig. 6(b). *Pin 3 is earthy.

(ii) With the FL1/36 unit still removed, monitor the video output of the coder and adjust the oscilloscope trace to display the sound-in-syncs content of a single sync pulse. Remove the audio input to the coder and check that the sound-in-syncs digits become stationary. Check that the digits, reading from the left-hand side of the display, are:

either 1****0101010101010110
or 1****1010101010101001
(* may be either 1 or 0)

If not, adjust R34 on the UN23/530 unit to achieve this, see Figs. 6(c) and 6(d). An unacceptable digit pattern is shown in Fig. 6(e).

5. Final Checks

(i) Apply a composite pulse-and-bar signal to the *Video* input of the coder and apply a feed of line-drive pulses to the *Standby Syncs* input.

(ii) Monitor the coder output. Check that the digit amplitude is 1V p-p and that any digit overshoot is less than 50 mV p-p. If not, check the AM1/578 unit.

(iii) Check that the differential-gain and differential-phase distortion figures are within the limits given in the General Specification.

(iv) Remove the pulse-and-bar signal. Check that emergency sync pulses (derived from the line drive input) are present at the coder output and that these pulses carry sound-in-syncs digits.

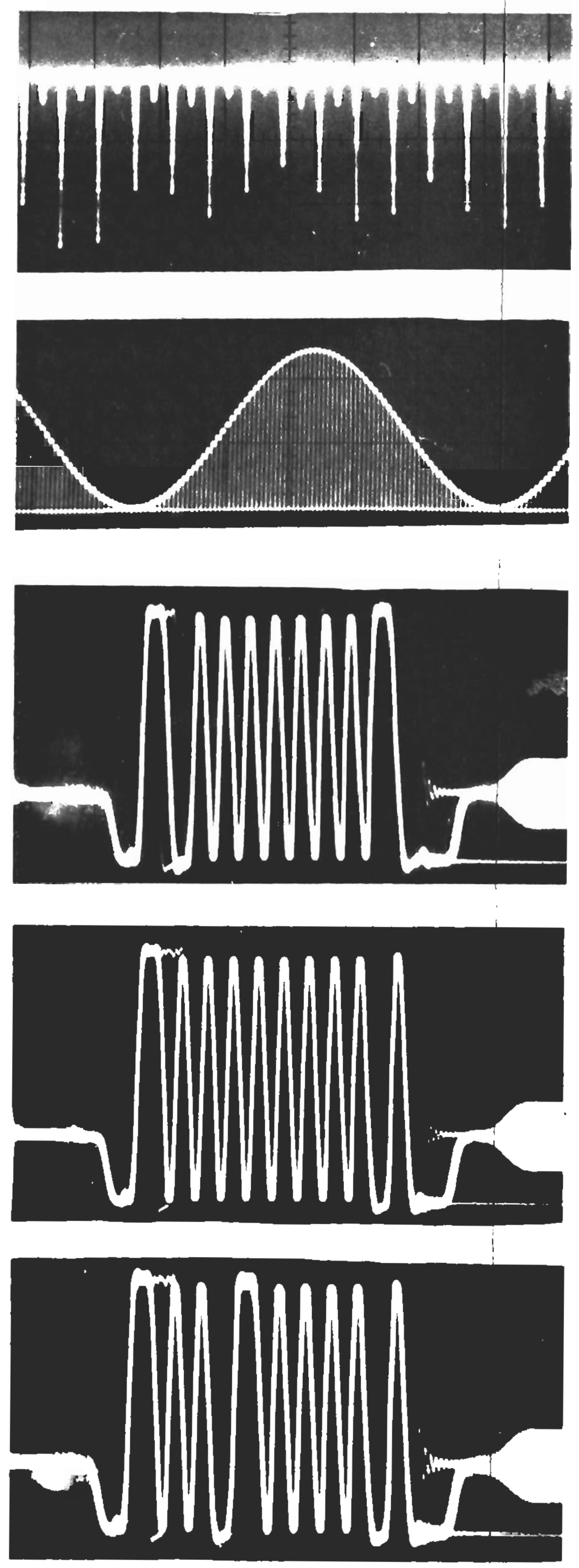
(v) Replace the pulse-and-bar signal. Check that black-level disturbances are less than 15 mV p-p.

Unit Interconnections

Interconnections between the component units of the coder (other than power supply feeds) are given in Fig. 7 on page 9.

References

1. Sound-in-syncs Decoder CD3M/504



(a) AM6/9 limiting level correct (vertical scale 50m/div.)

(b) UN23/530, R39 adjustment correct

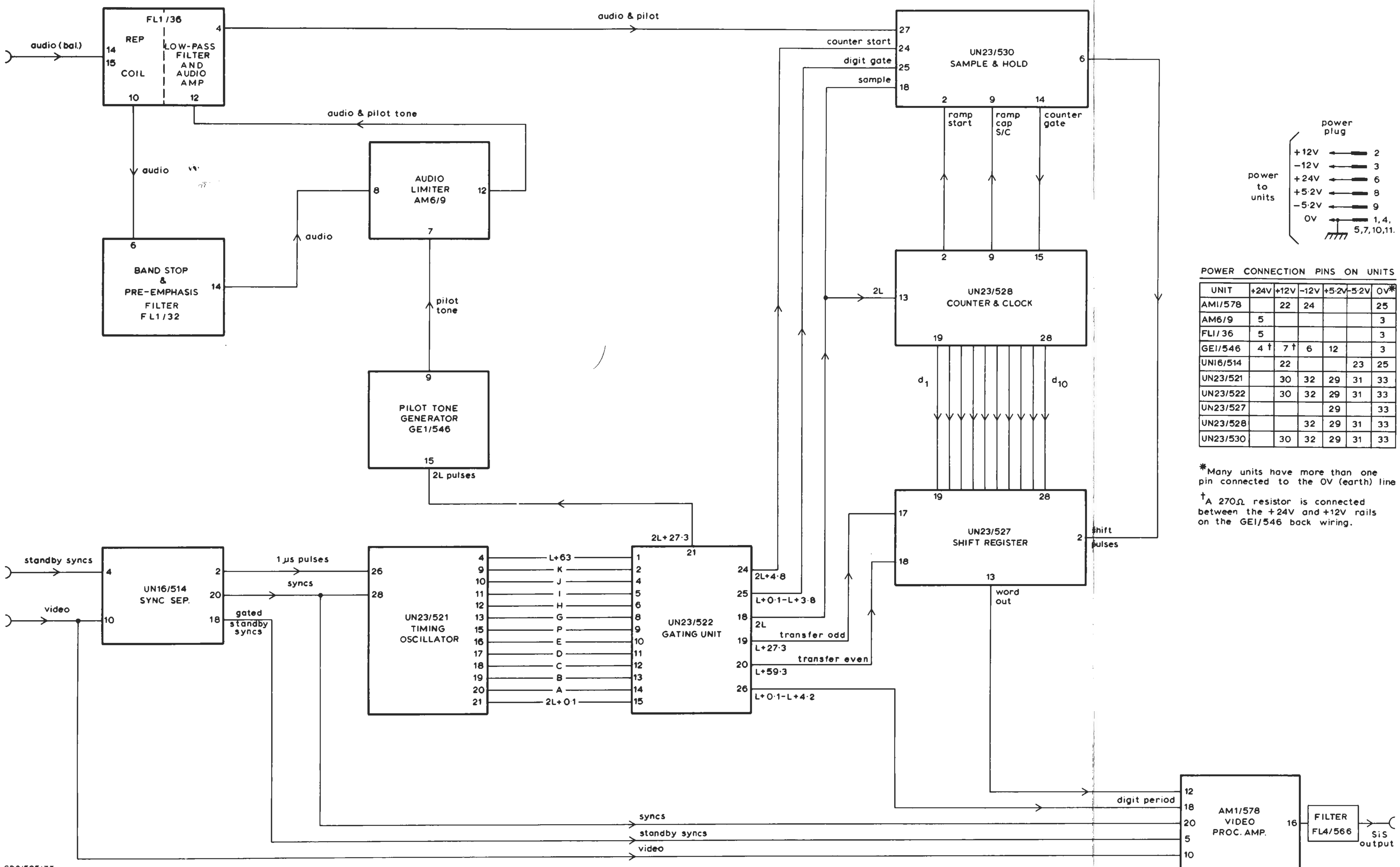
(c) Coder output, acceptable digit pattern

(d) Coder output, acceptable digit pattern

(e) Coder output, incorrect digit pattern

CD2P/505/3

Fig. 6 Waveforms



POWER CONNECTION PINS ON UNITS

UNIT	+24V	+12V	−12V	+5·2V	−5·2V	0V*
AMI/578		22	24			25
AM6/9	5					3
FLI/36	5					3
GEI/546	4 †	7 †	6	12		3
UNI6/514		22			23	25
UN23/521		30	32	29	31	33
UN23/522		30	32	29	31	33
UN23/527				29		33
UN23/528			32	29	31	33
UN23/530		30	32	29	31	33

*Many units have more than one pin connected to the 0V (earth) line

†A 270Ω resistor is connected between the +24V and +12V rails on the GEI/546 back wiring.

Fig 7. CD2/505: Unit Interconnection Diagram