INSERTION TEST SIGNAL GATING UNIT UN9/568

Introduction

The UN9/568 accepts a composite video signal complete with Insertion Test Signal (I.T.S.) and two line-trigger signals. The outputs are components of the Insertion Test Signal.

The unit is built on a printed wiring board which is mounted on a CH1/43A chassis.

General Specification

Inputs	Video signal, one volt p-p.
	Line trigger signal coincident with the start of lines 19 and 332; five volts p-p.
	Line trigger signal coincident with the start of lines 20 and 333; five volts p-p.
Outputs	I.T.S. luminance bar; 1·4 volts p-p into 75 ohms.
	I.T.S. 2T pulse; 1·4 volts p-p into 75 ohms.
	I.T.S. chrominance pulse; 1·4 volts p-p into 75 ohms.
	I.T.S. linearity staircase; 1·4 volts p-p into 75 ohms.
	Sync pulse on lines 20 and 333; 0·9 volts p-p into 225 ohms.
	I.T.S. chrominance bar; 1·4 volts p-p.
Logic Levels	
Logic 0: input	1·1 volts max.
output	0·4 volt max.
Logic 1: input	1·9 volts min.
output	2·6 volts min.
Power Requirements	+6 volts at 55 mA
	+12 volts at 115 mA
	−12 volts at 115 mA

Circuit Description (Fig. 1)

Fig. 1 is a circuit diagram of the UN9/568.

The video input is applied through pin PLA2 to two common-emitter amplifier stages TR21 and TR22. Feedback is applied from the collector of TR22 to the emitter of TR21.

Clamp pulses, 2 μs wide, are applied through pin PLA4 to emitter-follower TR23. The pulse from TR23 switches f.e.t. TR24 so that the signal at the collector of TR22 is clamped to earth potential.

Negative-going 10-μs line-trigger pulses are applied at pins PLA16 and 18 and each signal is inverted in a separate NAND-element of circuit IC11.

The circuit so far described in common to all stages of the unit. The remainder of the circuit comprises six sections which are identical except for the timing components of monostable circuits which produce gating pulses. Each section is designed to provide a particular part of the I.T.S. waveform at its output.

The following description, specifically of Circuit 1, is typical.

The inverted line trigger signal corresponding to line 19 triggers monostable circuit 1IC1 which produces a negative-going gating pulse 14 μs wide. This pulse is applied to the base of transistor 1TR5; transistors 1TR5 and 1TR6 have a phase-splitting action. When the gating pulse is present a positive-going pulse from the collector of 1TR5 is applied to the gate of 1TR1 and a negative-going pulse from the collector of 1TR6 to the gate of 1TR2. Thus 1TR1 is saturated, 1TR2 is cut off and the required part of the video signal is passed through two emitter-follower stages, 1TR3 and 1TR4, to the output at pin PLA6.

A positive-going output from monostable circuit 1IC1 is passed to the monostable circuit in Circuit 2, 1IC1. A similar switching action results in the 2T-pulse component of the I.T.S. waveform being made available at pin PLA7.

Test Schedule

The unit is designed to be tested as part of the MN2M/513. Detailed alignment instructions are given in Designs Department Specification 11.84(69).

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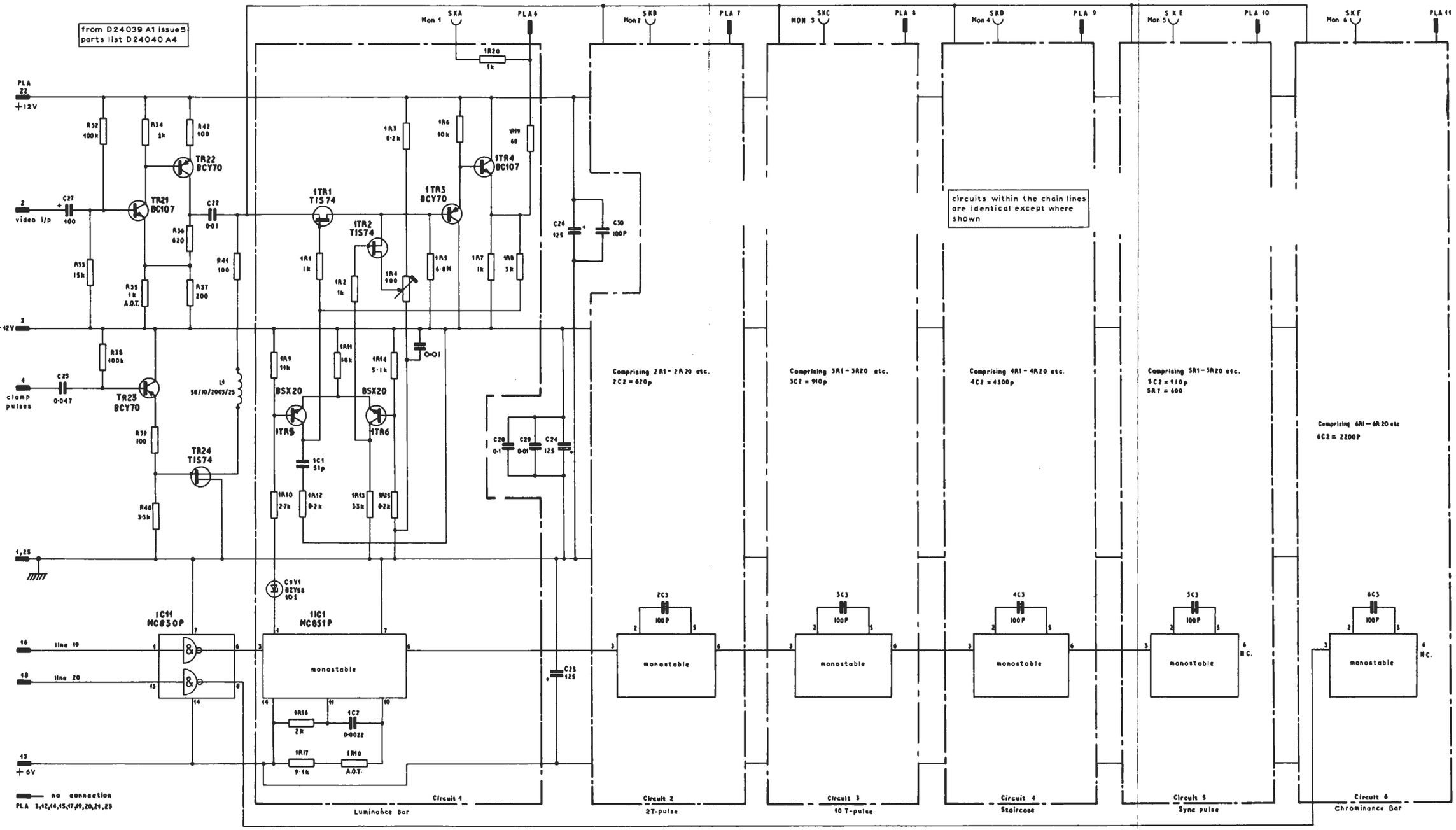

Transistor terminations view on leads

TIS74

BCY70 BC107 BSX20 collector connected to envelope

Integrated cct. view on top.

MC830P MC851P

Notes
1. Pins 6 marked NC on 1IC1 & 6IC1 are not connected.

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Fig.1. Circuit of UN9/568