PROCESSING AMPLIFIERS AM1/14A-F AND AM1M/16A-C

General

The amplifiers in the AM1/14 series are constructed on printed circuit cards and when mounted in pairs on a chassis CH1/26A they form the AM1M/16 series as follows.

Each subunit AM1/14 incorporates a programme amplifier which drives a level switch. Index pegs are fitted to the chassis-mounted units AM1M/16 in the positions indicated below.

AM1M/16A: 3 and 33 AM1M/16B: 3 and 34 AM1M/16C: 3 and 35

These amplifiers are used in sound automatic monitors MN2M/2 to MN2M/6, described in a separate Instruction.

Functions

Analogue-to-Digital Conversion

A main function of the six subunits AM1/14A-F required in a complete monitor system is to transform the normal (or 'analogue') programme signals at the sending and receiving points into digital form for convenience of comparison. If the switching stage of an AM1/14 is not operated, the output is 0 volts, representing the digit l. When the stage is operated its transistor conducts; the resulting output of -24 volts represents the digit l.

An increasing input level causes the switching stage to operate at the following point:

AM1/14A: -38 dB	AM1/14D: -12 dB
AM1/14B: -35 dB	AM1/14E: $-9 dB$
AM1/14C: -32 dB	AM1/14F: $-6 dB$

The amplifiers AM1/14B and AM1/14E are used at the sending (or reference-programme) point to detect in which of three zones the signal lies:

- (a) below -35 dB,
- (b) Between -35 and -9 dB,
- (c) above -9 dB.

The receiving (or compared-programme) amplifiers AM1/14A, C, D and F operate at levels 3 dB on either side of the transition levels, that is, at -38, -32, -12 and -6 dB, thus providing guard-bands to prevent operation of the monitor alarm for minor discrepancies in the levels being compared.

Signal Processing

The other main function of the units is to process the signal so that the monitoring-system fault sensitivity approaches that required to simulate subjective assessment. To this end, the frequencyresponse characteristic is distorted for three reasons:

- To give greater weight to the medium-frequency components, whose amplitudes are generally much less than those of components of lower frequency.
- 2. To modify the noise spectrum to allow for the unequal response of the ear.
- To reduce sensitivity to frequencies at the extremes of the audio range to accommodate variations in line characteristic.

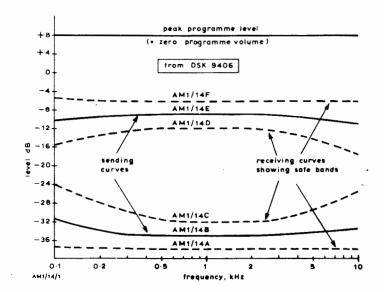


Fig. 1. Frequency Response and Operating Levels of AM1/14A-F for Rising Programme Signal

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In the language of switching circuit analysis, it may be said that the choice of the voltages 0 and -24 to represent the digits or 'logic values' I and θ follows a positive logic convention, because the higher digit denotes the more positive voltage.

Each AM1/14 has a response characteristic dependent on the level at which it operates. The curves for a rising input level are given in Fig. 1. These curves determine the sensitivity of the monitor at different frequencies and programme levels.

AM1/14, 16

The concept of 'programme levels' is introduced here for convenience, because it makes the numerical scale of programme and tone measurements the same. A zero programme level signal produces occasional peak readings of 4 on a P.P.M. which has been lined up to read 4 on steady zero level tone. Zero programme LEVEL is thus the same as a programme VOLUME of -8 dB. See Note*.

Smoothing of Group-delay Distortion Effects

The amplifiers also incorporate an integrating circuit to smooth out waveform discrepancies due to differences in group delay in the link. The six types differ in the discharge time constant of this circuit so that those operating at higher level drop out before those operating at lower level, as the output level falls.

Circuit Description (Fig. 3)

TR1 and TR2 form an input amplifier with negative feedback. The input impedance is high and is largely determined by R1 and R2 in parallel. The output from this stage incorporates the high-level limiting circuit D1 to D4 which commences to operate at an input level above —3 dB. TR3 and TR4 form a similar amplifying pair with feedback, followed by the frequency correcting networks which produce the required amplifier characteristics. The values for these networks in the six amplifiers are given in Fig. 2. C21 and C22 are required for stability at high input levels.

Transistors TR5 to TR9 form an amplifier section over which the output level control feedback operates. TR5 is the input amplifier of the section and this is followed by a Darlington pair, TR6 and TR7, driving a complementary push-pull output stage TR8 and TR9. Voltage negative feedback is applied by the network consisting of R18, R19, R21, D5, D6, C13 and RV1 between the output and the emitter of TR5. The feedback is varied in two ways. When the output voltage across R30 (which when rectified operates the level switch) rises to such a value that the zener diodes D5 and D6 conduct, the series arm R18, R21 and R22 is shunted by the reduced impedance in the arm R19, D5 and D6 and the feedback is

increased. The diodes commence to conduct on each half-cycle when the voltage across them exceeds the zener voltage (3·3 volts) of one of them plus the forward voltage drop (0·7 volt) of the other. RV1 operates as an overall gain control fixing the sensitivity level of the amplifier, and the diode-controlled feedback supplies a limiting action. Thus the voltage applied to the rectifier (D9) at levels above the critical level is controlled by the law of this limiter rather than by an overload condition. R21 and R22 have been included as an optional adjustment of the operating point.

A common input signal is applied to the bases of the push-pull pair TR8 and TR9, and the correct relative d.c. conditions for these transistors are obtained from the forward voltage drops across D7 and D8. R28 may be used as a monitoring component. The output voltage from the amplifier section is applied to the cascade voltage doubler rectifier C17, C18, D9 and D10. R31 controls the charging time constant and this varies with the amplifier type, increasing in value with increase in switching level. R32 and R33 control the discharge time constant, and as mentioned above, this value is reduced as the switching level increases. These two time constants provide the integrating characteristic which has been found suitable to counter most of the effects of phase distortion over long lines.

TR12 and TR13 form a trigger circuit and output switch. When C18 is in the discharged condition there is a small base current flowing via R33 in TR10, causing conduction also through TR11. This results in a voltage of about -1 volt at the base of TR12. The emitter of TR12 is held at -3.3 volts by the zener diode D11 and therefore TR12 is cut off and also TR13. The output terminal is thus at 0 volts. This output represents the digit I.

When the incoming signal causes the voltage across C18 to rise to about -3.5 volts, the emitter bias of TR12 is exceeded and the transistor conducts. TR13 also conducts, and positive feedback via R37 increases the conduction currents in both transistors. The output terminal is now at almost -24 volts. This output represents the digit θ .

Transistors TR10 and TR12 form a compensating circuit for temperature variations, thus providing d.c. stabilisation.

Adjustment and Testing

Power Supply

Voltage, 24 volts d.c. Current per AM1M/16, 125 ±25 mA.

Procedure

 Connect the positive of the power supplier to pin PLA-14 of the AM1M/16 under test and the negative to pin PLA-4.

In BBC measurements of transmission quantities, zero programme volume and zero level tone have traditionally been taken as reference points. If, say, a transmitter or a recording system is modulated to 100 per cent by zero programme volume, the modulation depth is 40 per cent during line-up on zero level tone. The advantage of using this particular modulation ratio is that statistical analysis of programmes of various types suggests that the signal power of the programme and line-up tone is likely to be very roughly the same.

In the sound automatic monitors with which AM1/14 amplifiers are designed to be used, it is the processed peak voltages of two programme signals that are compared, and alignment of the comparator system must be carried out with steady tone of the same peak voltages as the programme signals simulated.

^{*} Note on 'Volume' and 'Level'

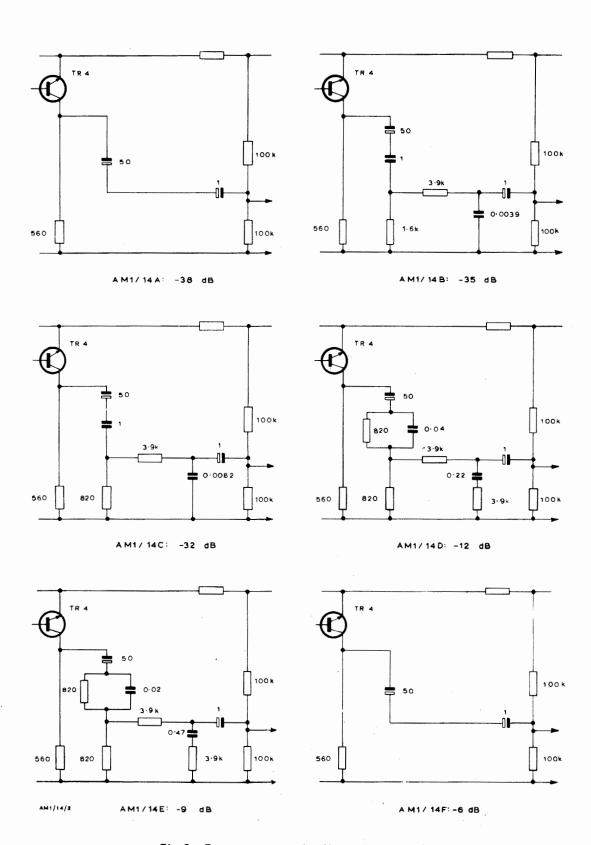


Fig. 2. Frequency-correction Networks of AM1/14A-F

- Using an Avometer Model 8 on its 25-volt range, connect meter positive to pin PLA-14 of the AM1M/16, and meter negative to
 - (a) pin PLA-13 when testing subunit AM1/14A, B or C, or
 - (b) pin PLA-12 when testing subunit AM1/14D, E or F.

When connecting the meter to PLA-13, avoid a short-circuit to PLA-14, as this can damage TR13 in the AM1/14A, B or C.

- Apply 1-kHz tone from a 600-ohm source terminated with 600 ohms to pins PLA-14 and PLA-11.
- 4. Set the tone level to the value appropriate to the type of AM1/14 as indicated in Table 1.

TABLE 1

Unit		Input Level (dB)		
Unit Subunit	Subunii	1 kHz	100 Hz	10 kHz
AM1M/16A	AM1/14A AM1/14D	-38 -12	-37·5±1 -15·5±1	-37·0±1 -15·0±1
AM1M/16B	AM1/14B AM1/14E	-35 -9	-31·5±1 -10·5±1	-32·0±1 -10·0±1
AM1M/16C	AM1/14C AM1/14F	-32 -6	-24·5±1 -5·5±1	$ \begin{array}{r} -24.5 \pm 1 \\ -5.0 \pm 1 \end{array} $

- 5. Adjust RV1 on the AM1/14 under test so that its output switching circuit just operates to change the Avometer reading from nearly 0 volts to almost 24 volts. An AM1/14A, B or C, with its RV1, is on the left side of an AM1M/16 amplifier, and an AM1/14D, E or F is on the right.
- Check the setting by reducing the level of the tone by 6 dB and slowly increasing it until the switch again operates. The operate point should be as shown in Table 1, within ±0.5 dB.
- 7. Reduce the level of the tone from above the operate point. The switch should release at a level 3.5 ±0.5 dB below the operate level.
- 8. Check the input levels required to operate the switch at 100 Hz and 10 kHz for an increasing level of tone. These levels should be within the limits shown in Table 1 (if the levels for 1-kHz operation are exactly correct).
- Check the voltage between pins 5 and 8 on the printed board, with an Avometer Model 8 on its 25-volt d.c. range, as follows:
 - (a) When the input to PLA-11 and PLA-14 is adjusted to zero level at 1 kHz, the

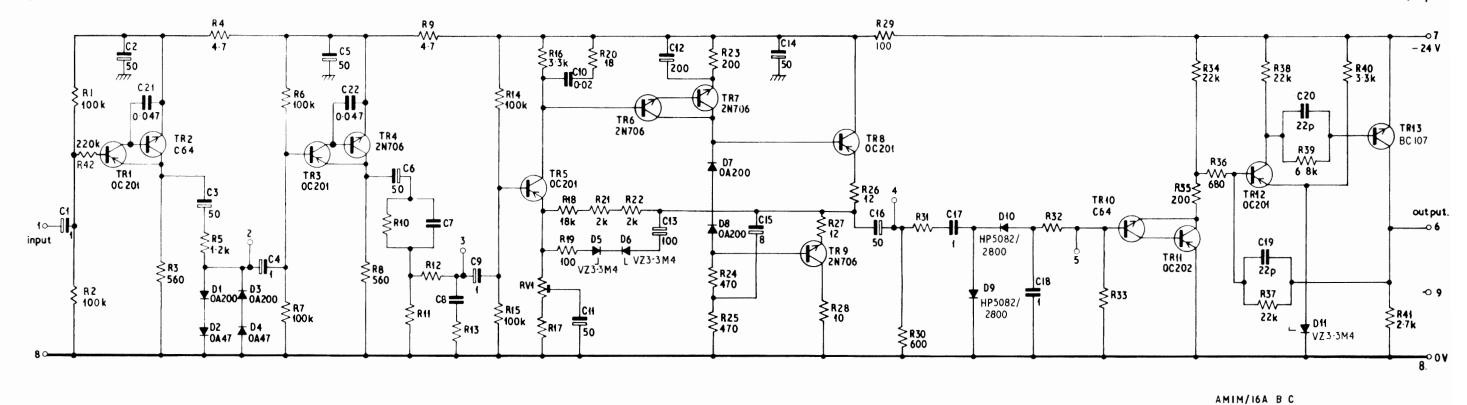
TABLE 2

Amplifier Type	Board Pin 5 Volts	Switching Delay Limits (ms)	
AM1/14A	8·6 <u>+</u> 0·4	650 to 890	
AM1/14B	8·2 <u>+</u> 0·4	470 to 650	
AM1/14C	7·8 ±0·4	350 to 470	
AM1/14D	4·5 <u>+</u> 0·3	115 to 155	
AM1/14E	4·3 ±0·3	85 to 115	
AM1/14F	4·3 ±0·3	65 to 85	

voltage should be as in Table 2.

- (b) When the input is reduced until the switch releases, the voltage should be -2.3 ± 0.3 volts
- (c) When the input is raised until the switch operates, the voltage should be -3.2 ± 0.3 volts
- 10. Check the operation of the limiting circuits by measuring the voltage across R30, i.e. between pins 4 and 8 on the printed board, using an oscilloscope. Limiting (flattening of the waveform) should occur at about 4 volts peak-to-peak. Limiting, as observed between pins 2 and 8 on the printed board, should also occur with an input to the amplifier above -3 dB.
- Feed a 1-kHz tone at zero level to the amplifier unit input pins, PLA-11 and PLA-14. Apply the switched d.c. output from PLA-12 to the vertical deflection terminals of an oscilloscope. Connect a relay with two pairs of make contacts so that one pair of contacts short-circuits the applied tone and the other pair switches a trigger voltage (say 24 volts d.c. from the supply employed to operate the relay) to the oscilloscope. Operate the relay and check the delay time between the triggering of the oscilloscope trace and the switching action of the amplifier output from -24 to 0 volts. This should be as shown in Table 2. Check the second amplifier output at PLA-13 similarly. An amplifier may give satisfactory results if it has drifted somewhat outside these limits (particularly if the other processing amplifiers in a system have drifted similarly) but this is a developing fault condition. A low time may be due to leakage in D9 or D10.

Text continued on page 7



Transistor Electrodes Identification
View on leads





2N 706 OC 201 C 64 OC 202

from D17300 A 2

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R 10 LINK 820 820 LINK R 11 1.6k 820 820 820 R12 LINK 3-9k 3-9k 3-9k 3-9k LINK R13 LINK LINK 3·9k 3-9k R17 10k 10k 9·1k 7-5k 4·7k LINK RVI 270 330 470 2.2k 4.7k 10k C 7 0.04 0.02 C8 0-0039 0-0082 0-22 0.47 R31 750 820 910 1k 1-lk 1-2k R32 30k 24k 20k 16k 13k 10k R33 300k 240k 200k 160k 100 k 130 k

B C D -35dB -32dB -12dB

-9dB

-6dB

-38dB

01 02 AMI/I4D E F AMI/I4A B C ¹ ₀_ 03 20 - 24 V 3 o 30 4 o 40 07 08 09 6 0-010 -o II -o 12 OUT DEF OUT A B C O 15 |

AM1/14/3T

TABLE 3

Measuring Point	Voltage
TR1 Emitter	8.5
TR3 Emitter	-9.0
TR5 Emitter	-8.0
TR9 Collector	about -0.1
Junction R26/R27	-7.5
Junction R26/R27	

Test Voltages

Typical voltages, relative to the 0-volt line, are given in Table 3 to assist fault finding.

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