VIDEO AMPLIFIER AM18/506

Introduction

The AM18/506 provides the main signal path through the AM18/504 Stabilising Amplifier. It consists of two amplifiers normally joined by an external delay line and it receives as input a composite video signal, monochrome or colour.

The first amplifier provides outputs to the delay line, to a sampling pulse generator and to an error signal sampling and amplifying chain. It receives back from the error signal chain an inverted copy of any error signal and feeds this to the delay line in parallel with the original signal.

The second amplifier provides facilities for stabilising sync pulse amplitude and feeds the main output.

The unit is constructed on a CH1/12A chassis with index pegs 1 and 18.

General Specification

Signal Input	
(composite video)	0·7 V p-p video ±3 dB
	0·3 V p-p sync ±6 dB
Signal Output	
(composite video)	1 V p-p
Input Impedance	75 ohms nominal
Output Impedance	75 ohms nominal
Power Required	160 mA at +12 V 140 mA at −4 V
Weight	1 lb

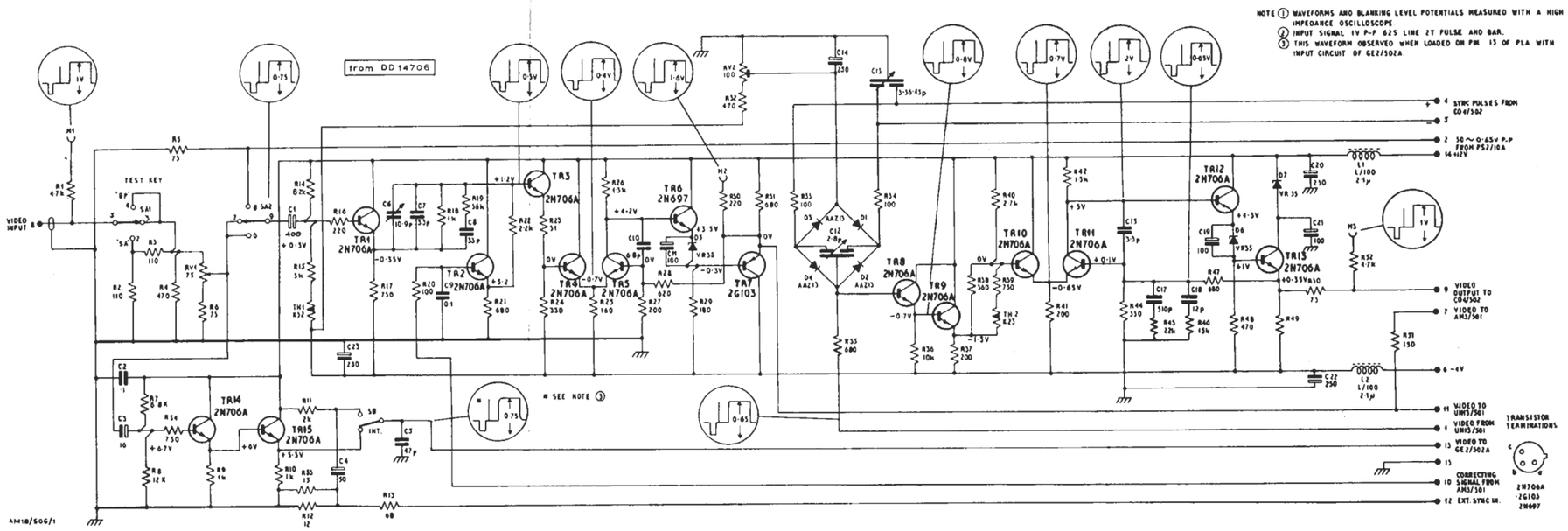

Fig.1 AM18/506: Circuit Diagram

Circuit Description

The circuit diagram is given in Fig. 1. The input signal passes via the spring loaded *Test Stab* key, and via the gain control RV1, to TR1 and TR14. The switch is biased by the spring to its normal (central) position but has to be held in either of the other two positions. In the *SA* position the signal level is reduced by 6 dB for test purposes; in the *BP* position the signal is removed from TR1 and 0·45 volts p-p 50-Hz substituted to enable a check on the efficiency of the clamping action of the parent unit.

TR14 and TR15 are emitter followers which, with the *Int/Ext* switch in the *Int* position, feed composite video to the associated sampling pulse generator.[2] In the *SB* position of the switch, external syncs of the correct amplitude and d.c. level are substituted.

TR1 and transistors TR3 to TR7 form the first of the two amplifiers. The signal from TR1 is fed to the base of TR3 in parallel with any inverted error signal from the associated error-signal sampling and amplifier chain.[3] The corrected signal passes via emitter follower TR4 to the feed back triple TR5 to TR7. This has a gain of about 10 db and a very low output impedance for feeding the delay line[4] and error signal sampling chain. The network R19, C6, C7 and C8 corrects for minor imperfections in transmission performance of the parent unit as a whole.

The signal from the delay line feeds the second of the two amplifiers and the sync stabiliser bridge. The bridge is held non-conductive during picture periods by potentials from an associated unit[5] but, during sync periods, these potentials are overridden by pulses which cause the diodes to conduct. Under these condtions, the base of TR8 is clamped to the potential of the slider of RV2, which thus acts as a sync amplitude control. This action can be inhibited by a switch in the associated unit. Capacitors C12 and C13 are bridge-balancing controls.

The signal on the base of TR8 passes via emitter followers TR9 and TR10 to the feedback triple TR11 to TR13. This has a very low output impedance built out to 75 ohms by R50 for feeding the output.

Maintenance

Routine maintenance is not required. The gain control RV1 is set to approximately mid position so that the overall gain of the parent unit is unity.

Signal waveforms at various points of the circuit are shown on the circuit diagram Fig. 1.

References

1. Designs Department Specification No.6.100(65)
2. Sampling Pulse Generator GE2/502A
3. Error Signal Sampling and Amplifier Chain AM3/501
4. Delay Line UN13/501
5. Sync Pulse Slicer CO4/502

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