Issue 1
23.8.72

DESIGNS DEPARTMENT SPECIFICATION NO. 5.226(72)

OS3/503 Oscillator Variable Frequency

This unit is capable of producing stable frequencies in the range 24MHz to 352MHz at intervals of 8MHz, with an output power of +7dBm.

The various output frequencies are synthesised from a highly stable 5MHz oven controlled crystal oscillator and the required output frequency is selected by the position of 7 'U'-links and a coaxial plug. A lamp on the front panel indicates when the unit is operating normally.

The unit is housed in a CH1/46A and does not include power supplies.

Power supplies	+6V 300mA -6V 150mA -24V 150mA (400mA when unit is cold)
Output power	+7dBm ± 2dB
Output frequencies	24MHz to 352MHz at intervals of 8MHz
Fine frequency adjustment	> 2 parts in 10^5
Output socket	TNC on front panel
Frequency stability	
Long term	Better than ± 5 parts in 10^8 for an ambient temperature between $-10^{\circ}C$ and $+40^{\circ}C$ and supply voltages ± 5% of nominal.
Short term	Peak frequency deviation better than -60dB with respect to 50kHz deviation with 50uS pre-emphasis.
Noise spectrum	Better than -60dB in 1kHz B/W 20kHz from centre frequency.
Spurious outputs	
Sidebands at ± 0.5MHz ± 1MHz ± 1.5MHz	Better than -60dB relative to centre frequency.
Other components within ± 10MHz of centre frequency	Better than -60dB relative to centre frequency.
Harmonics of centre frequency.	Better than -10dB relative to centre frequency.
Sub harmonics of centre frequency	24-176MHz - 45dB 176-352MHz - 35dB
All other spurious outputs	Better than -40dB relative to centre frequency.

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PRODUCTION TEST SCHEDULE

Equipment required:

1. Current limited variable power supplies to supply:

   +6V 300mA
   -6V 150mA
   -24V 400mA

2. Dual trace oscilloscope and two high impedance probes (Tektronix type 585 with type 82 plug-in, or equivalent)

   Band width - $\geq$ 30MHz
   Sensitivity - $\leq$ 100mV/cm

3. High frequency oscilloscope and high impedance probe. (Hewlett-Packard type 183 with plug-in types 1841A and 1830A or equivalent)

   Band width - $\geq$ 350MHz
   Sensitivity - $\leq$ 500mV/cm

   (A lower frequency oscilloscope could be used if an appropriate correction factor is applied to the amplitude of high frequency measurements).

4. Frequency counter which will display frequencies up to 360MHz. (Hewlett-Packard type 5245L with plug-in type 5253B or equivalent).

5. Signal generator (Marconi type TF 801 or equivalent)

   Range - 10MHz to 25MHz
   Output - 10mW in 50 ohms

6. Pulse generator (Calne Electronics type PG 101 or equivalent).

   Range - 250KHz to 500KHz
   Output - Square wave 5V p-p

7. Spectrum Analyser (Hewlett-Packard type 8554L and 8552B or equivalent)

   Frequency range - 0 to 1GHz
   Band width - 1KHz to 100KHz
   Sweep per division - 10KHz to 100MHz
   Dynamic range - $\geq$ 65dB

8. AVO 8

Check that the unit has been manufactured in accordance with the drawings.

BBC

DS/SPA4

Connect the power supplies to the following pins, Earth (0V) Pin 3, +6V Pin 10, -6V Pin 12 and -24V Pin 13 but set all the power supplies to zero volts.

From the block diagram D 31880 A4 it can be seen that the unit consists of a voltage controlled oscillator which is locked to a crystal oscillator by a phase lock loop. Each part of the loop should be tested separately, as follows:

Reference Oscillator

Gradually increase the voltage on pin 13 to -24 volts, the current drawn should be 400mA, this will drop to about 150mA after a few minutes when the crystals oven temperature has stabilised. Increase the voltage on pin 3 to +6 volts, the current drawn should be 300mA ± 50mA.

Use an oscilloscope to check the waveform at the following points:-

TR4 base	- 5MHz, > 0.5V p-p
TR4 Collector	- 5MHz, > 3V p-p
IC9 Pin 12	- 500KHz, > 3V p-p
IC11 Pin 13	- 500KHz, 40nS negative going pulse, > 3V p-p

Programmable Divider

The division ratio of the programmable divider is set by connecting 'U'-links in positions 2, 4, 6, 8, 10 and 12; positions 1, 3, 5, 7, 9 and 11 are rest positions.

'U'-link in position	division ratio
2	1
4	2
6	4
8	8
10	16
12	32

Other division ratios may be obtained by using more than one 'U'-link. e.g. links in positions 4 and 8 corresponds to a division ratio of 2+8, that is, a division ratio of 10.

Unplug PL'D' and connect it to a signal generator set to produce 1V p-p at 10MHz. Connect the Y_1 input of dual trace oscilloscope to pin 11 of IC2 and connect the Y_2 input to pin 10 of IC11. Trigger the timebase from Y_2.

Set the 'U'-links to positions 2, 4, 6, 8, 10 and 11, that is, a division ratio of 31. By observing the number of input pulses per output pulse check that the divider operates correctly with input frequencies from 10MHz to 23MHz. The waveform displayed on the Y_2 trace should be a negative going pulse with an amplitude of at least 3 volts and a duration of about 30nS.

Now set the 'U'-links to positions 1, 3, 5, 7, 9 and 12 (division ratio of 32) and carry out the same check.

If the circuit is faulty connect 'U' links in positions 1, 3, 5, 7, 9 and 11, the circuit should now divide by 64. Pin 5 of IC8a is the output for this test. If it does divide by 64 then the fault must be in the feedback path, that it IC6 and the 'U' links. If it does not divide by 64 then the basic counter must be faulty, that is IC1, IC2, IC3, IC4, IC5, IC7, IC8 or their interconnections on the printed circuit board.

The counter must be capable of operating with an input frequency up to 22MHz. A simple "ripple through" counter will not operate at 22MHz when feedback is applied, therefore a "synchronous" counter has been used. In this type of counter the input signal is applied to the clock inputs of all the bistables, however, only the bistables with a logic 1 on their J and K inputs change state.

Consider the following circuit:-

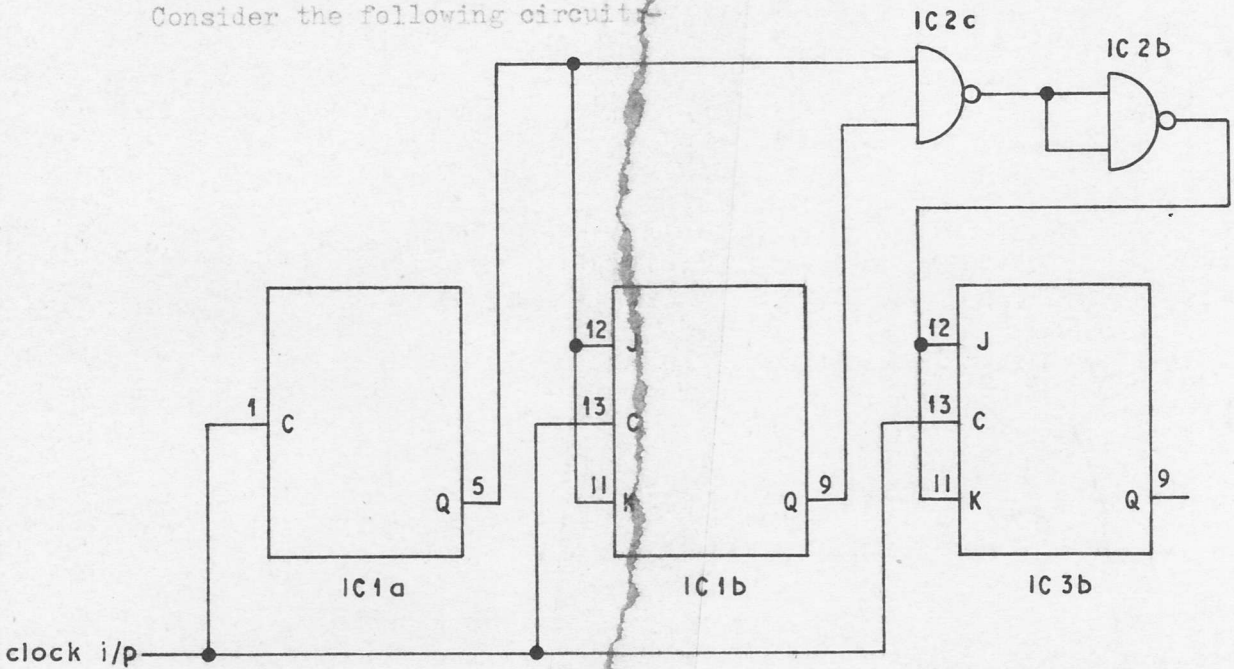


FIG.1 PROGRAMMABLE DIVIDER-SIMPLIFIED DIAGRAM

This is a simplified circuit of the first three stages of the counter. Pins 1 and 13 are clock inputs, Pins 12 and 13 are "J" and "K" inputs respectively and pins 5 and 9 are "Q" outputs. If all the outputs are initially at logic 0 then the negative going edge of the first clock pulse will change the Q output of IC1a to logic 1 but it will not affect the state of IC1b or IC3b because their J and K inputs were at logic 0 (a clock input only changes the state of a bistable if its J and K inputs are at logic 1). The next clock pulse will change the Q output of IC1a to logic 0 and the Q output of IC1b to logic 1. The third clock pulse changes the Q output of IC1a to logic 1 but does not affect the output of IC1b or IC3b. The J and K inputs of IC1b will now be at logic 1 and also, due to the action of gates IC2c and IC2b, the J and K inputs of IC3b will be at logic 1, so the fourth clock pulse will change the state of all three bistables. The fifth clock pulse will set the Q output of IC1a, IC1b and IC3b to 1, 0, 1 respectively and the sixth and seventh pulses will set their outputs to 0, 1, 1 and 1,1,1, respectively. When all the outputs are at logic 1, all the J and K inputs will be at logic 1 so the next clock pulse sets all the Q outputs back to logic 0. Hence the circuit forms a binary counter that divides by 8.

The counter in the OS3/503 operates in the above manner but three more binary stages have been added. In order to find a fault check that the frequency at the Q output of IC1a is half the clock frequency and that the outputs of all the subsequent bistables are ¼, ⅛, 1/16, 1/32 and 1/64 of the clock frequency (check them from left to right on the circuit). If the Q output of one of the bistables is producing the wrong frequency, check that

its J and K inputs are at logic 1 for a period equal to one cycle of the clock frequency, and also check that the frequency is equal to that at the Q output of the previous bistable. If the J and K inputs are correct the fault is probably in the bistable or associated printed circuit board wiring, but if the J and K inputs are incorrect the fault is probably in the gates which drive the J and K inputs or the associated printed board wiring.

Loop Amplifier and Filter

Set the pulse generator to produce a 5V p-p 500kHz square wave and connect it, in place of the coaxial lead, to C202 (tag on BRD 2) and earth. Check that the waveform on the emitter of TR202 is a 20V p-p square wave, and that the voltage on the yellow wire from R208 is about -11 volts with no AC component. Reduce the input frequency to 250kHz and check that the waveform at R208 has a peak-to-peak voltage of between 10 and 24 volts.

The filter has a cut off frequency of 300kHz approximately and very high attenuation at 0.5MHz, 1MHz, and 1.5MHz. The tuned circuits L202/C206 and L205/C212 resonate at 0.5MHz, L204/C210 resonates at 1MHz and L203/C208 resonates at 1.5MHz. The characteristic impedance of the filter is 1000 ohms but it is terminated at its output in a high impedance so that the output of the filter can vary between 0 and -24 volts as the mark space ratio of the input signal is varied. (If it was terminated in 1000 ohms the output would only vary between 0 and -12 volts). Reconnect the coaxial lead to C202 and PL'D' to SK'D'.

Circuits on board 2

The circuits on board 2 (voltage controlled oscillator, high frequency divider and output amplifier) may be tested before the board is mounted in the CH1/57B. Where socket numbers are quoted the relevant pin number is shown in brackets, and coaxial sockets (BNC or SMB as convenient) may be soldered between the earth plane and the pin on the printed circuit board.

Voltage Controlled Oscillator

1. Testing the board outside the CH1/57B.

Connect a variable power supply PSU1 (adjustable between 0 volts and -24 volts) between the earth plane (0 volts) and pin G (0 to -24 volts), also connect pin G to C132. Connect a power supply between the earth plane and pin E (-ve), and connect another power supply between the earth plane and pin F (+ve). Increase the voltage on pin E to -6 volts, the current drawn should be 150mA ± 30mA and increase the voltage on pin F to +6V the current drawn should be 30.mA ± 12mA.

2. Testing the board inside the CH1/57B and mounted in the CH1/46A.

Disconnect the yellow wire from R208 and connect it to R123 (pin on side of CH1/57B). Connect a 100K ohms variable resistor in the position for R7 and place a 'U' link in position 13.

Increase the voltage on pin 12 to -6 volts, the current drawn should be 150mA ± 30mA.

Connect a frequency counter to SK'J' and check that the oscillator can be tuned over the range 176MHz to 352MHz by adjusting R7 (PSU 1). If the output signal from SK'J' (Pin A) is not high enough to operate the counter, then a pick up loop consisting of two turns (diameter about 0.5 inch) of 16 SWG wire connected to a BNC socket type GR35007H can be used. Connect the pick up loop to a frequency counter and hold the loop near L111, but do not hold it closer than necessary to operate the counter as it will load the VCO and reduce its frequency range.

If the oscillator does not cover the correct range unsolder l111 and adjust its length to make the oscillator cover the right range.

High Frequency Divider

Using a high frequency oscilloscope with a high impedance probe check that each divide by two circuit operates correctly over the full frequency range of the VCO. The divider outputs are connected to SK'H' (pin B), SK'G' (pin C), SK'F' (pin D) and SK'D' (track on corner of board) respectively. The first two divide-by-two circuits (IC101 and IC102) are AC coupled, emitter-coupled-logic and their outputs should be greater than 400mV peak-to-peak. The second two divide-by-two circuits are DC coupled, emitter-coupled-logic with logic levels of -0.7 volts (logic 1) and -1.7 volts (logic 0) relative to earth. The mean level at the junction of R104 and R105 should be -1.2 volts relative to earth.

When PL'D' is connected to SK'D' the voltage at SK'D' should be between 0.5V p-p and 1V p-p and the frequency at SK'D' should cover the range 11MHz to 22MHz.

Output Amplifier

Connect a power meter to SK'C' (track on corner of board near SK'K') and link SK'E' (track on side of board near SK'E') to SK'F' (pin D), SK'G' (pin C), SK'H' (pin B) and SK'J' (pin A) in turn and check that the output power is between +5dBm and +9dBm over the full range of the VCO, If necessary adjust R112 in order to obtain the correct output power over the full frequency range (that is, for all settings of R7 or PSU 1). Now connect a spectrum analyser to the output and check that the harmonic and sub-harmonic outputs meet the specification over the full frequency range.

Connect an oscilloscope to SK'D' and check that the frequency at this point varies smoothly as P7 is adjusted from minimum to maximum resistance, when SK'E' is linked to SK'F', SK'G', SK'H' and SK'J' in turn. This test ensures that the high frequency dividers operate correctly when they are loaded by the output amplifier.

If board 2 was tested outside the CH1/57B mount it inside the CH1/57B and connect it up as shown in the drawings, then repeat the above tests, referring to (2) under the heading "voltage controlled oscillator".

Reconnect the yellow wire from D103 to R208.

Phase Lock Lamp Circuit

Put 'U' links in positions 1,3, 5, 7, 9, and 12, connect an oscilloscope to C202 (pin on board 3) and adjust R7 until a 500kHz rectangular waveform is displayed. The rectangular waveform indicates that the loop is in phase lock and the phase lock lamp should now be on.

If there is no signal at C202 then the fault is probably in IC11 or its associated wiring, assuming all the other parts of the oscillator have been tested and are satisfactory. In order to test IC11 connect pin 10 to ground and pin 13 to +5 volts (it is necessary to disconnect the normal inputs to these pins), the voltage at pin 8 should be +0.5 volts (logic 0). Now connect pin 10 to +5 volts and pin 13 to ground, the voltage at pin 8 should be +2.4 volts (logic 1). Pins 10 and 13 are the preset and clear inputs respectively.

Check that the phase lock lamp is extinguished when
(a) the collector of TR4 is shorted to earth
(b) PL'D' is unplugged
(c) R7 is set to its maximum resistance.

Complete Phase Lock Loop

Put 'U'-links in positions 1, 4, 5, 8, 10, 11 and 13, that is a division ratio of 26 and R7 in circuit. Connect a 250 KΩ variable resistor in the position marked R7, and connect an oscilloscope to C202 (pin on board 3). Adjust the variable resistor until a 500kHz rectangular waveform is displayed, then reduce its value until the waveform is almost unstable (make sure that the waveform instability is not caused by false triggering of the oscilloscope). Remove the variable resistor, measure its resistance and find the horizontal line on the resistor selection chart (DSK 15581 A4) that corresponds with the above measurement. The optimum values for the A.O.T. resistors R7 to R12 are given by the points at which the horizontal line intersects the six curves. Select the nearest preferred value to those given on the chart and solder them in position. The table on the resistor selection chart shows which resistor should be used for any particular division ratio, and the required resistor should be selected by placing a 'U'-link in positions 13 to 18.

Diagram removed

By observing the waveform at C202 check that the OS3/503 phase locks on each division ratio between 23 and 44. If the mark-space ratio of the waveform is greater than about 10:1 for any division ratio, then the A.O.T. resistor (R7 - R12) in circuit should be adjusted to reduce the mark-space ratio (however this adjustment should not normally be necessary).

Connect SK'E' to SK'J' and connect a spectrum analyser to the output then check that the spurious sidebands at the centre frequency ± 0.5MHz, ± 1MHz and ± 1.5MHz are more than 60dB below the centre frequency for each division ratio between 23 and 44.
(N.B. Time will be save if the last two tests are combined).

Write the 'U'-link positions required for each division ratio on the paster (D 31881 A4) e.g. when R8 should be in circuit a 'U'-link should be in position 14, so "14" should be written on the paster.

Fine Frequency Adjustment

Set the unit to a high frequency, say 304MHz and connect a frequency counter to PL'C'. Now adjust the frequency to 304MHz ± 10Hz using R16 (N.B. this adjustment should be made when the unit has been on for at least one hour).

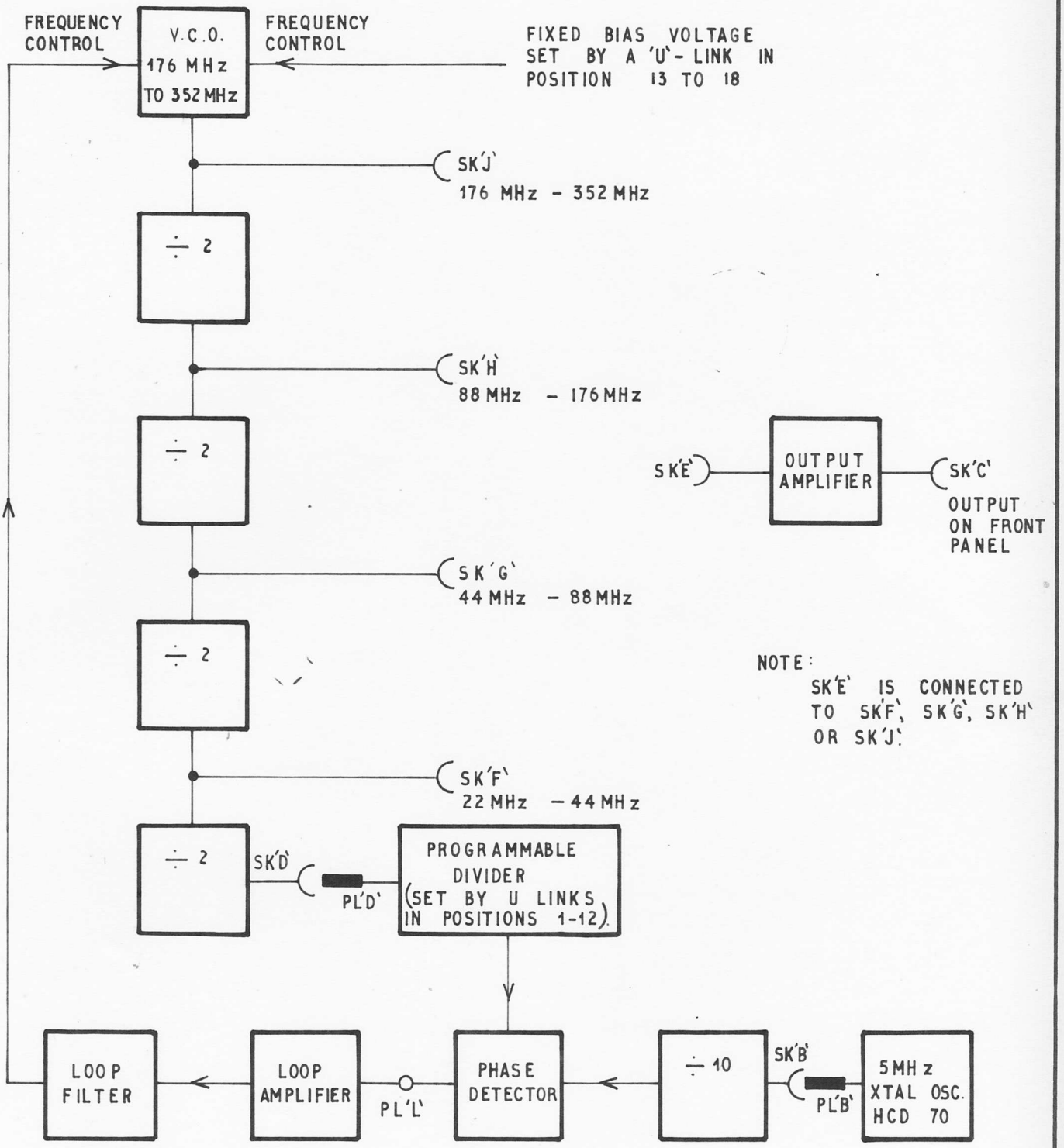
Labelling

If the unit has been set up on a particular frequency requested by the customer, fix a label to the front of the unit showing that frequency.

D31880A4

ISS	CHANGE
1	30/6/78

OS3/503
(OSCILLATOR VARIABLE FREQ)
BLOCK DIAGRAM



BBC
DS/A4

OS3/503
OSCILLATOR VARIABLE FREQ
BLOCK DIAGRAM

DRN.	G.W.W.
TCD.	B.Y.
CKD.	
APPD	

DESIGNS DEPARTMENT
D31880A4

S & H LTD 2285b

D31864A4

sheet 1 of 10 sheets.

OS3/503 OSCILLATOR, VARIABLE FREQUENCY - PARTS LIST

CHANGE	ISS.
6/1/72	1
SPEC'S ADDED. ITEM 7 REVISED. JRS JCR.4-12-72	2
ITEMS 8&9 ADDED. CF.7929-053/503(3) PH. 24.7.73	3.

ITEM No.	No. OFF	SEE NOTES	DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
			DRAWING NUMBERS.		
			Block Diagram D31880A4		
			Circuit D31863A1		
			Parts List D31864A4		
			Assembly & Wiring D31865A2		
			Details 1-6 D31866A2		
			Detail 7&7A D31867A4		
			P.B.Wiring Brd.1 D31868A2		
			P.B. Wiring Brd.1 (Comp.Side) D31869A2		
			P.B. Comp.Loc. Brd.1 D31870A4		
			P.B.Drillings Brd.1 D31871A4		
			P.Bwiring Brd.2 D31872A2		
			P.B.Wiring Brd.2 (Comp.Side) D31873A2		
			P.B.Comp.Loc. Brd.2 D31874A2		
			P.B. Drilling Brd.2 D31875A2		
			P.B.Wiring Brd.3 D31876A3		
			P.B. Wiring Brd.3(Comp.Side) D31877A3		
			P.B. Comp.Loc Brd.3 D31878A4		
			P.B. Drilling Brd.3 D31879A4		
			Freq. Selection Chart (Paster) D31881A4		
			Detail B D31890A3.		
			SPEC ED/053/503		
			FURTHER INFORMATION REQUIRED FOR MANUFACTURE.		
			Unit Assembly Information EA10484		
			Unit Wiring Information EA10137		
			Unit Wiring Information EA10140		
			Unit Wiring Information EA10139		
			Inductor Information EA10127A4		
			Inductor L/12017, L/12018		
			14B/147, 14B/148, 14B/149, 14B/150		
			D31867A4		
			D26951A4. D32105A4. D32106A4.		
			D31477A4-CP		
1	1		Chassis CH1/46A Constructed & Modified		SPEC ED/CH1/46
			By Contractors as follows:-		
			Escutcheon drilled and engraved to:-		D31866A2, Det.1
			Front Bracket drilled to:-		" Det.2
			Rear Bracket drilled to:-		" Det.3
			R/H Cover Plate Drilled to:-		" Det.4
		*	INCLUDING EMBODIMENT LOAN ITEMS ON P.L. D20875 A4		
2	2		Bracket		D31866A2, Det.5
3	2		Block		D31866A2, Det.6
4					
5					
6					
7	1	*	Chassis, CH1/57B modified		SPEC ED/CH1/57.
			by contractor as follows:-		D31890A3, Det.8
8	1	*	PASTER (DYE LINE PRINT)		D31881A4
9	1		LABEL		D31867A4 DET.7A.

BBC

DS/PLA4

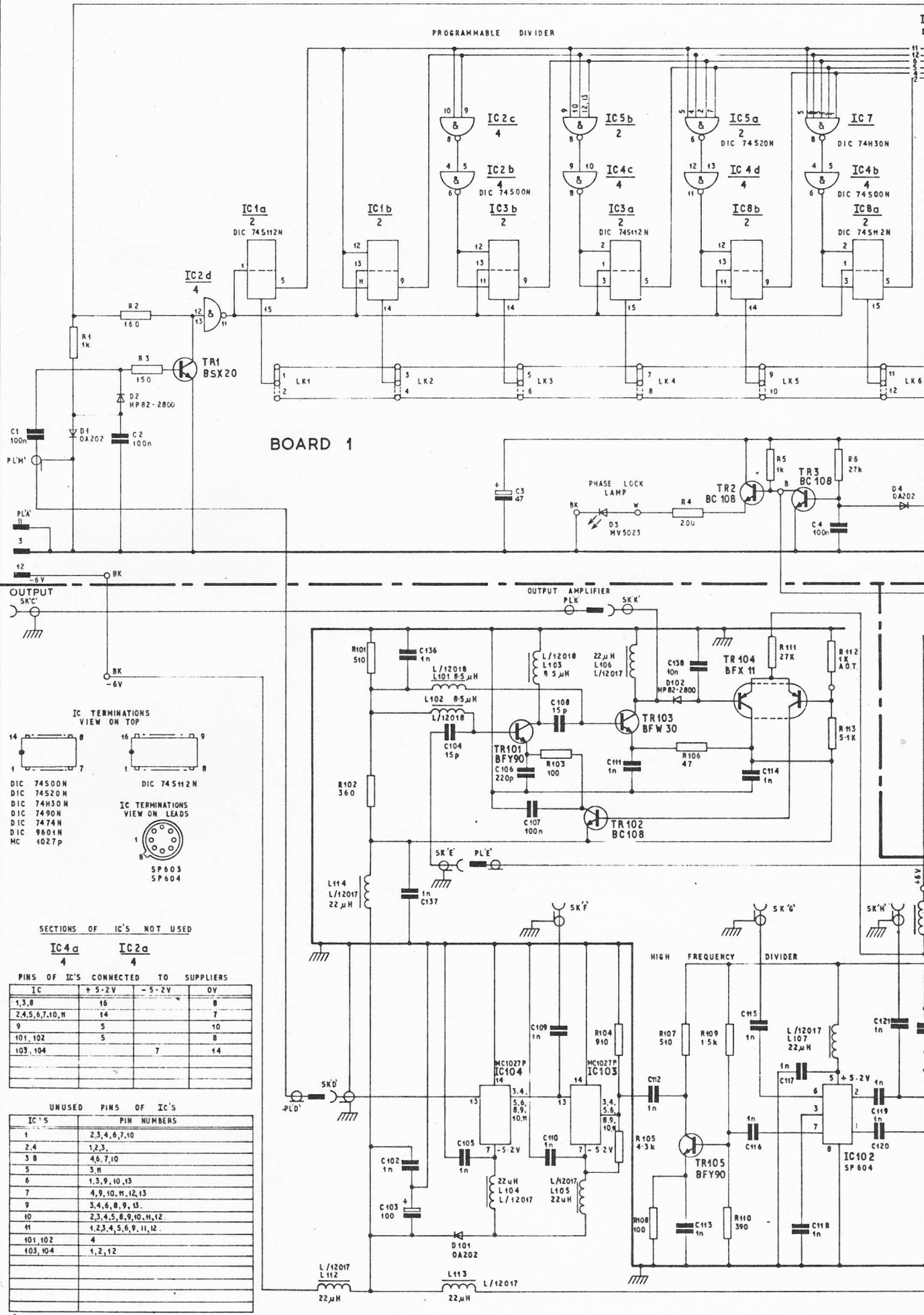
OS3/503
OSCILLATOR, VARIABLE FREQUENCY
Parts list

DRN.	G.M.W.
TPD.	
CKD.	M.T.E.
APPD.	

DESIGNS DEPARTMENT

D31864A4.

sheet 1 of 10 sheets

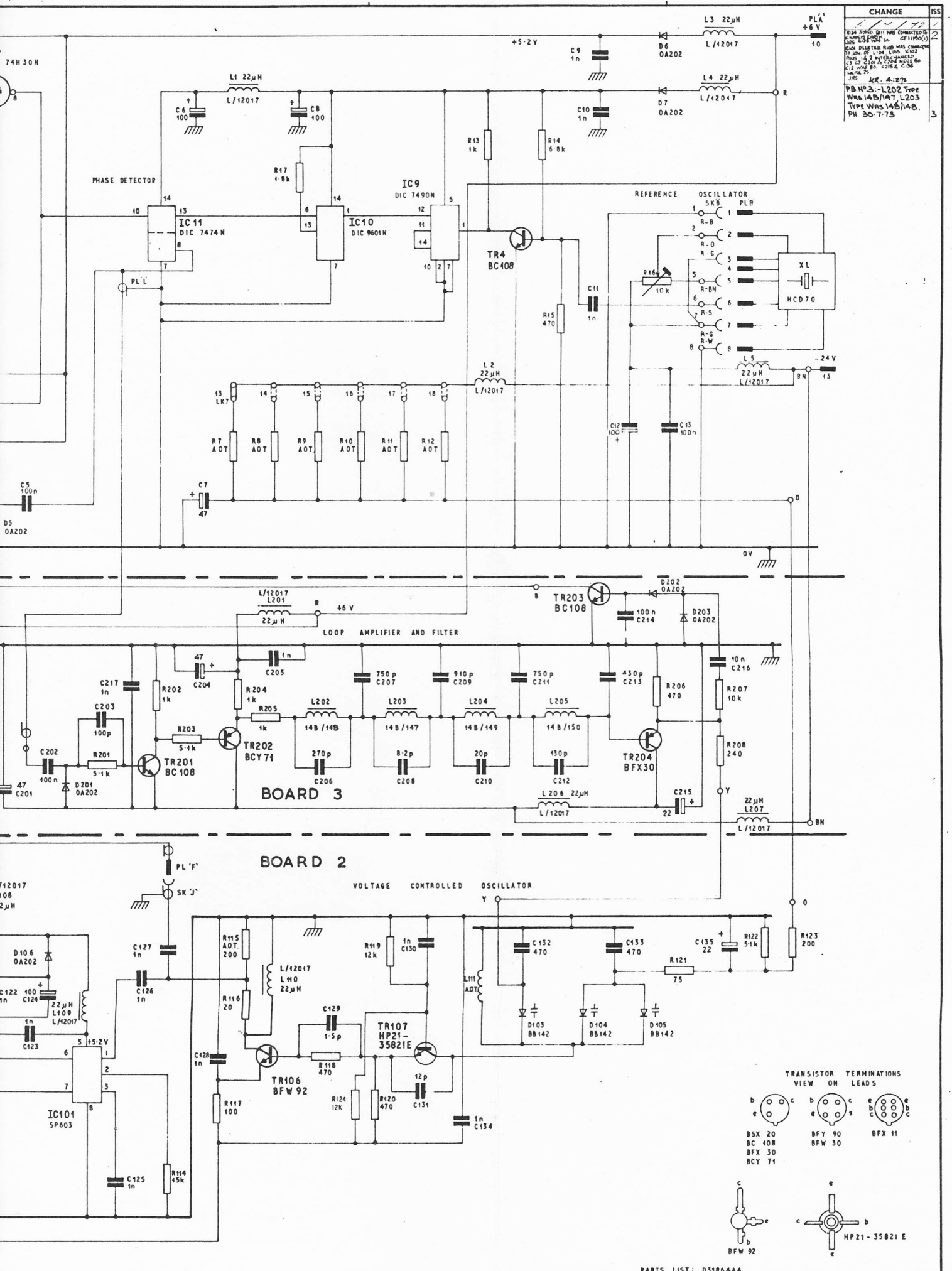


D 31863 A1

OS3/503 (OSCILLATOR, VARIABLE FREQUENCY) CIRCUIT

BBC DS/A1

OS3/503 (OSCILLATOR VARIABL



PARTS LIST: D31864A4

FREQUENCY CIRCUIT

DRN.	G W W	DESIGNS DEPARTMENT
TCD.	B Y	
CKD.	M J E	D31863A1
APPD.		