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19.9.74

DESIGNS DEPARTMENT MANUFACTURING INFORMATION

NO. 5.258(74)

Oscillation Variable Frequency

(Frequency Synthesiser)

OS3/507

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JJS

D.D.M.I. NO. 5.258(74)
Title Sheet

BBC

DS/SPA4

DESIGNS DEPARTMENT MANUFACTURING INFORMATION

NO.5.258(74)

OSCILLATOR VARIABLE FREQUENCY

(FREQUENCY SYNTHESISER)

OS3/507

C O N T E N T S

Specification

Production Test Schedule

D R A W I N G S

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Parts List	D 36142 A4
Assembly and Wiring	D 36143 A1
Details	D 36144 A1
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Codes & Frequencies in OS3/507	DSK 16262 A3

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DESIGNS DEPARTMENT MANUFACTURING INFORMATION

NO.5.258(74)

OSCILLATOR VARIABLE FREQUENCY

(FREQUENCY SYNTHESISER)

OS3/507

1. INTRODUCTION:

This unit is a frequency synthesiser for use in the UHF Test Equipment type EP14M/507. It can produce frequencies in the range 908MHz to 1284MHz at intervals of 8MHz with a high degree of stability. These frequencies are used in the EP14M/507 to produce input and output channels 21 to 68. (There are two synthesisers in each UHF Test Equipment, one for the transmitter section and one for the receiver section). The output frequency is selected by setting code switches on the front panel of the EP14M/507, to the required channel.

Good frequency stability is obtained by phase locking the voltage controlled oscillator (VCO) to a very stable reference oscillator (OS2/526). Provision is made for the phase locked loop to be broken so that the VCO frequency can be controlled by an external voltage. This facility is used in the EP14M/507 in order to provide frequency sweep and spectrum analyser facilities.

The VCO has two indentical outputs at approximately +8dBm and with about 30dB isolation. When phase locked one of the outputs is used to drive the phase locked loop, but when the VCO is used in the sweep mode both outputs may be used to drive external circuitry. This facility enables a tracking generator / spectrum analyser function to be provided in the EP14M/507.

The synthesiser also produces an output in the range 8MHz to 384MHz which can be phase locked at intervals of 8MHz or swept.

An output for a light emitting diode is provided to indicate when the unit is functioning correctly. The light goes out when the VCO is phase locked or when the sweep facility has been selected.

The synthesiser has been designed to enable channels 21 to 68 to be produced. If the code switches are set below channel 21 or above channel 68 a false output is obtained.

Further information may be found in Designs Department Technical Memorandum No. 5.91(74).

2. MECHANICAL

The unit consists of three printed circuit boards. Board 2 (VCO and UHF amplifiers) is 3.75" x 1.5" and mounted inside a metal box which is mounted on Board 1. Board 1 (8" x 5") is mounted inside a chassis type CH1/68; this is

the standard chassis used in the EP14M/507. Board 3 (DC control circuitry) is 6" x 4.8" and it is connected to Board 1 by a 15 way cable. Board 3 is normally mounted without a chassis on the side panel of the EP14M/507. A 10 way cable is used to connect a two digit code switch to Board 3.

Internal and external RF connectors on the CH1/68 are type SMB and supply and switching connections are coloured feed-through terminals. All connections are on the end faces of the unit but monitor points and a pre-set control are on the top of the unit.

Weight	2lb.
Size	8" x 5" x 1¼" + unmounted PCB 6" x 4.8".

3. ELECTRICAL:

Output frequencies

Main (UHF)output	908MHz to 1284MHz at intervals of 8MHz when phase locked, or continuous on sweep mode.
VHF Output	8MHz to 384MHz at intervals of 8MHz when phase locked, or continuous on sweep mode.

Input Required

Reference frequencies	0.5MHz, TTL 900MHz, at -5dBm approx } Normally obtained from OS2/526.
Supply Voltages	+12 volts ± 0.1 volts at 600 ± 100MA -12 volts ± 0.1 volts at 60 ± 10MA

Output Levels

Main (UHF) output	+8dBm ± 3dB into 50Ω
VHF output	-10dBm ± 3dB into 50Ω

Method of Setting Frequency

Two BCD code switches
Main output frequency:
=900 + 8(N-20)MHz
VHF output frequency:= 8(N-20)MHz
Where N is the number indicated.

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Spurious Outputs from PLB

(Main UHF output)

$f_{out} \pm 0.5$MHz $f_{out} \pm 1$MHz $f_{out} \pm 1.5$MHz	Better than -60dB relative to centre frequency.
Harmonics of f_{out} (lowest harmonic is 1816MHz)	Better than -10dB (not measured accurately due to lack of equipment)
900MHz Breakthrough	Better than -35dB relative to centre frequency.
Breakthrough from another synthesiser driven from the same OS2/526	Better than -55dB relative to centre frequency.
Other spurious outputs	Better than -65dB relative to centre frequency.

Spurious Outputs from PLG

(VHF Output)

$f_{out} \pm 0.5$MHz $f_{out} \pm 1$MHz $f_{out} \pm 1.5$MHz	Better than -60dB relative to centre frequency.
Harmonics of f_{out}	Better than -20dB relative to centre frequency over the range 25MHz to 250MHz
Other spurious outputs	Better than -35dB relative to centre frequency.

Frequency Stability - Both Outputs

Long Term	Entirely determined by the long term stability of the OS2/526 when the VCO is phase locked. Better than $\pm$ 10MHz for a constant input voltage applied to the sweep input over a temperature range from +20°C to 50°C.
Short Term(Noise)	Better than -45dB relative to centre frequency in a 1kHz bandwidth 20kHz from centre frequency. Better than -65dB relative to centre frequency in a 1kHz bandwidth more than 150kHz from centre frequency.

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Frequency Deviation (Noise)	Less than 300Hz RMS measured in a 15kHz bandwidth.
Sweep/Phase Locked Control	-12 volts applied to 'sweep/phase lock' input breaks the phase locked loop and connects the 'sweep' pin to the VCO.
Sweep Input	VCO tunes non-linearly over the range 908MHz to 1284MHz by applying voltages in the range ± 11 volts. Typically 908MHz = +9V and 1284MHz = -5.8V.
VCO Gain	
Coarse varactor input at 900MHz	60MHz/V
at 1300MHz	5MHz/V
Fine Varactor Input	
900MHz to 1300MHz	Between 3 and 8MHz/V

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DESIGNS DEPARTMENT MANUFACTURING INFORMATION NO. 5.258(74)

Oscillation Variable Frequency

(Frequency Synthesiser)

OS3/507

PRODUCTION TEST SCHEDULE

1. Drawings

Circuit	D 36141 A1
Assembly and Wiring	D 36142 A1
P.B. 3 Comp. Loc.	D 36153 A3
Codes and Frequencies	D 16262 A3

2. Test Equipment

	Example
Power Supplies + and -12 volts at 1 amp	
500kHz Oscillator, accuracy 1 part in 10^7, noise better than -70dB in 1kHz B/W 20kHz from centre frequency. TTL output	OS2/526
900MHz Oscillator -5dBm into 50Ω accuracy and noise as 500kHz oscillator	OS2/526
Oscilloscope and High impedance probe. Bandwidth 35MHz	Telequipment D67
UHF Spectrum Analyser 1 - 1285MHz	Hewlett Packard 141T, 8554L, 8552B, 8558B.
Probe for Spectrum Analyser 5K x 100	
Digital Voltmeter	Solatron LM 1619
Power Meter	Hewlett Packard 432A
Frequency Counter 900MHz to 1300MHz	Hewlett Packard 5245L, 5254A
Attenuator variable in 1dB steps, Zo = 50Ω	
AVO 8	

3. Mechanical Inspection

Check that the unit has been satisfactorily manufactured in accordance with the drawings. In particular check that there is enough clearance between the cases of the transistors and that the transistors in the VHF amplifier have been wired with the shortest possible leads. Check that none of the leadless disc capacitors are broken and that they are soldered securely.

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4. Alignment and Test

4.1 The parts of this test schedule marked with vertical lines contain circuit information and testing instructions which need only be carried out if a fault exists in the relevant part of the unit (single line), or if a test jig is not available (double line).

4.2 Code Converter, Demultiplexer and Digital to Analogue Converter (Board 3)

Plug Board 3 into the 15 way socket on the side of the test jig B (supplied by D.D.) and connect the lead from the test jig to the code switch lead from board 3. Connect positive and negative power supplies to the red and blue sockets on the side of the box (the black socket is earth), and gradually increase the voltages to + and -12 volts while monitoring the currents. The current consumption should be as follows:

+12 volts, code switch set to 20 - 80mA ± 10%
+12 volts, code switch set to 21 - 60mA ± 10%
-12 volts, any code switch setting - 7mA ± 30%

4.3 Code Converter

The light emitting diodes labelled 9, 10, 11, 12, 13 and 14 will now come on when the voltages on PLD 9 to 14 respectively are at logic 1. Set the code switch as shown in table 1 and check that the output code on PLD is correct.

4.4 If the output code is not correct check the voltage on 3D1; it should be 5.1 volts, ± 0.1 volts. If it is correct connect sockets 1, 2, 3, 4 and 5 to test points 3TP1, 2, 3, 4 and 5 respectively. Light emitting diodes 1, 2, 3, 4 and 5 will now indicate the state of the intermediate code. Set the code switch as shown in table 1 and note the intermediate code. If the intermediate code is correct the fault is in the binary adders (3IC4 and 3IC5) or associated circuitry, if it is wrong the fault is in the gates (3IC1, 3IC2 and 3IC3) or associated circuitry. For further investigations a probe connected to one of the sockets 1 to 5 may be used to discover the logic levels on other parts of the circuit; the associated LED comes on when the logic is at level '1', i.e. +5 volts.

TABLE 1

Code Switch Setting		Code Switch Output		Intermediate Code					Output Code PLD					
Tens	Units	Tens MSB LSB	Units	3TP5	3TP4	3TP3	3TP2	3TP1	14	13	12	11	10	9
2	1	0010	0001	1	1	1	1	1	0	0	0	0	0	0
2	2	0010	0010	1	1	1	1	1	0	0	0	0	0	1
2	3	0010	0011	1	1	1	1	1	0	0	0	0	1	0
2	4	0010	0100	1	1	1	1	1	0	0	0	0	1	1
2	5	0010	0101	1	1	1	1	1	0	0	0	1	0	0
2	6	0010	0110	1	1	1	1	1	0	0	0	1	0	1
2	7	0010	0111	1	1	1	1	1	0	0	0	1	1	0
2	8	0010	1000	1	1	1	1	1	0	0	0	1	1	1
2	9	0010	1001	1	1	1	1	1	0	0	1	0	0	0
3	0	0011	0000	0	0	1	0	0	0	0	1	0	0	1
3	1	0011	0001	0	0	1	0	0	0	0	1	0	1	0
4	0	0100	0000	0	1	0	0	1	0	1	0	0	1	1
4	2	0100	0010	0	1	0	0	1	0	1	0	1	0	1
5	0	0101	0000	0	1	1	1	0	0	1	1	1	0	1
5	3	0101	0011	0	1	1	1	0	1	0	0	0	0	0
6	0	0110	0000	1	0	0	1	1	1	0	0	1	1	1
6	8	0110	1000	1	0	0	1	1	1	0	1	1	1	1

4.5 Demultiplexer

Light emitting diodes should come on as shown in table 2.
(N.B. Output PLD3 is not used but it should be checked).

TABLE 2

Code Switch Number	LED	Connected to
21 - 28	A on only	PLD 7
29 - 36	B on only	PLD 6
37 - 44	C on only	PLD 5
45 - 52	D on only	PLD 4
53 - 60	E on only	PLD 3
61 - 68	All off	

4.6 The demultiplexer produces a logic 1 (+5 volts) on one of 5 output pins according to the value of the 3 bit binary number connected to its input. The logic 1 on one of its output pins is used to switch on a transistor which acts as a constant current source of 0.5mA - 0.1mA. If the light emitting diodes A to E do not come on as indicated above the fault is either in the demultiplexer 31C7, transistors 3TR13 to 3TR17 or their associated circuitry.

4.7 Digital to Analogue Converter.
Disconnect SKD 8 wire (B/W) when testing without jig.
Turn 3R29 fully clockwise and connect a digital voltmeter between the green socket (which is connected to PLD 8) and -12 volts (blue socket). Set the code switch and adjust the potentiometers as shown in table 3.

TABLE 3

Code Switch Setting	Adjust	For Voltmeter Reading
46	3R23	12 ± 0.2 volts
21	3R28	21 ± 1 volt
68	3R28	3 ± 1 volts, if necessary

4.8 Now vary the code switch from 21 to 68 and check that the voltmeter reading changes by 0.4V ± 0.2V per step. If limiting occurs at both ends of the range turn 3R28 clockwise to reduce the voltage swing. The output voltages should now be within the tolerances shown in table 3 for channels 21 and 68; the tolerance for channel 46 is not important except as a starting point for setting 3R23 and 3R28. It has been found that the voltage step between code switch setting 52 and 53 is most likely to need adjustment. Therefore A.O.T. 3R10 on code switch setting 53 to give 0.4V less than code switch setting 52.

4.9 If the output voltage does not increase for every code switch increment the fault is in 3TR2, 4, 6, 8, 10 or 12 or their associated circuitry. For instance if the output only changes on alternate code switch settings the fault is associated with 3TR12, or if the output decreases instead of increasing on alternate code switch settings the fault is associated with 3TR10 and so on.

Re-Connect SKD 8 wire (B/W) if tested without J19.

4.10 Set 3R29 to approximately its mid position.

4.11 Code Converter, Demultiplexer and Digital to Analogue Converter (Board 3) Test Procedure without the use of a Test Jig.

Connect two BCD code switches to SKA and SKB and connect positive and negative power supplies to PLD 2 and PLD 15 respectively (PLD 1 is earth). Gradually increase the voltages to + and -12 volts while monitoring the currents. The current consumption should be as follows:

+12 volts 40mA ± 10%
-12 volts 7mA ± 30%

4.12 Code Converter

The code converter uses complementary metal oxide silicon integrated circuits which, in this circuit, should have a supply voltage of +5.1 ± 0.1 volts. The logic 1 level is equal to the supply voltage +0, -0.2 volts, and the logic 0 level is +0.1 volts ± 0.1 volts; however, the source impedance is in the region of 5KΩ so a high impedance voltmeter should be used to measure the logic levels.

4.13 Set the code switch to the number shown in table 1 and check that the correct logic levels appear on PLD 9 to 14. If the output code is not correct check the intermediate code (see paragraph 4.4).

4.14 Demultiplexer

The demultiplexer produces a logic 1 on one of 5 output pins according to the value of the 3 bit binary number connected to its input. The logic 1 on one of its output pins is used to switch on a transistor which acts as a constant current source of 0.5mA ± 0.1mA. Check that the appropriate transistors is switched on by connecting an ammeter between its collector and +12 volts. The transistor should be switched on as shown in Table 4.

TABLE 4

Code Switch Numbers	Transistor Switched On	PLD
21 - 28	3TR17 only	7
29 - 36	3TR16 only	6
37 - 44	3TR15 only	5
45 - 52	3TR14 only	4
53 - 60	3TR13 only	3
61 - 68	None	

4.15 If the transistors do not come on as indicated above the fault is either in the demultiplexer 3IC7, transistors 3TR13 to 3TR17 or their associated circuitry.

4.16 Digital to Analogue Converter

Proceed as shown in paragraphs 4.7, 4.8, 4.9 and 4.10 but connect the voltmeter between -12 volts and PLD8.

4.17 Printed Circuit Boards 1 and 2

Mount the OS3/507 chassis on a test jig A supplied by Designs Department and connect the coloured leads to their respective coloured feedthrough tags. Also connect the 500kHz output from the OS2/526 to PLA, and the 900MHz output to PLE via a 1dB stepped attenuator. Connect PLD to the 15 way plug on test jig B, plug board three into the socket on test jig B and connect the lead from test jig B to SKA and SKB. Do not connect power supplies to test jig B as in the previous sections, instead connect positive and negative power supplies to the red and blue sockets on test jig A. Gradually increase the voltage to + and -12 volts while monitoring the currents. Jig consumption should be as follows:

+12 volts 720mA ± 10%
-12 volts 720mA ± 10% (cold)

Check that the voltage on 1D12 (orange tag) is +5 volts ± 0.1 volts.

NOTE: If test jig A is not available see paragraph 4.40.

4.18 Voltage Controlled Oscillator

Refer to D.D. 5.101(75) Designs Department Tech. memo.

Description of a System for Measuring the Gain Versus Centre Frequency of a Voltage Controlled Oscillator (With Particular Reference to the OS3/507 VCO)

4.19 VHF Amplifier

Set the input level to PLE to -5dBm, connect PLC to PLF and connect a spectrum analyser to PLG. Set the analyser controls as follows:

Bandwidth	300kHz
Scan Width	50MHz/div
Video Filter	Off
Input Attenuator	10dB
Reference Line Level	0dBm
Scan Time	2mS/div
Centre Frequency	250MHz

Switch on SA and adjust RA to tune the VCO over its full range. Check that the following specification is met.

Output Frequency range at PLG	25 - 250MHz
Output level over the above frequency range	-6 ± 4
Harmonics (relative to the fundamental)	better than -20dB
Other spurious outputs (relative to the fundamental)	better than -35dB

4.20 High Frequency Divider Chain

Connect an oscilloscope probe to 1IC7 pin 7, switch on SA and tune the VCO over the range 908 - 1284MHz. Check that the waveform on the oscilloscope indicates a mean level of +3.8 ± 0.2 volts, is at least 0.8 volt peak to peak and varies in frequency from 0.5MHz to 24MHz.

4.21 If the waveform on 1IC7 pin 7 is not correct check test points 1TP3 and 1TP4 and the junction of IC76 and 1R86. Use a 5K x 100 probe connected to a high frequency oscilloscope (B/W 500MHz) or a spectrum analyser. Table 5 gives typical waveforms and harmonic levels.

4.22 Programmable Divider

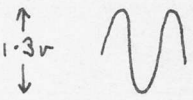
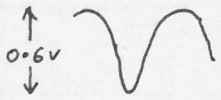
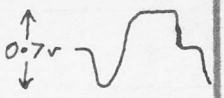
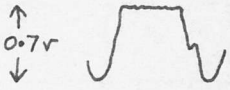
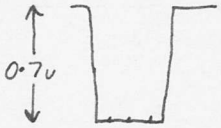
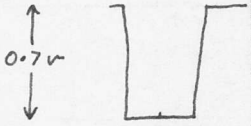
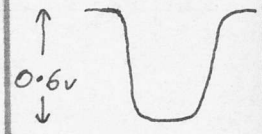
Set the code switch to 21 and connect an oscilloscope probe to the collector of 1TR20. Switch on SA and adjust RA to tune the VCO to 1000MHz ± 5MHz (use a frequency counter connected to PLB). The waveform displayed should have a frequency of 6.2MHz and a peak to peak amplitude of 4 ± 1 volts. Set the oscilloscope time base such that one cycle occupies 0.25 divisions then by setting the code switch to 22, 24, 28, 36 and 52 in turn, check that one cycle occupies 0.5, 1, 2, 4 and 8 divisions respectively. Repeat this test with the VCO set to 906MHz and 1290MHz. IC1B pin 9 - check square wave is present.

4.23 Frequency Detector and Phase Detector Inhibit

Set the code switch to 44, switch on SA and adjust RA to tune the VCO to 1092MHz ± 5MHz (use a frequency counter connected to PLB), the frequency at the collector of 1TR20 should now be 0.5MHz approximately. Connect an AVO set to 2.5 volts FSD between 1TP1 and 1TP2 then adjust 1R13 for zero volts on AVO.

TABLE 5

Typical Waveforms and Harmonic Levels

Test Point	Harmonic Number	Frequency at PLG ± 10%		
		8MHz	50MHz	380MHz
Junction of 1R86 and 1C76				
	1	-27dBm	-23dBm	-30dBm
	2	-60dBm	-57dBm	-50dBm
	3	-47dBm	-43dBm	-60dBm
1TP4				
	1	-41dBm	-31dBm	-40dBm
	2	-54dBm	-43dBm	-51dBm
	3	-49dBm	-42dBm	-70dBm
	4	-61dBm	-49dBm	-65dBm
	5	-58dBm	-50dBm	
1TP3				
	1	-33dBm	-31dBm	-36dBm
	2	-54dBm	-51dBm	-49dBm
	3	-40dBm	-41dBm	-54dBm
	4	-54dBm	-52dBm	-60dBm
	5	-45dBm	-47dBm	
	6	-58dBm	-54dBm	
	7	-48dBm	-49dBm	
1IC8 pin 3	0.6 volt peak to peak square wave			
1IC7 pin 7	1 volt peak to peak square wave			

4.24 The voltage on the wiper of 1R13 should now be equal to the mean d.c. voltage at the output of the monostable 1IC1b pin 9, and this should be +1 ± 0.3V.

4.25 Using an AVO check that the voltage relative to earth on 1TP1 decreases and on 1TP2 increases with VCO frequency and vice-versa.

4.26 Put LK1 in position L and adjust 1R19 so that the collector of 1TR3 is at +5V only when the VCO frequency is between about 1050MHz and 1150MHz, 1R19 controls the width of the window. Use RA to tune the VCO. Width of window must not be less than 100MHz.

4.27 Class 'D' Amplifier, Gain Control and Filter.

Put LK1 in position M, this 'disenables' 1IC2b and 'enables' 2IC2c which feeds the 500kHz reference signal from PLA to the class 'D' amplifier. Set the code switch to 21, connect an oscilloscope probe to SKL and adjust 3R29 to obtain a 500kHz square wave with an amplitude of 0.7 ± 0.2 volts peak to peak (ignore any overshoots). Increase the code switch setting and check that the peak to peak voltage on SKL increases by about 0.3 volts for each unit increase in the code switch setting, to a maximum of 16 ± 1 volts.

4.28 If the voltage on SKL does not vary as stated in 4.27 check that the voltage on SKD 8 varies from about -1 volt to -10 volts between channels 21 and 68. Also check that 1IC4 pin 6 varies from about +1 volt to +10 volts and that emitter followers 1TR7 and 1TR8 operate correctly. (N.B. The mean voltage at SKL should be +0.6V relative to earth when the mark space ratio is 50-50).

4.29 Variable Attenuator

Switch off SA, short the junction of 1R59, 1R60, 1R61 and 1R62 to earth, and connect an AVO 8 (10 volt range) between the filtercon 2C2 on the VCO (+ve lead) and the collectors (cases) of the transistor listed in Table 6. Check that the voltage drops to less than 0.5 volts as shown in the table.

Code Switch Number	Voltage 0.5 volts on 1TR- only
21 to 28	19
29 to 36	18
37 to 44	17
45 to 52	16
53 to 60	None
61 to 68	None

Remove the short to earth.

4.30 Summing Integrator.

Switch on SA. Set the code switch to 44 and adjust RA to obtain an equal voltage on 1TP1 and 1TP2. (Short TP1 to TP2). Check that the voltage on 1IC5 pin 6 SKM is 0 ± 0.2 volts, remove short TP1-2. Adjust RA and check that the voltage varies between at least ± 5 volts.

4.31 Set the code switch to 61, and vary RA so that the voltage on 1IC5 pin 6 SKM varies by ± 0.1 volts about 0V. Check that the voltage on the collector (case) of 1TR19 swings from at least +11.25 volts to -11V.

4.32 Closed Loop Operation.

Switch off SA and ensure that LK1 is in position M. Switch on SA. The frequency detector should now pull the VCO to a frequency determined by the code switch. Set the code switch to 44 and adjust 1R13 to set the VCO to 1092MHz ± 5MHz (use a frequency counter connected to PLB). Now change the code switch to all channels and check that the VCO is pulled to approximately 900 + 8 (N-20)MHz (where N is channel number).

4.33 If when channel 24 is selected the VCO is pulled below 900MHz it is probable that the fualt is in 1D15, 1D16, the light emitting diode or the phase lock lamp circuit. For the operation of this circuit see Technical Memorandum 5.91(74).

4.34 Put LK1 in position L and set the code switch to 44, the VCO should now be phase locked at 1092MHz ± xHz, where x is determined by the stability of the 500kHz and 900MHz reference signals.

4.35 The following adjustments should be made when the unit is warm. (35°C +) Change the code switch to 24 and connect an oscilloscope to SKL, a 500kHz rectangular wave should now be displayed, and the phase lock lamp should be off. Adjust 1R13 to set voltage SKM to TR11b to approx. +0.65V. If instability occurs see section 4.37.

4.36 Using a frequency counter connected to the UHF (PLB) outputs, check that the VCO phase locks at the correct frequency for every code switch setting between 21 and 68. DSK 16262A3 shows most of the frequencies and codes in the synthesiser for all its output channels. If the VCO will not phase lock on channels 21, 22 and 23 repeat the procedure for setting 1R13 (given in 4.35) on channel 21. Also see 4.37.

Connect a spectrum analyser to the UHF (PLB) output and set the controls as follows:

Bandwidth	3kHz
Scan Width	20kHz/div
Video Filter	10Hz
Input attenuator	20dB
Reference line level	Equal to main output level
Scan Time	1s/div
Centre Frequency	Tune to output frequency

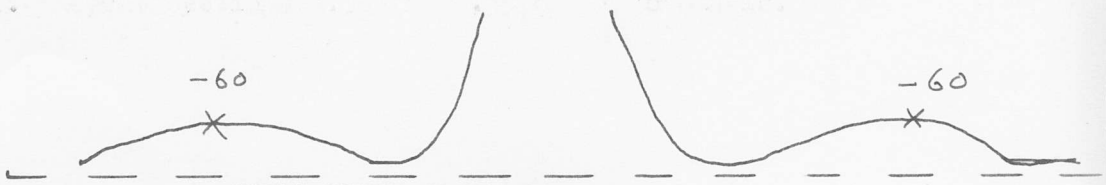
4.37 Due to variations in the gain of different samples of the voltage controlled oscillator (caused mainly by 2TR3, 2D2 and 2D3) the following adjustments are necessary,

1. Select channel 21 or worst channel (sometimes 31) and examine the noise spectrum using the settings given above.

2. Disconnect 1R110 and use 3R29 to increase the square wave at SKL until it just becomes unstable. Its peak to peak voltage should be between 2 and 3 volts, if it is not adjust the resistor 1R115 and repeat the test.

3. Reconnect 1R110 (the feed to 2D3) and adjust 1R110 to make the square wave at SKL just unstable when its voltage is 1.5V p-p on channel 21. (Absolute min. 1.1V typ. 1.3V). Readjust the voltage to 7V p-p.

4. If the noise spectrum still does not meet the specification change 2D3 and repeat 1 to 3.



IDEAL NOISE SPECTRUM
CH21
FIG. 1

4.38 Short Term Frequency Stability

Connect a spectrum analyser to the UHF (PLB) output and set the controls as follows:-

Bandwidth	3kHz
Scan Width	20kHz/div
Video filter	10Hz
Input attenuator	20dB
Reference line level	Equal to main output level
Scan time	1s/div
Centre Frequency	Tune to output frequency

Check that the noise sidebands meet the following specification:

(a) Better than -46dB relative to centre frequency level in a 1kHz bandwidth 20kHz from centre frequency.

(b) Better than -65dB relative to centre frequency level in a 1kHz bandwidth more than 150kHz from centre frequency.

On some channels noise 'ears' will appear about 60kHz from the centre frequency, this is the natural resonant frequency of the phase loop. The 'ears' should be at least 55dB below the centre frequency level. Measure on all channels. NOTE: High channels worse; 64+ may be out of spec.

4.39 Spurious Sidebands

Connect a spectrum analyser to the UHF (PLB) output and set the controls as follows:

Bandwidth	300kHz
Scan Width	0.5MHz/div
Video Filter	Off
Input Attenuator	20dB
Reference line level	Equal to main output
Scan Time	AS APROPRIATE
Centre frequency	Tune to output frequency

Iss. 2
16.7.76

Check that the 0.5, 1 and 1.5MHz sidebands are at least 60dB below the centre frequency level. If the 0.5MHz sidebands are too large adjust the cores of 1L7 and 1L10 to obtain minimum sideband level. Measure on all channels typical value -70dB.

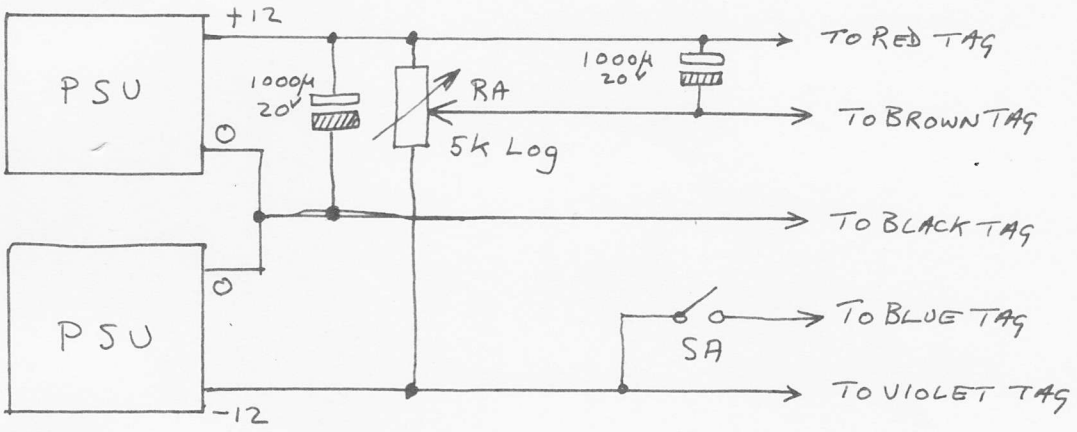
4.40 Phase Lock Lamp

Check that the lamp comes on momentarily each time a new channel is selected.

4.41 The phase lock lamp should come on when the frequency detector is inhibiting the phase detector or when a large AC signal appears on the varactor diode. But it is switched off when RLA1 is energised so that the VCO may be swept without the lamp flickering.

4.42 Test Procedure without Test Jig A

If test jig A is not available the following circuit should be constructed:



Now follow the test procedure starting at 4.17.

4.37 Set the code switch to channel 21 and decrease the level of the 900MHz signal applied to PLE until the synthesiser looses phase-lock, increase the level by 1dB then check that the synthesiser will phase lock each time channel 21 is selected, note the level of the 900MHz signal. Set the code switch to channel 68 and increase the 900MHz level until the synthesiser looses phase lock, reduce the level by 1dB and note the new level. Write the two noted levels on the top of the unit.

BBC

DS/SPA4

D36142A4

SHEET 1 OF 19 SHEETS

ISS.	CHANGE	
1	12-3-74	* ADDED. SPEC. ADDED. E.L. 22.3.74
2		
3		ITEM 12 '*' ADDED D37415A3 ADDED DSK 16262 A3 ADDED B.W.M.S.H. 17-4-75

OSCILLATOR, VARIABLE FREQENCY
PARTS LIST
053/507

ITEM No.	No. OFF		DESCRIPTION		C'C'T REF.	BBC REF. OR DRG. No.
			DRAWING NUMBERS			
			CIRCUIT	D36141A1		
			PARTS LIST	D36142A4		
			ASSEMBLY & WIRING	D36143A1		
			DETAILS	D36144A1		
			P.B. WIRING (BD. No 1)	D36145A2		
			P.B. " , COMP SIDE (" " 1)	D36146A2		
			P.B. COMP. LOC. (" " 1)	D36147A2		
			P.B. DRILLING. (" " 1)	D36148A4		
			P.B. WIRING (" " 2)	D36149A3	P.B. WIRING	EARTH PLANE (BD. Nº2) D37415 A3
			P.B. DRILLING (" " 2)	D36150A4		
			P.B. WIRING (" " 3)	D36151A2		
			P.B. " , COMP. SIDE (" " 3)	D36152A2		
			P.B. COMP. LOC. (" " 3)	D36153A3		
			P.B. DRILLING (" " 3)	D36154A4		
			LABEL	D36465A4		
			LABEL	D36466A4		
			CODES AND FREQUENCIES	DSK 16262 A3		
			FURTHER INFORMATION REQUIRED FOR MANUFACTURE			
			UNIT ASSEMBLY INFORMATION	EA10484		
			" WIRING INFORMATION	EA10137		
			" " "	EA10139		
			" " "	EA10140		
			" " "	D23478A4		
			" " "	D32105A4		
			" " "	D32215A4		
			" " "	D33243A4		
			INDUCTORS	14B/301, 14B/302		
				14B/303, 14B/304		
				L/12017		
			LABEL	D32193A4-CP		
			SPEC: EO/053/507			
1	1	*	CHASSIS, CH1/68 MODIFIED AS FOLLOWS :-			
			BOX, DRILLED TO			D36144A1 DET 1
			REAR LID			" " 2
2	1		SCREENING BOX, (EACH INCLUDING 10-BBA BRASS HANK RIVET BUSHES. BBC REF 1-31203-108)			D36144A1 DET 3
3	1		" " LID			" " 4
4	1		BRACKET			" " 5
5	1		MOUNTING PLATE			" " 6
6	1		LABEL, D32193A4 CP DET 1, ENGRAVED TO			" " 7
7	1		" " " 1 " "			" " 8
8	1		" " " 3 " "			" " 9
9	1		" " " 3 " "			" " 10
10	1		" " " 3 " "			" " 11
11	1		" " " 3 " "			" " 12
12	1	*	LABEL (OZAKLING)			D36465A4

BBC

DS/PLA4

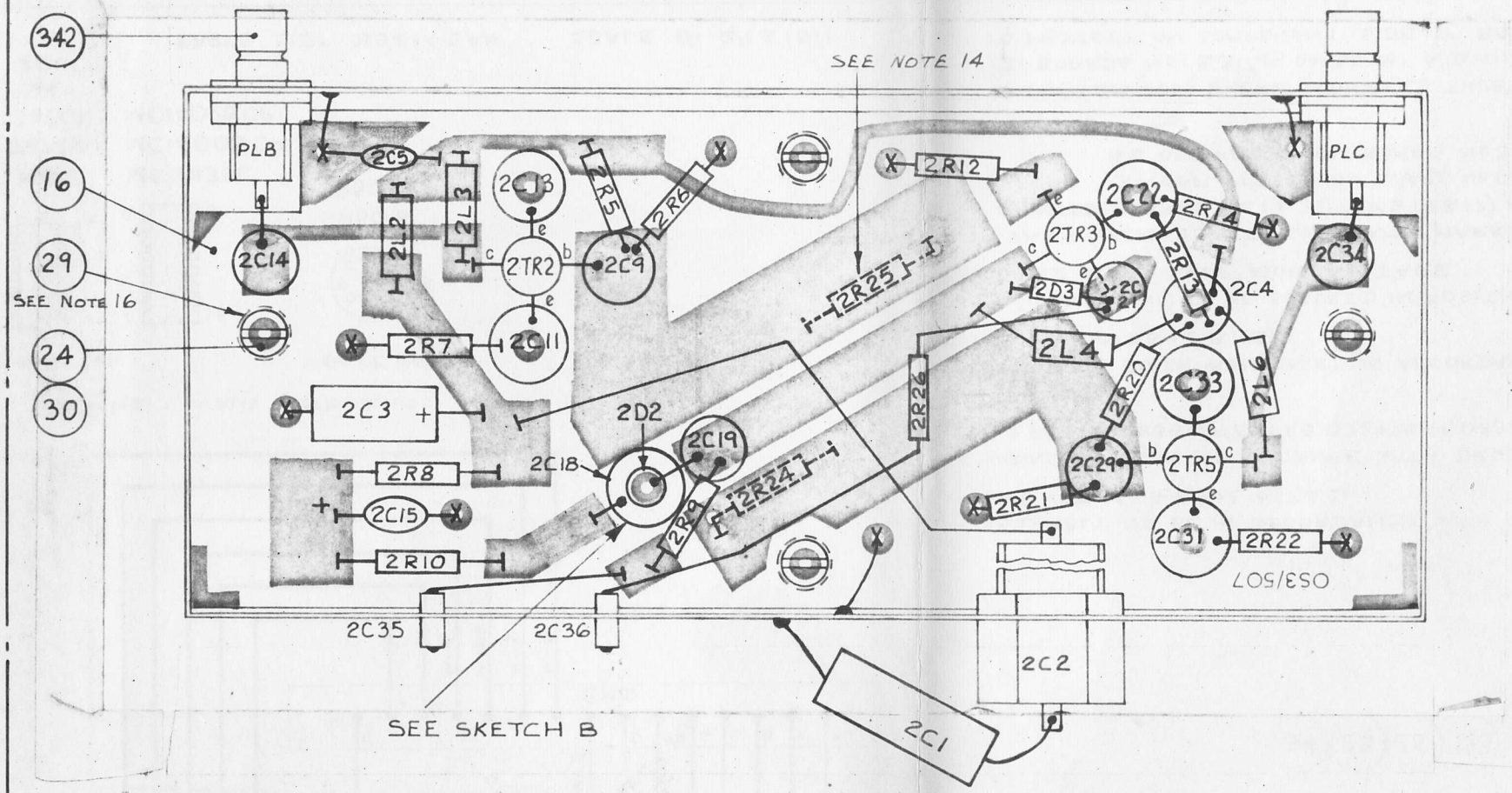
053/507
OSCILLATOR, VARIABLE FREQENCY
PARTS LIST

DRN.	L.M.
TPD.	
CKD.	
APPD.	M.T.E

DESINGS DEPARTMENT

D36142A4

SHEET 1 OF 19 SHEETS

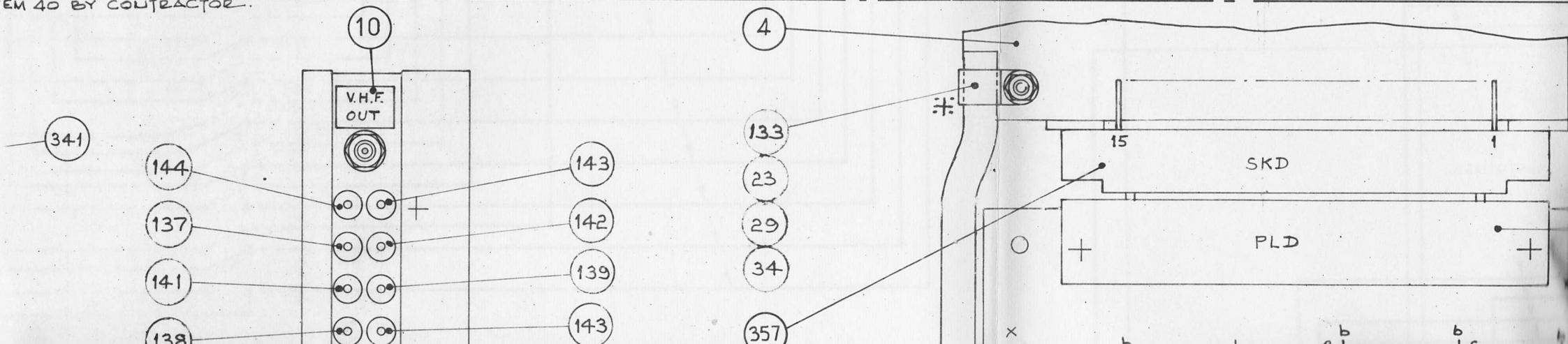


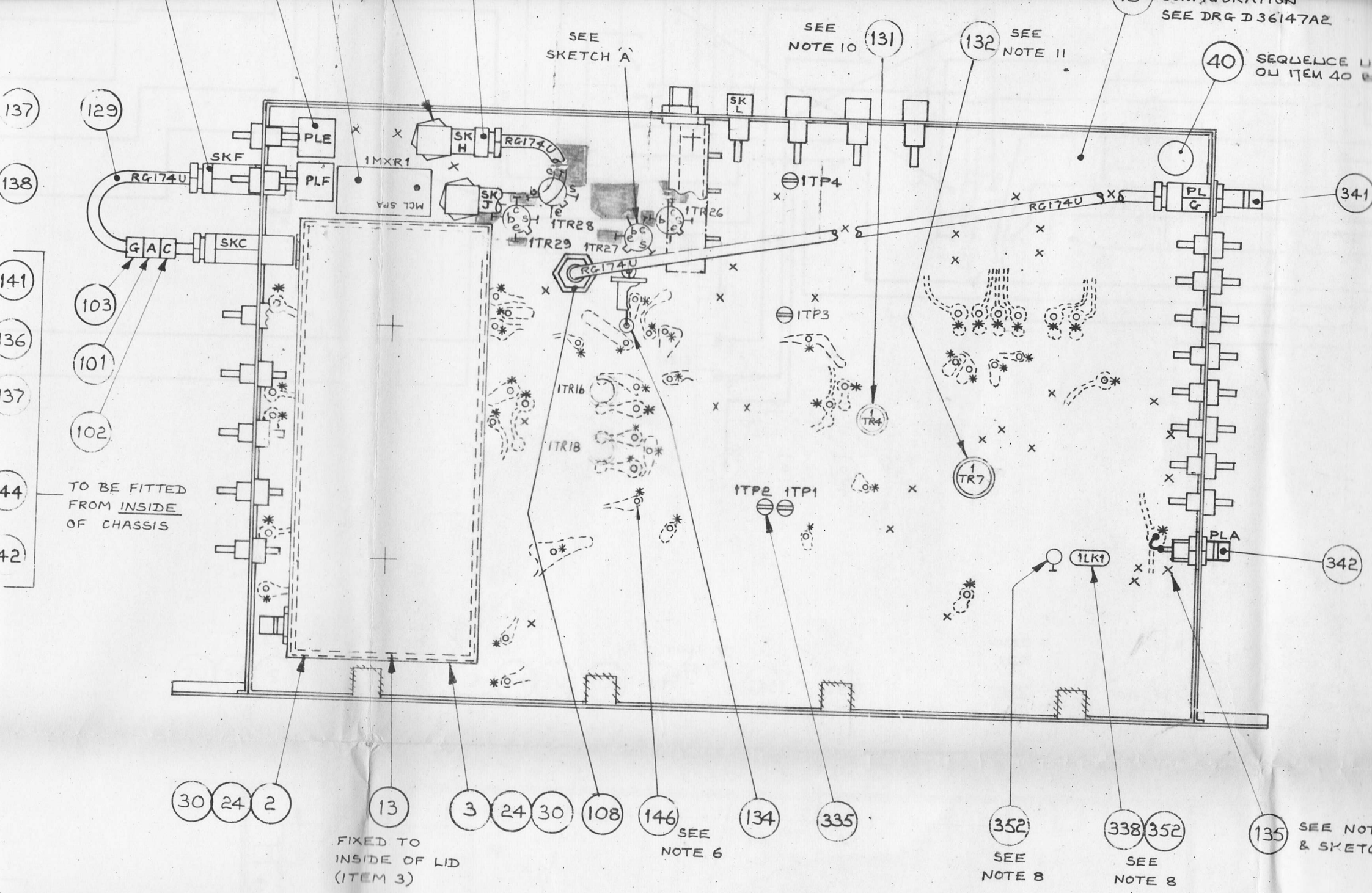
ASSEMBLY OF SCREENING BOX (2 x FULL SIZE)

...T

7A2

...ELICE NO. 2 TO BE MARKED
...EM 40 BY CONTRACTOR.




SEE SKETCH 'A'
SEE NOTE 10
131
132
SEE NOTE 11
SEE DRG D36147A2
40
SEQUENCE
ON ITEM 40
137
129
138
PLE
SKF
PLF
1MXR1
SK H
SK J
SK L
RG174U
1TP4
1TR26
1TR28
1TR29
1TR27
341
PL G
G A C
SKC
103
101
102
141
136
137
1TP3
1TR16
1TR18
1TR4
1TR7
1TP2
1TP1
144
TO BE FITTED FROM INSIDE OF CHASSIS
142
PLA
342
1LK1
30 24 2
13
FIXED TO INSIDE OF LID (ITEM 3)
3 24 30 108
146
SEE NOTE 6
134
335
352
SEE NOTE 8
338 352
SEE NOTE 8
135
SEE NOT
& SKET

DS/A4

BBC

All dimensions in millimetres unless otherwise stated
Normal tolerences
no decimal place ±1 mm
one decimal place ±0.3mm
two decimal places ±0.1mm
unless otherwise stated

THIRD ANGLE PROJECTION

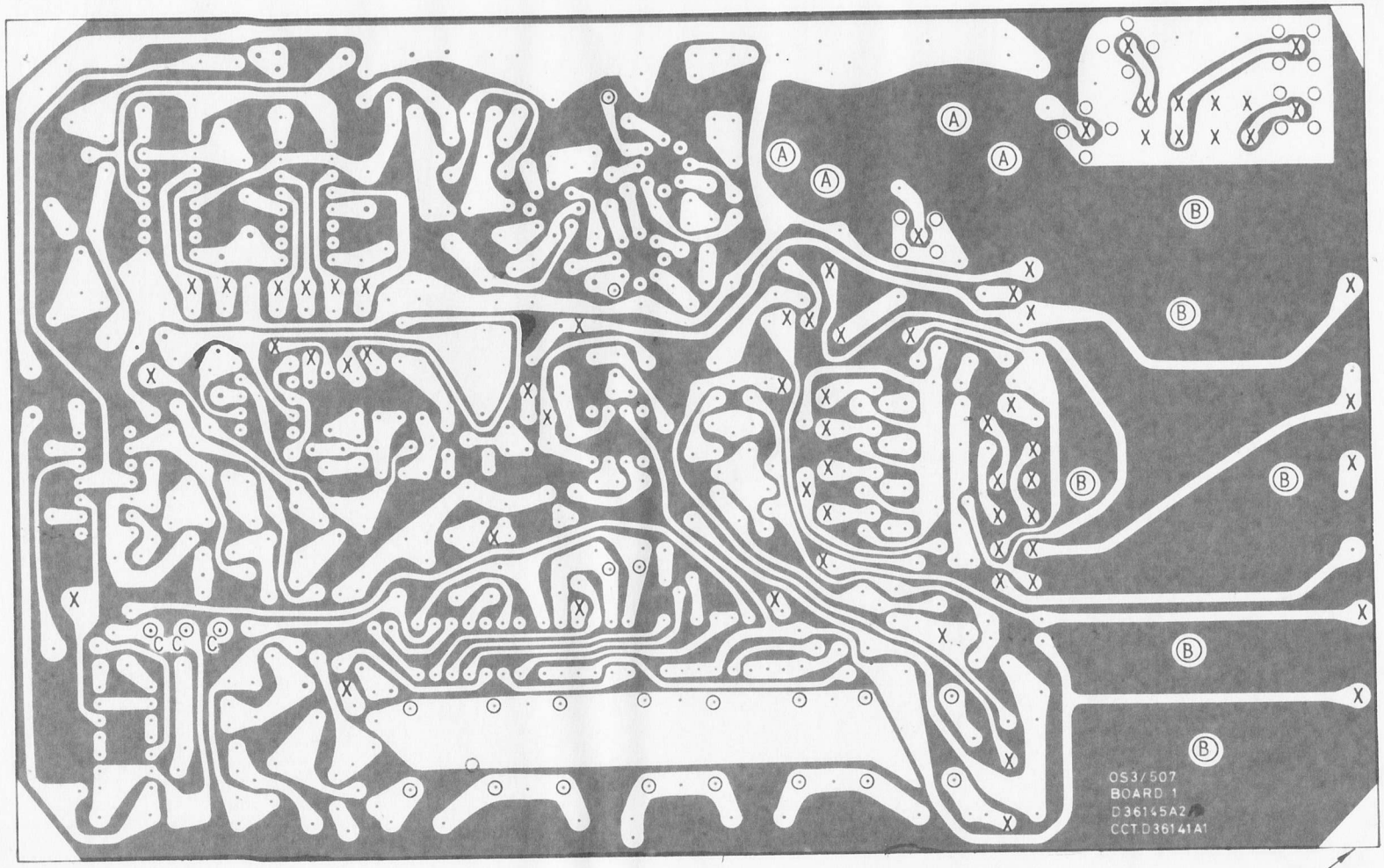
Original Frame Size 190mm × 277mm

D 36148 A4

OS3/507

CHANGE	ISS
REDRAWN TO C.F. 11773 (2) B.W.M. 11-4-75	3

SCALE 1:1



HOLE REF	DRILL No.	DEC Ø	MM Ø
A	12	·189	4·8
B	37	·104	2·65
C	43	·089	2·3
○	52	·0635	1·6
⊙	55	·052	1·3
X	60	·040	1·0
UN CODED	——	——	0·85

APPROXIMATE No. OF HOLES 664

CUT BOARD TO EDGE OF COPPER

MATERIAL: 1·5 MM THICK BAKELITE XYLONITE LTD. SHEET TYPE H76FR/1/1 CLAD ON BOTH SIDES WITH COPPER 35 MICRONS THICK

FINISH: TINNED

MANUFACTURED TO: D36145 A2, D36146 A2, D36147 A2

APPD | CKD | TCD | DRN | BWM

EQUIPMENT DEPATMENT

OS3/507
PRINTED BOARD NO.1
DRILLING

D 36148 A4

DS/A4

BBC

OS3/507 PRINTED BOARD DRILLING (BOARD No, 2)

D 36150 A4

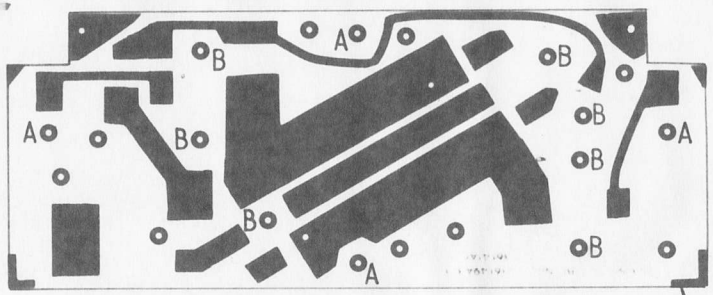
CHANGE	ISS
REDRAWN TO C.F. 11650(1) B.W.M. 20·5·75	3

OS3/507 PRINTED BOARD DRILLING (BOARD No 2)

DRN.	BWM
TCD.	
CKD.	J.H.
APPD.	

EQUIPMENT DEPARTMENT

D 36150 A4



CUT BOARD TO EDGE OF COPPER

HOLE REF	DRILL No, OR SIZE	DIAMETER DEC	DIAMETER MM
A	37	·104	2·65
B	13/64	·203	5·2
UN-CODED	60	·040	1·0

MATERIAL: 1·5 MM THICK MICA & MICANITE LTD SHEET TYPE MG5/2/2 CLAD ON BOTH SIDES WITH COPPER 70MICRONS THICK

FINISH: TINNED

MANUFACTURED: TO D36149 A3 D37415 A3

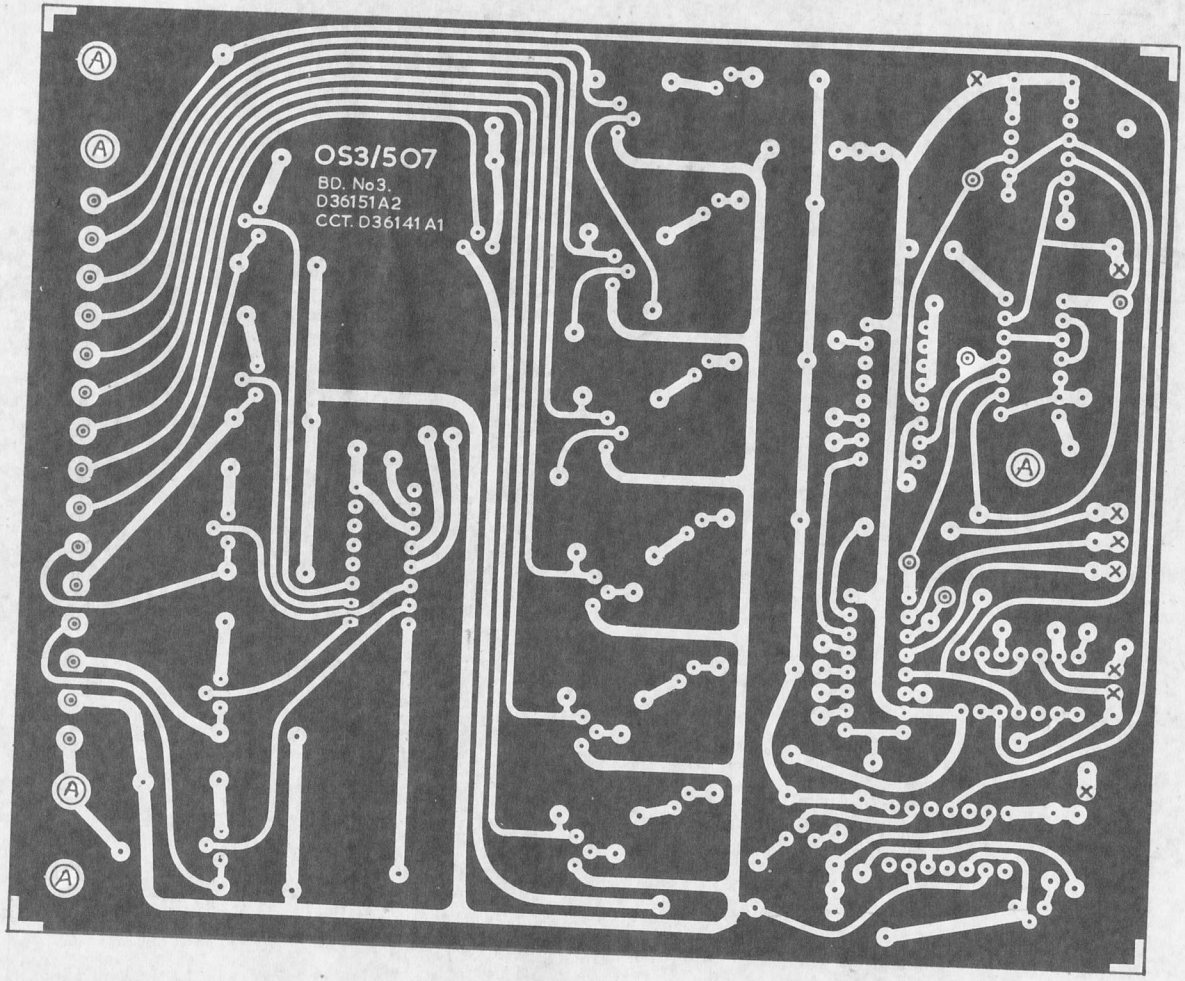
No, OF HOLES: 23

SCALE : 1:1

OS3/507 PRINTED BOARD DRILLING (BOARD No 3)

D36154A4

CHANGE	ISS
12-3-74	1
NO. OF HOLES ADDED. E.I. 22.3.74	2



HOLE REF	DRILL NO OR SIZE	DIAMETER DEC	DIAMETER MM
A	27	·144	3·7
⊙	55	·052	1·3
X	60	·040	1·0
UN-LETTERED	—	—	0·85

APPROXIMATE NO. OF HOLES 297.

CUT BOARD TO EDGE OF COPPER. SCALE 1:1

MATERIAL : 1·5MM THICK BAKELITE XYLONITE LTD. SHEET TYPE H76FR/1/1 CLAD ON BOTH SIDES WITH COPPER 35 MICRONS THICK.

FINISH : TINNED.

MANUFACTURED TO D36151A2, D36152A2 D36153A3

OS3/507 PRINTED BOARD DRILLING (BOARD No3)

DRN

TCD

CKD

APPD

TITLE

DESIGNS DEPARTMENT

D36154A4

TYPICAL VCO CONTROL VOLTAGE (BLUE PIN)	Volts Relative to Earth (±2V)	+10	+10	+10	+5			
DECODER OUTPUT	Pulling Down PLD	7	7	7	4			
	3TR — ON	17	17	17	14			
OUTPUT CODE	PLD 9 LSB	0	0	0	0			
	PLD10	0	0	0	0			
	PLD11	0	0	0	0			
	PLD12	0	0	0	1			
	PLD13	0	0	0	1			
	PLD14 MSB	0	0	0	0			
INTERMEDIATE CODE	A1 LSB	1	1	1	1			
	3TP1	1	1	1	0			
	3TP2	1	1	1	0			
	3TP3	1	1	1	0			
	3TP4	1	1	1	0			
	3TP5 MSB	1	1	1	0			
UNITS CODE SWITCH OUTPUT	LSB	0	0		0			
		0	1		1			
		0	0		0			
	MSB	1	0		1			
TENS CODE SWITCH OUTPUT	LSB	0	0		0			
		1	1		0			
		0	0		1			
	MSB	0	0		0			
DIVISION RATIO OF PROGRAMMABLE DIVIDER	N	1	2		25			
FREQUENCY AT INPUT OF PROGRAMMABLE DIVIDER	MHz	0.5	1.0		12.5			
VHF OUTPUT FREQUENCY	MHz	8	16		200			
OUTPUT FREQUENCY	MHz	908	916		110			
CHANNEL NO.	Code Switch Indication	21	22		45			

Original Frame Size
277mm × 400mm

BBC
DS/A3

CHANGE	ISS

THIRD ANGLE PROJECTION

All dimensions in millimetres unless otherwise stated:

Normal tolerances

no decimal place:–	±1 mm
one decimal place:–	±0.3mm
two decimal places:–	±0.1mm

unless otherwise stated

CODES AND FREQUENCIES IN OS3/507 (PART I)

DRN.	TCD.	CKD.	APPD.
	BMB	VTE	VTE

DESIGNS DEPARTMENT

DSK16262A3

ALE:-