DRAFT

Designs Department Manufacturing Information

No. 5.400(81)

I.F Amplifier AM21/506

Written By: A.R. Lewis

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I.F. Amplifier AM21/506

PRODUCTION TEST SHCEDULE

1. DESCRIPTION

The AM21/506 I.F. amplifier was designed as part of the TM4M/503 UHF TV transposer. It is one of the transposers' three active modules and contains the input mixer, variable-gain i.f. amplifier, i.f. filter and output mixer. It is possible to control the tilt of the frequency response of the unit with an external voltage. The vision carrier i.f. is 40.75MHz with the sound carrier i.f. at 34.75MHz.

2. INFORMATION

2.1 Designed in RF Section (5), Designs Department

2.2. Designer and Engineer responsible, A.R. Lewis

2.3 Handbook: part of D.D. Handbook No. 5.156(81)

2.4 No technical instruction available

2.5 Pre-production batch of 8 tested at D.D.

3. MANUFACTURING PERFORMANCE SPECIFICATION

3.1 Input requirements

RF inputs	PLD	Input signal, -45to -15dBm, 470 - 860MHz
	SKK	Down-mix local oscillator, +10dBm, input vision frequency +40.75MHz ±output offset
	SKL	Up-mix local oscillator, +10dBm required output vision frequency (without offset) +40.75MHz
AGC input	C1	0 - 28 volt, 15 volts for 30dB gain reduction 4 volts for 3dB gain reduction
Slope control input	C2	0 - 15 volts, 3 volts for +2.5dB slope 9 volts for -2.5dB slope 5.6 volts (nom) for flat response

3.2 Outputs

RF outputs	PLE	UHF output, -19dBm, 470 - 860MHz
	SKJ	Vision carrier, -3dBm nom, 40.75MHz
15V output	C4	15 ± .05V, 680mA max.

3.3 Power Supply

	C3	28V, 170±20mA plus current drain from '15V output'

3.4 Performance

Conversion gain	30 ±3dB at maximum gain setting (0V on AGC input).
Gain control range	45dB min
Input return loss	>16dB
Output retrun loss	>16dB
Frequency response	<0.5dB p-p ripple in 8MHz channel (slope corrector set for flat response).
Total slope corrector range	±2.5dB min; from vision frequency to colour subcarrier frequency.

4. WARNINGS

4.1 There are normally no voltages in excess of 50V d.c. or 30V r.m.s a.c. in this unit.

4.2 3TR3, 4, 5 and 8 are MOS devices and should be handled with care.

5. TEST APPARATUS REQUIRED

Power supply (28V, 500mA)

DVM (.01%)

100Ω 9W resistor (0001217)

100Ω MR25 (0099007)

Signal generator, 510 to 910MHz, +10dBm e.g. HP8640B

Spectrum analyzer and tracking generator - 1GHz

Directional coupler (450 - 900MHz)

10dB, 50Ω attenuator

1kΩ MR25 (0099082)

5kΩ potentiometer, multi-turn

51pF 2% polystyrene capacitor

6. INSPECTION CHECKS

6.1 Inspect the unit for any mechanical defects. Check that it has been manufactured correctly to D 50012 A1.

6.2 Inspect the unit for any wiring defects and check that it has been wired correctly to D 50011 A1.

6.3 Check the polarity of the following:-

6.3.1 MXR101, MXR102, MXR210, MXR202

6.3.2 TR301 - 311

6.3.3 D301 - 309

6.3.4 IC301 - 304

6.3.5 C303, 345, 348, 380, 381, 385

6.3.6 R330, 333, 345, 346

7. TEST PROCEDURE

7.1 15volt regulator

Connect a source of 28V (500mA max) to C3. Monitor the voltage at TP308 with a DVM.

Adjust R374 for a DVM reading of approximately 15volts. The current drawin from the 28V supply should be 170mA approx.

Connect a 100Ω 9W resistor between TP308 and ground and adjust R374 for a DVM reading of 15.00 $\pm$0.03 volts.

7.2 Input mixer (Board 1)

Disconnect the four lead-outs of L105 from board 3 and connect them as follows: slate to ground, blue to geen, yellow to ground via a 100Ω MR25. Connect the signal generator set to give +10dBm at 510MHz to SKK.

Connect the tracking generator output set to -20dBm via the dicrectional coupler to PLD. Use the spectrum analyzer to measure the return loss at a frequency approximately 40MHz lower than the frequency at SKK which is visible as a 'birdie' on the trace. Swing the signal generator frequency between 500 and 900MHz. Adjust 106 and C107 for optimum input return loss.

This input return loss figure may be difficult to meet if the inner connection of the coaxial cable to the board is not kept as short as possible. The lead lengths of the 3dB couplers and R105, R106 are also critical and should be kept very short. If C101 or C108 is damaged in assembly or poorly fitted this could also cause a poor input return loss. If there is any doubt about the mixers then check the conversion loss of the unit which sould be <10dB.

7.3 <u>Output mixer (Board 2)</u>

Repeat the tests of 7.2 on board 2 but not that the signal generator is connected to SKL and return loss at PLE is to be measured. All component references are increased by 100 e.g. for L105 read L205.

7.4 <u>Input amplifier and AGC stage (Board 3)</u>

The connections from L105 to board 3 should be disconnected. LK301 and LK304 should be open-circuit. Connect the tracking generator output via a 20dB pad and short coaxial lead to PLM. Set the tracking generator to sweep between 30 and 45MHz at a level of -30dBm at PLM. Connect the open end of C315 via a short (1 metere max) coaxial lead to the spectrum analyzer. Check that the gain is 20 ±4dB. Adjust L332 and, if necessary L304 until the gain peaks at38 ± 2MHz.

The gain at 38MHz should now be 20 ± 2dB.

Connect the live end of C313 to 15volts via a 1kΩ resistor and check that the gain of the amplifier drops to <-10dB. Remove the 1kΩ resistor.

If the gain of the stage is low then check the individual stage gains by using a high impedance probe. TR301 stage has 18dB nominal gain and TR302 stage has 10dB nominal gain. TR303 has a gain of 2dB if the open end of C315 is left open circuit, -8dB if the open end of C315 is terminated in 50Ω. D303 in conjunction with R306 provides AGC action. Insufficient AGC range may indicate either that D303 is faulty or R306 is the wrong value.

7.5 Anti-log amplifier (Board 3)

Use the test set-up of 7.4 but bridge LK304 and connect the live end of C1 to the wiper of a 5kΩ potentiometer. The two ends of the potentiometer should be connected to 0 volts and 28 volts respectively. Monitor the voltage on C1 with a DVM.

With the voltage on C1 at 0 volts check that the gain through the AGC amplifier is as measured in 7.4.
Adjust the potentiometer until the voltage at C1 is 15 ± 0.05 volts. Adjust R333 until the amplifier gain is -10dB.
Adjust the potentiometer until the voltage at C1 is 4.00 ± 0.05 volts. Adjust R330 until the amplifier gain is +17dB. Repeat the setting of R333 and R330 until the gain is -10dB at 15volts and 17dB at 4 volts. Adjust the potentiometer until the voltage at C1 is 24 volts andcheck that the amplfier gain is less than -25dB.

7.6 Slope corrector (Board 3)

Connect a 51pF capacitor between L317, L318, LK303 junction and TP302 (LK302 and LK303 should be open-circuited). Connect the tracking generator output via a 20dB pad and a short (1 metre max) coaxial lead to PLN. Set the tracking generator to sweep between 30 and 50MHz at a level of -30dBm at PLN. Use a high-impedance 2.5k/50Ω probe on the spectrum analyzer and monitor the signal at TP302. Adjust L316 for flattest response in the region 34 to 42MHz. Measure the gain from PLN to TP302.

The frequency response at TP302 should be within 0.2dB of the frequency response at PLN (measured with the probe) in the frequency range 34 to 42MHz. The gain to TP302 should be 2 ± 1dB.

7.7 Output amplifier and buffer (Board 3)

Disconnect the leads from L205 on Board 2 and solder a 100Ω resistor between the open end of C358 and ground. Use the test set-up of 7.6 but monitor the signal across the 100Ω resistor with the probe.

The gain from PLN to the 100Ω resistor should be 20 ± 2dB at 40.75MHz. The gain at 36.3MHz should be 0.5 ± 0.2dB less than the gain at 40.75MHz.

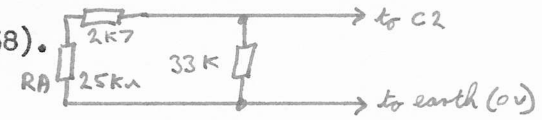
If the gain is too low at 40.75MHz then the turns ratio of L331 may be wrong - the gain of TR306 stage should be 14 ± 1dB. L328, C362, R317 determine the gain at 36.3MHz relative to 40.75MHz.

7.8 Vision carrier extractor

Use the test set up of 7.6 but reduce the input level at PLN to -80dBm and connect the vision carrier output at SKJ directly to the spectrum analyzer. Adjust in turn L322, L323 and L324 fo r maximum output at 40.75MHz. Repeat the adjustment of L322, L323 and L324 if necessary until maximum output is obtained. Increase the signal level at PLN to -60dBm. Check the output level at SKJ. This should be -4dBm.

7.9 Slope corrector driver stage

Use the test arrangement of 7.6 but connect the live end of C2 to the following circuit (which may be found connected to PLA13 in the transposer tester TE1/38).



Monitor the voltage on C2 with a DVM. Remove the 51pF capacitor connected in 7.6 and link across the pins of LK303. Use the high-impedance probe on the spectrum analyzer to display the signal at the output pin (C358). Set RA to maximum resistance and check that the voltage on C2 is 9 ± 0.4volts.

Adjust R346 until the gain through the amplifier is 2.5dB more at 40.75MHz than at 36.3MHz. Readjust RA to maximum resistance and check that the voltage on C2 is 3 ± o.2volts. Adjust R345 until the slope varies between ±2.5dB at 9 and 3 volts.

If there is any difficulty in achieving the required slope of 2.5dB at 3 volts then a slight adjustment of L316 (not more than one turn) may be made with 3 volts on C2. If more than one turn of L316 is required or the correct slope cannot be set at 9 volts there is a fault in the circuit. Check that IC301c output can swing between 3 and 9 volts and IC301d can swing between 2 and 24 volts. There may be a fault with D304, 5, 6 and 7. Check for a faulty component and replace if necessary.

7.10 <u>I.F. filter (Board 3)</u>

Connect a tracking generator with zero sweep width facility to PLM. Disconnect the leads from Board 2. Short together the pins of LK301 and LK302. Temporarily remove C343 and connect the spectrum analyzer input to the junction of L315 and TR304 via a 56nF d.c. isolating capacitor.

Tune L307 until a notch in the frequency response is obtained at 23.5MHz.
Tune L311 until a notch in the frequency response is obtained at 27.78mHZ
Tune L313 until a notch in the frequency response is obtaine at 54.32MHz
Tune L309 until a notch is the freuqnecy response is obtaine d at 62.62MHz

Remove R309. Use a 5kΩ 100:1 probe to monitor the signal at the live endo f C316. Solder a short piece of wire across C322. Adjust L306 until the response peaks at 34.10MHz - use the 1dB per division range on the spectrum analyzer.

Remove the short across C322 and short across C327. Adjust L308 until the notch in the frequency response, observed at C316, is at 38.76MHz.

Connect the tracking generator output to PLN via a 1kΩ series resistor. Use the probe to monitor the signal across C338. Solder a short piece of wire across C333. Adjust L314 until the frequency response peaks at 41.77MHz.

Remove the short across C333 and short across C327. Adjust L312 until the notch in the frequency response, observed at C338, is at 38.54MHz Remove the short across C338. Refit R309.

Connect the spectrum analyzer input to TR304 stage output as previously described. Display the through response at the filter on 1dB per division and adjust L310 for the flattest response. The filter ripple should be <0.5dB p-p in the range 34 to 42MHz. If the response is greater than this then slight adjustment to the tuning coils is allowed to bring the response within the allowed limits. L314 and L306 are likely to be most in error due to the shunting effect of the probe and initial fine adjustment should commence with these coils. Reconnect C343.

7.11 <u>Overall tests</u>

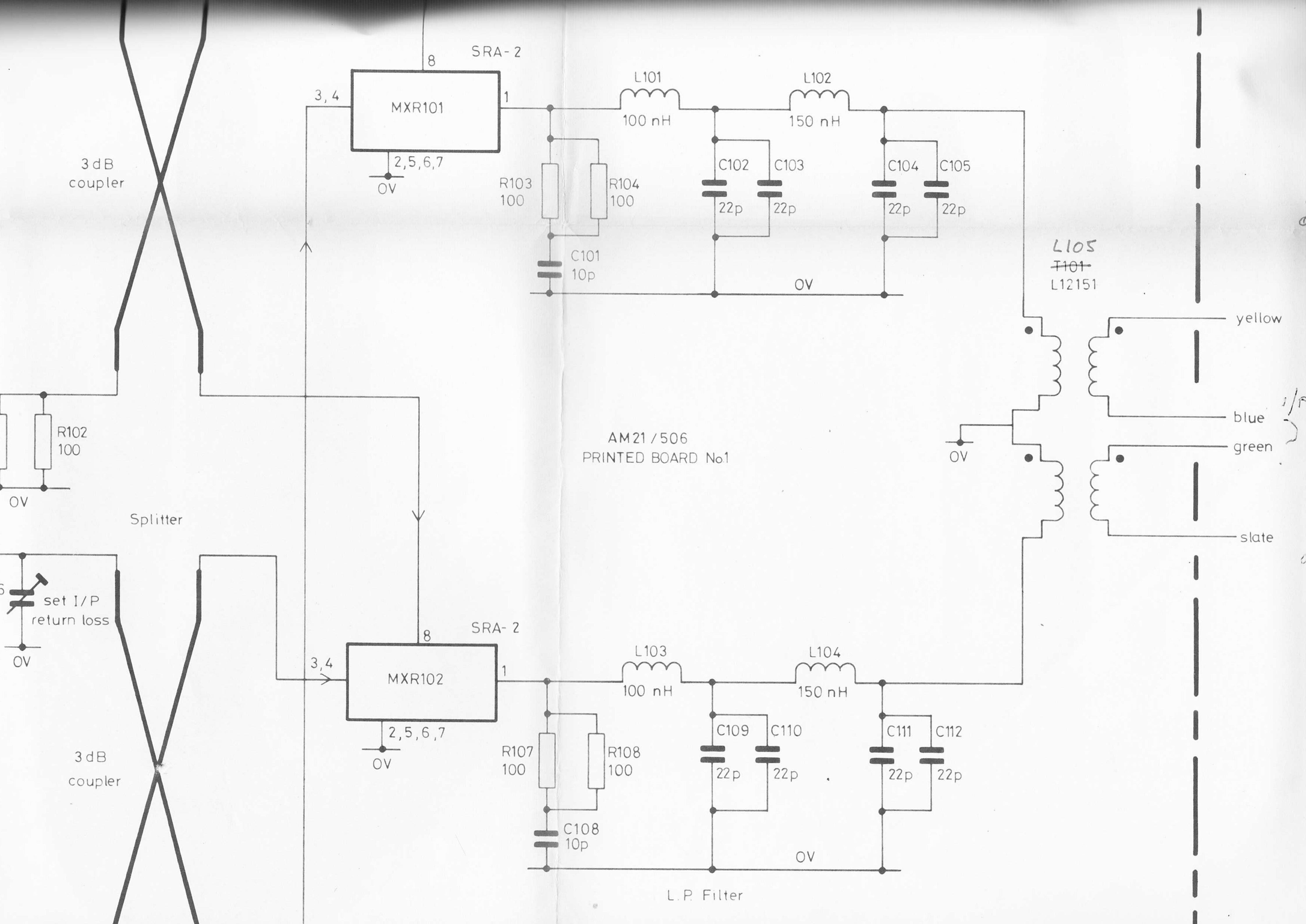
Solder the connections from Board 1 and Board 2 to Board 3 - note that different connections are used at the input and output ends of the card. Connect an oscillator giving +10dBm at 904MHz to SKK. Connect an oscillator giving 10dBm at 800MHz to SKL. Suitable signals can be obtained from an OS3/509. Connect a signal generator giving -50dBm at 864MHz to PLD. Connect the live end of C1 to 0 volts. Monitor the signal at PLE on a spectrum analyzer.

The output at PLE should be a signal at 760MHz at a level of -20dBm ±3dB. If the gain is outside the tolerance figures given then the best way to isolate the faulty part of the circuit is to use a high impedance 5k/50Ω probe and examine the gain to various points of the circuit. The table below nominal figures for gain from PLD to the specified point in the circuit for the conditions described above.

Board 1 output	-8.5dB (conversion gain)
R304, C306, C308 junction	+9.0dB
R304, C310 junction	+18dB
C315, L306 junction	+20dB
L314, C341 junction	+19dB
TP310	+21dB
C353, TR305 junction	+21dB
TP303	+35dB
C358 output end	+38.5dB
Board 2 output	+30dB (overall conversion gain)

Signal levels (rms) in the vision carrier output using 2.5kΩ/50Ω probe are:-

TR306 emitter	
IC302 pin 7	
TP306	
TP307	
output socket SKJ (terminated)	180mV


3dB
coupler
SRA-2
8
3,4
MXR101
1
2,5,6,7
OV
L101
100 nH
L102
150 nH
R103
100
R104
100
C101
10p
C102
22p
C103
22p
C104
22p
C105
22p
OV
L105
T101
L12151
yellow
blue
green
slate
R102
100
OV
Splitter
AM21/506
PRINTED BOARD No1
OV
set I/P
return loss
OV
SRA-2
8
3,4
MXR102
1
2,5,6,7
OV
3dB
coupler
L103
100 nH
L104
150 nH
R107
100
R108
100
C108
10p
C109
22p
C110
22p
C111
22p
C112
22p
OV
L.P. Filter

Δ 50010 A4

CHANGE	ISS.
12-2-81	A

AM21/506 PARTS LIST

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
			DRAWING NUMBERS		
			CIRCUIT (P.B 1 & 2) Δ 50008 A2		
			CIRCUIT (P.B 3) Δ 50009 A1		
			P. LIST Δ 50010 A4		
			ASSY & WIRING Δ 50011 A1		
			DETAILS 1-8 Δ 50012 A1		
			P.B 1 & 2 MASTERS (4 SHEETS) Δ 50013 A2		
			P.B 1 & 2 ASSY INFORMATION Δ 50014 A2		
			P.B 1 & 2 DRILLING Δ 50015 A3		
			P.B 3 MASTERS (4 SHEETS) Δ 50016 A2		
			P.B 3 COMP LOC Δ 50017 A2		
			P.B 3 DRILLING Δ 50018 A3		
			LABEL LEGEND Δ 50019 A4		
			SCREEN ETCHING MASTER Δ 50020 A2		
			FURTHER INFORMATION REQUIRED FOR MANUFACTURE:		
			ASSEMBLY INFORMATION E.A 10484		
			WIRING INFORMATION EA 10137, E.A 10140		
			COUPLER TUBE Δ 49983 A4-CP		
			ETCHED BRACKET Δ 49981 A2-CP		
1	1		LARGE EXTRUSION		Δ 50012 A1 DET 1
2	2		SMALL "		" " 2
3	2		SMALL COVER		" " 3
4	1		LARGE "		" " 4
5	2		END PLATE		" " 5
6	2		DIVIDING PLATE		" " 6
7	4		TIE ROD		" " 7
8	1		SPACER		" " 8
9					
10					
11					
12	2		P. BOARD (SEE NOTE BELOW)	TO	Δ 50013 A2 (4 SHEETS)
					Δ 50015
			THE QUANTITY SPECIFIED (I.E 2) GIVES 2		
			IDENTICAL BOARDS (P.B 1 & P.B 2).		
13	1		P. BOARD No 3	TO	Δ 50016 A2 (4 SHEETS)
					Δ 50017 A2, Δ 50018
14	4		COUPLER TUBE		Δ 49983 A4-CP
15	1		LABEL (CODE & TITLE)		Δ 50019 A4
16					
17					
18					
19					

13

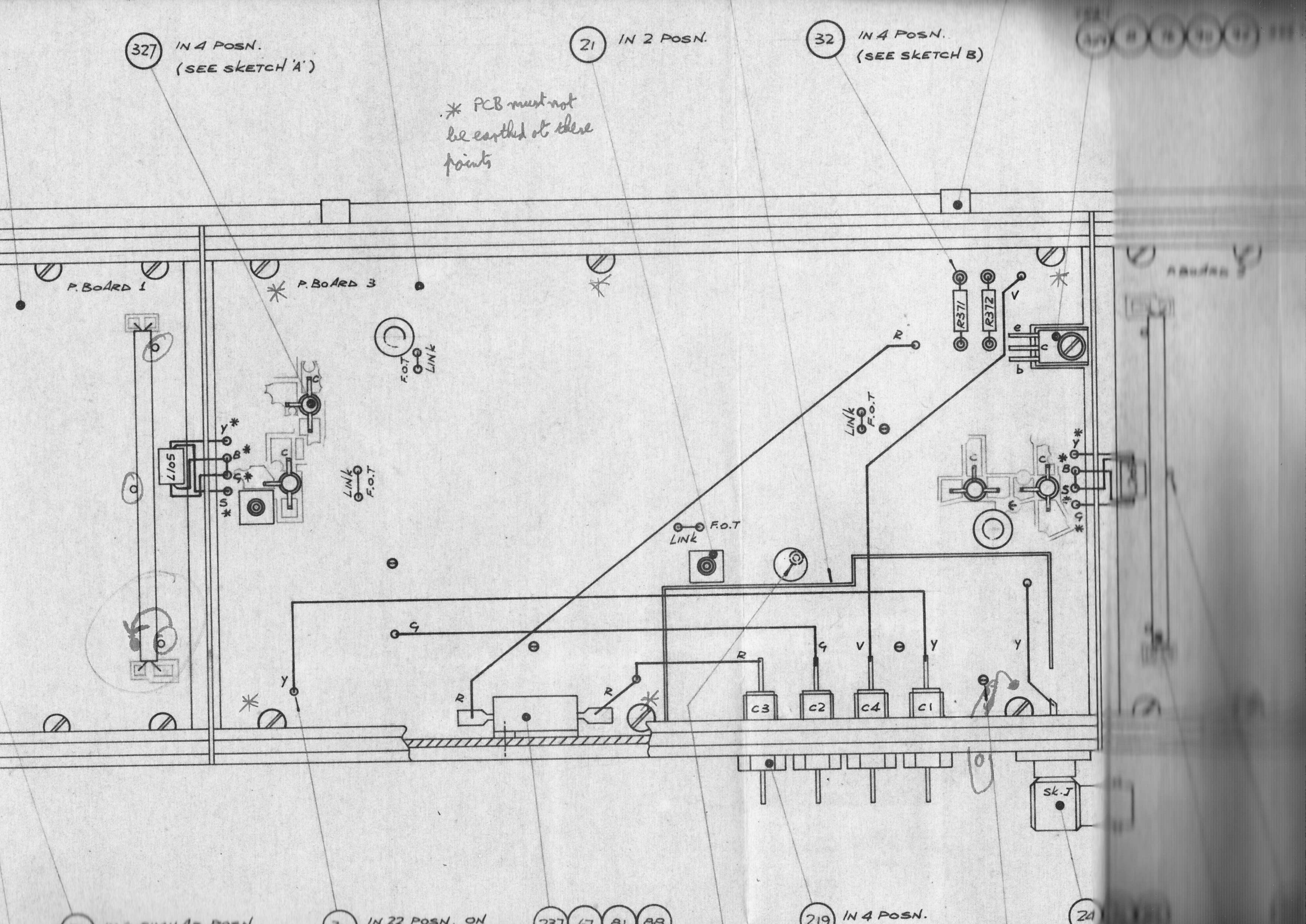
UNAPPROVED

BBC

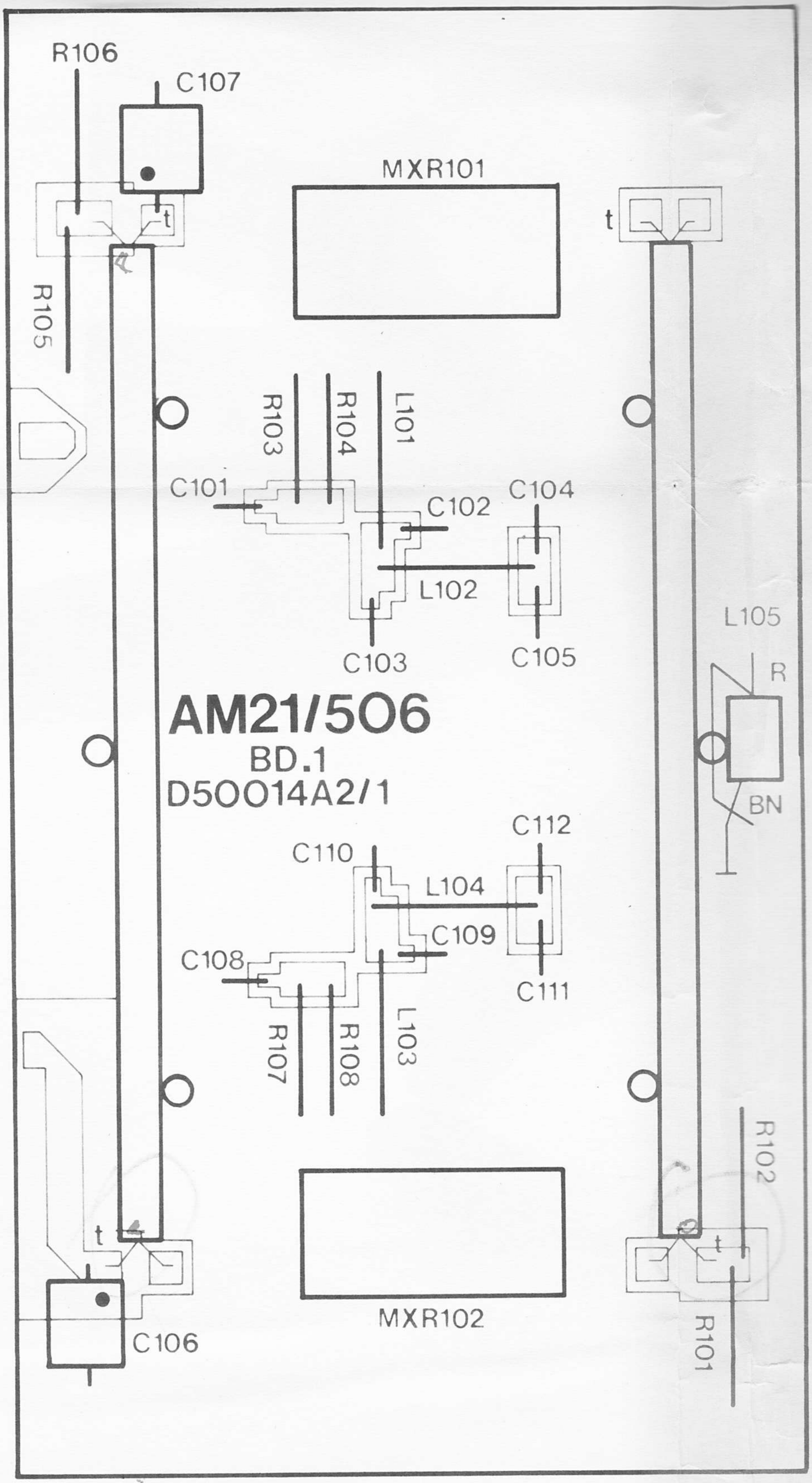
DS/PLA4

AM21/506 PARTS LIST
I.F AMPLIFIER

DRN.	K. TURNER	DESIGNS DEPARTMENT
TPD.		
CKD.		Δ 50010 A4
APPD.		SHEET 1 OF 15 SHEETS



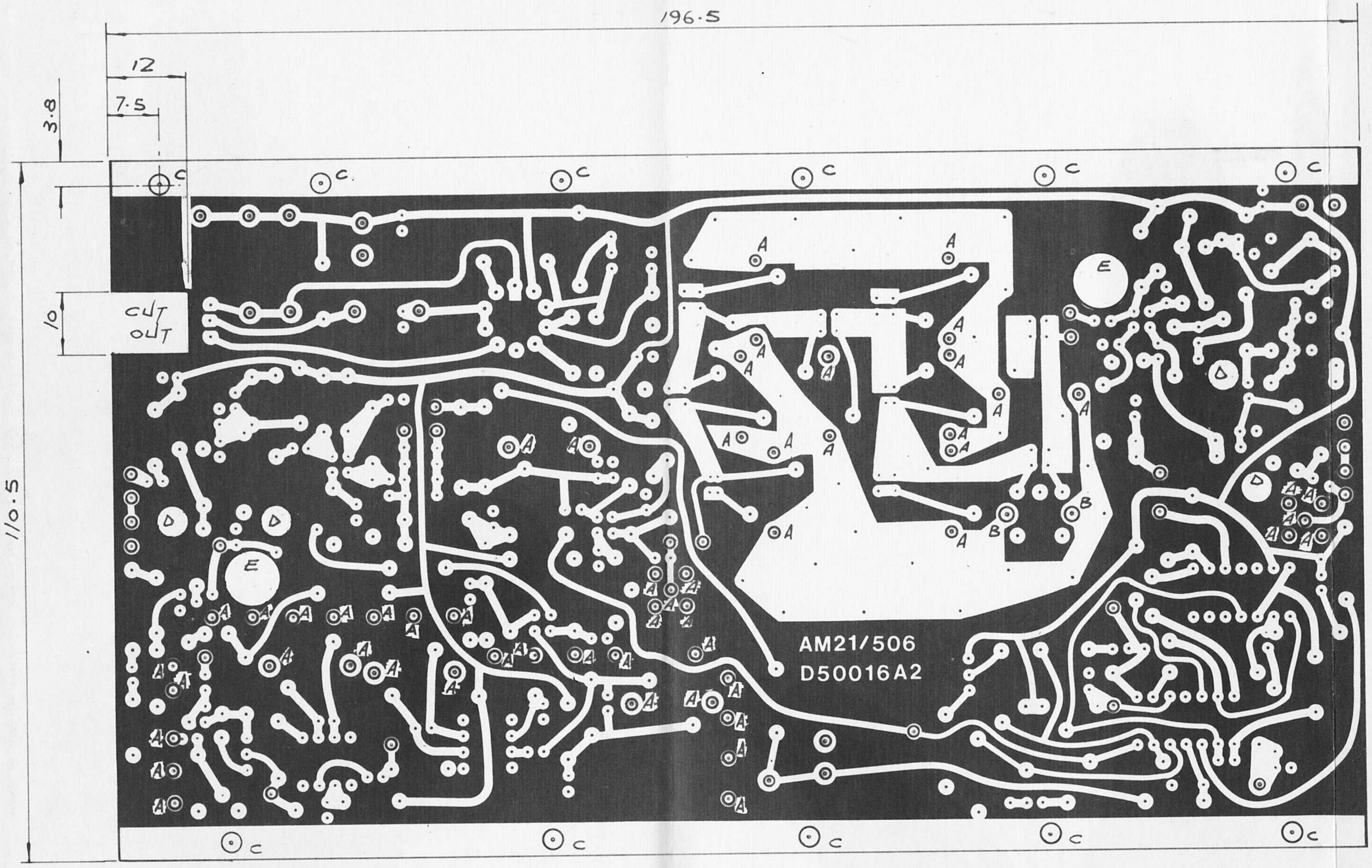
327 IN 4 POSN. (SEE SKETCH 'A')
21 IN 2 POSN.
32 IN 4 POSN. (SEE SKETCH B)
* PCB must not be earthed at these points
P. BOARD 1
P. BOARD 3
L105
R371
R372
F.O.T
LINK
C3
C2
C4
C1
SK. J
219 IN 4 POSN.
24
IN 22 POSN. ON



mponent lead-outs to be cut as short as possible.

mic chip capacitors (C101,102,103,104,105,108,109,110,111,112,201,202,203,204,205,208,209,210,211,212)
g tweezers mount chip capacitors equally across gap in copper track.
d excesive heat - solder quickly. Use only a low melting point solder to DIN 1707 and
nperature controlled soldering iron of 370° nominal.

t where stated otherwise, bend leads of all components as shown in sketch 'A' and
er to printed board copper track.



HOLE SIZE
...R 1·4 DIA
...R 2·0 DIA
...R 3·4 DIA
...R 5·0 DIA
...R 9·0 DIA

MATERIAL 1·6 THK. TO BS 4584, + CLS·2, EP-GC-CU-3 35/35, 1·6 ± 0·20 (EPOXIDE WOVEN GLASS FABRI... CLAD ON ~~ONE~~/BOTH SIDES WITH 35μm THK. COPPER).

MANUFACTURED TO D50016A2 (4 SHEETS), D50017A2

L/12151

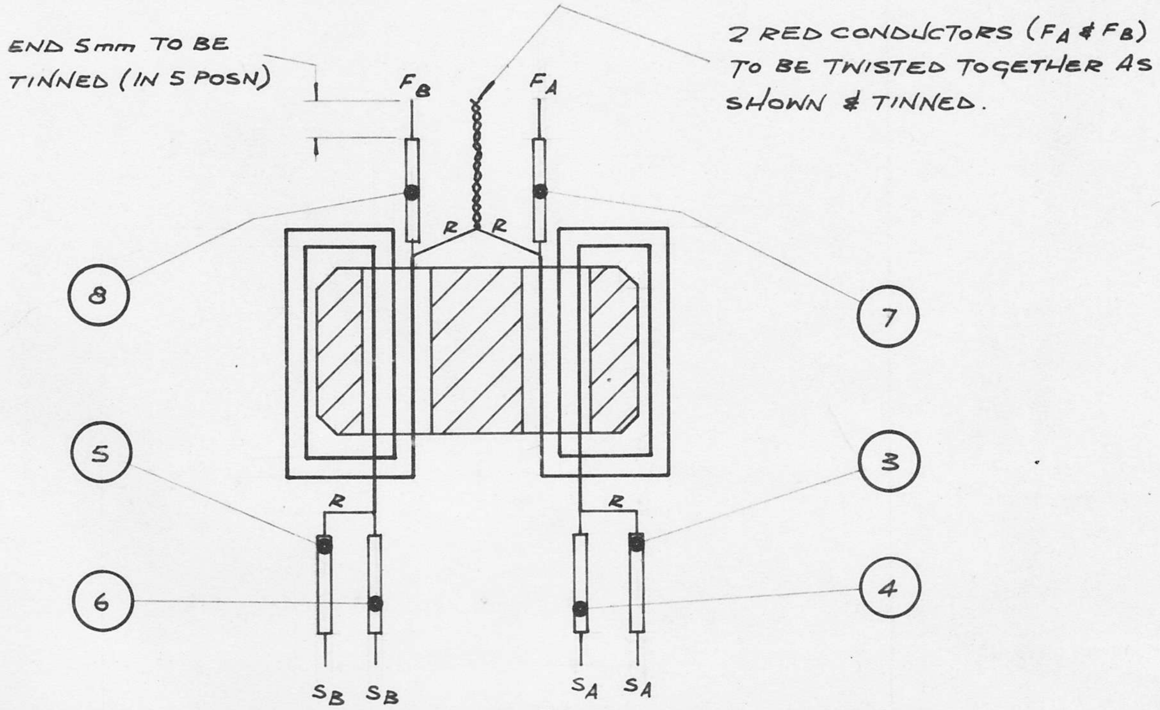
ISS	CHANGE
1	FIRST USED ON AM21/506 7-1-81

ROTATION

Y Z

THIRD ANGLE PROJECTION

SCALE N.T.S



Inductor to be manufactured in accordance with E13127A4 notes 1, 3, 4b, 8 & 9

ITEM No	No OFF	see note	DESCRIPTION	BBC REF OR DRG No
1	1		CORE, MULLARD TYPE FX 2049	
2	AR		WIRE, 36 SWG, BIFILAR (RED/GOLD)	
3	1		SLEEVE, INSUL, 0.5 BORE x 20LG, SYMEL BROWN	
4	1		" " " " " SLATE	
5	1		" " " " " RED	
6	1		" " " " " YELLOW	
7	1		" " " " " GREEN	
8	1		" " " " " BLUE	

* DENOTES ITEMS SUPPLIED ON EMBODIMENT LOAN TO THE CONTRACTOR BY THE B.B.C. FREE OF CHARGE

WINDING DETAILS

WDG	WIRE	TURNS	START	FINISH	TAP	ROTATION	SPECIAL REQUIREMENTS
A	ITEM 2	2¼		AS DRAWN			
B	"	2¼		"			

TEST INFORMATION

WDG	INDUCTANCE 'L' MIN± H	MAX (WITH CORE) ± H	RE (MIN L)	SPECIAL TEST REQUIREMENTS
A				
B				
C				

DATA SHEET

BBC

VM182A4

DATA SHEET

UNAPPROVED

DRN:
TCD
CKD
APPD

DESIGNS DEPT.

L/12151