Issue 1
30.3.82

Designs Department Manufacturing Information

No. 5.393(81)

UHF Power Amplifier AM14/561

.....
(G.G. Johnstone)
for Head of Designs Department

Written by: M.T. Ellen
N. Taylor

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BBC

DS/SPA4

VS

Issue 1
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No. 5.393(81)

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Designs Department Manufacturing Information

No. 5.393(81)

UHF Power Amplifier AM14/561

PRODUCTION TEST SCHEDULE

1. DESCRIPTION

This is a broadband, high gain amplifier with a directional coupler and AGC circuit to regulate its output power. It was designed as part of the UHF TV Transposer TM4M/503. The gain of the amplifier is fixed and its output power is regulated by using the AGC output to drive the PIN diode attenuator in an IF amlifier AM21/506. The AGC reference voltage, which determines the output power, is derived from an external potentiometer and an output is provided for an external LED to indicate that the power is normal, (i.e. that the output power is being limited by the action of the AGC). The range of the AGC output voltage is limited to a value determined by a second external potentiometer, in order to limit the overall transposer gain. Both potentiometers and the LED are earthed at one end.

The unit is housed in an extruded aluminium box with two compartments and two snap-on lids. The amplifier consists of an Engelbrecht hybrid stage giving 25dB gain in one compartment followed by two single ended transistor stages and an Engelbrecht transistor stage in the other compartment. The second compartment also has the AGC circuit, mounted on a separate PCB.

2. INFORMATION

2.1 Design Section - Radio Frequency

2.2 Designers - M.T. Ellen and R.J. Hart

2.3 Engineer Responsible - M.T. Ellen

2.4 Handbook - Part of the UHF TV Transposer TM4M/502 Handbook No. 5.156(81).

2.5 Technical Instruction - Not available 1st January 1981.

2.6 Pre-production Batch - This Production Test Schedule has been tested on a pre-production batch in Designs Department

3. MANUFACTURING PERFORMANCE SPECIFICATION

3.1 Input Requirements

3.1.1 UHF signals between 10 and 1000MHz at levels up to -20dBm.

3.1.2 Maximum gain control resistors switchable between 20kΩ fixed and 50kΩ variable connected between C4 and earth (part of TE1/38).

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3.1.3 Output power control resistors switchable between 16kΩ fixed and 250kΩ variable connected between C3 and earth (part of TE1/38).

3.2 Outputs

3.2.1 UHF signal with a level up to +33dBm between 470 and 860MHz

3.2.2 DC signal from 3 to 25 volts (at least) to control the level of the UHF input to the amplifier, in order to regulate its output power.

3.2.3 Current output of +10mA to drive 'power normal' LED (cathode earthed).

3.3 Power Supply

+28 ±0.5 volts at 1.5 ±0.1 amps.

3.4 Performance

Gain of input stage IC101 and IC102:- 25 ±2dB.
Gain of driver stages TR201 and TR202:- 20 ±1dB.
Gain of output stage TR203 and TR204:- 9 ±1dB.
Overall gain:- 54 ±3dB mean, with ±1dB gain variation from 470 to 860MHz
Input return loss:- ≥16dB.
3-tone intermodulation at +33dBm:- ≤-53dB
Vision to sound crossmodulation at +33dBm:- ≤9%.
Output return loss:- ≥12dB.
Output power AGC range:- ≤+23 to ≥+34dBm.
Value of resistor connected to C3 for +33dBm output:- 16kΩ.
AGC output polarity - low voltage for high gain.
AGC output voltage limiting - +3 to +26 volts. (The resistor connected to C4 sets the lower voltage limit).

4. WARNING

4.1 UHF power transistors TR201, 202, 203 and 204 contain beryllium.

4.2 No voltages above 50 volts dc or 30 volts ac are connected to this unit.

4.3 The UHF output (PLG) must be terminated when power is applied, see handbook No. 5.156(81) for further information.

5. TEST APPARATUS REQUIRED

Power supplier, adjustable 0 to 28 volts and 0 to 2 amp current limit.
Spectrum Analyser, 10 to 1200MHz (with storage normaliser if possible).
Tracking Generator, 10 to 1200MHz.
Power Meter.
UHF 3-tone Generator 470 to 860MHz with IP ≤-70dB.
Variable Attenuator, 0 to 40dB in 1dB steps or less.
Attenuator, 30dB, 5 watt, 50Ω (calibrated to ±0.1dB accuracy).
Precision Attenuator, 10dB, 250mW, 50Ω.
Coupler, 20dB, 50Ω.
DVM.
PIN Diode Attenuator test jig to sketch DSK 23404 A4.
Transposer Tester TE1/38.
Socket, 25-pole miniature 'D'.
2 off 50Ω termination, 1 watt.

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6. INSPECTION CHECKS

Check that the amplifier has been manufactured satisfactorily in accordance with the drawings. In particular check that:-

6.1 All the chip capacitors are soldered properly and that they are not cracked or shorted.

6.2 All the coupler wires are correctly terminated with very short leads.

6.3 All the power transistors are mounted without strain on their leads or ceramic package, using Dow Corning 340 heat sink compound and nut tightened to a torque of 8±0.5kg cm.

6.4 All the variable capacitors except C217, C236 and C237 are mounted with their rotors earthed and with very short leads.

6.5 The top of the triplate 20dB coupler is fixed as close as possible to PB No. 2.

6.6 The input and output leads are earthed correctly.

6.7 FB201 and FB202 are fitted.

7. TEST PROCEDURE

See warning, section 4.3.

7.1 To Check Current Consumption

7.1.1 Connect the variable power supplier to C1 (+ve) and the chassis. With the current limit set to 1.7 amps gradually increase the voltage to +28 volts and check that the current consumption is within the limits given in 7.1.2. If the current is outside these limits do not increase the voltage further and read section 7.1.3.

7.1.2 10 volts:- 150 ±50mA
20 volts:- 1100 ±100mA
28 volts:- 1500 ±100mA

7.1.3 Check that the voltage at the following points is greater than 0 volts- if not follow the instruction in brackets.

7.1.3.1 C1 (isolate supply to each PCB in turn then examine faulty PCB for short to earth).

7.1.3.2 IC101 and 104 pin 4 (check for o/c resistor or s/c amplifier or capacitor).

7.1.3.3 TR201 base (check for shorts around base bias components and o/c in R204).

7.1.3.4 TR201 collector (check for shorts around collector bias components).

7.1.3.5 TR202, 203, 204 (as for TR201).

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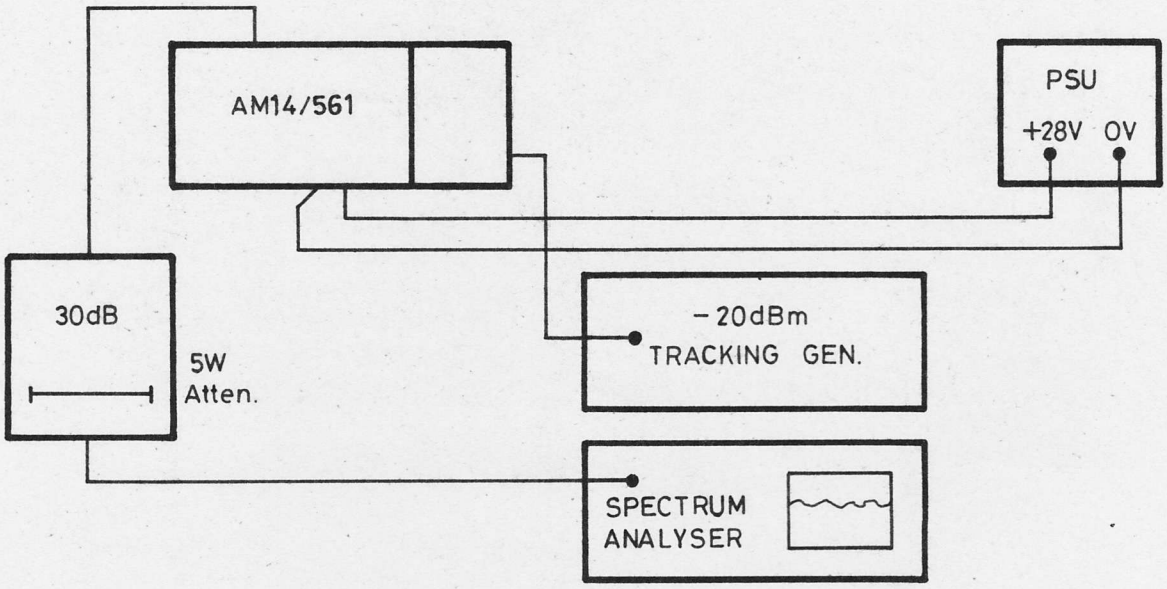
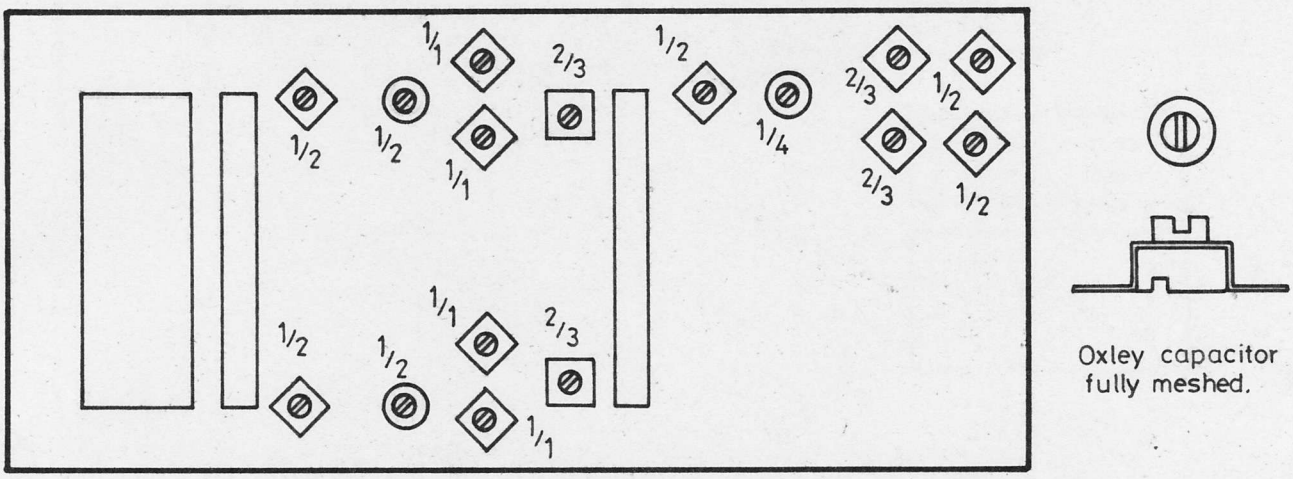
7.2 To Check RF Continuity

Test set up:
Figure 7.2.1



7.2.1 Pre-set the trimmer capacitors so that the vanes are intermeshed to the approximate values shown in Figure 7.2.2.

Figure 7.2.2



Feed -20 ±2dBm (470 - 860MHz) into the AM14/561 amp and check that the gain exceeds the limit given in 7.2.2.

7.2.2 50dB.

7.2.3 If almost no signal is present at the amp O/P check:

7.2.3.1 Link LK1 between the hybrid amp stage and the first transistor stage (copper tape on board 2), link LK3 between the output stage and the triplate coupler (copper tape on board 2).

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7.2.3.2 Chip coupling capacitors (220pF) C204, 212, 224 and 243 are present.

7.2.3.3 If the signal is present, but low particularly at LF, try prodding the coupling capacitors with an insulated rod to see if this produces any change (chip capacitors can easily be damaged by excess heat, causing the termination to part company from the body of the capacitor).

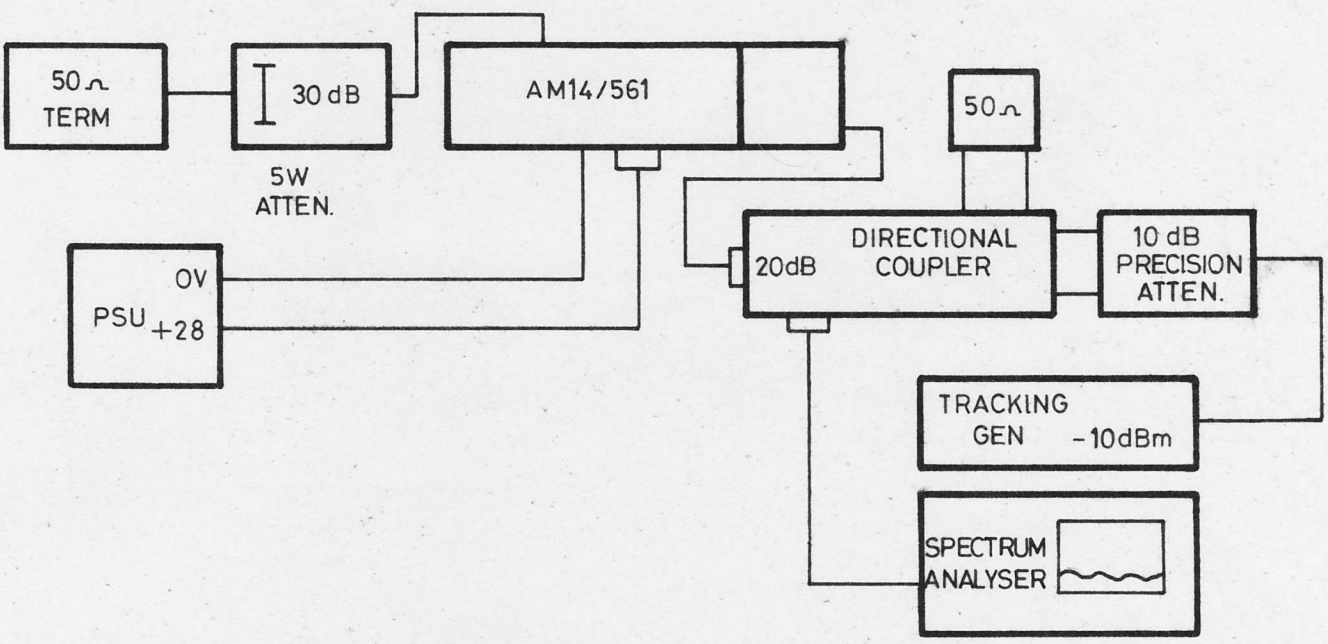
7.3 To Check for Spurious Output or Responses

With the test set up as 7.2 adjust the spectrum analyser sweep to 10 - 1200MHz, and check that there are no spurious outputs or responses caused by instability.

7.4 To Check Input Return Loss

Warning:- Maximum input level at PLF must be ≤-20dBm and PLG must be terminated, otherwise TR203 and/or TR204 may be destroyed.

Test set up:-
Figure 7.4.1

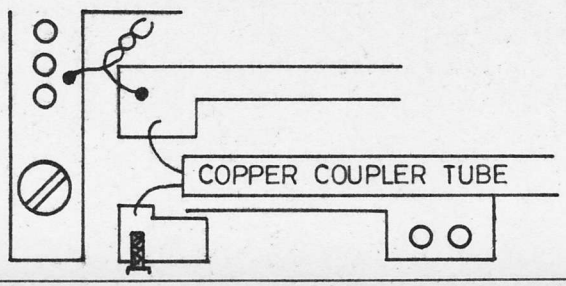


7.4.1 Ensure that the large lid is fitted and that the output of the amplifier is terminated (stray RF fields can effect the return loss display shown on the analyser).

7.4.2 Return loss should be better than 16dB.

7.4.3 If necessary add extra capacitance to the output port of the first 3dB coupler as shown. This is most conveniently achieved by soldering a twisted pair of PUN1/1 wires to the pad and to ground.

Figure 7.4.2



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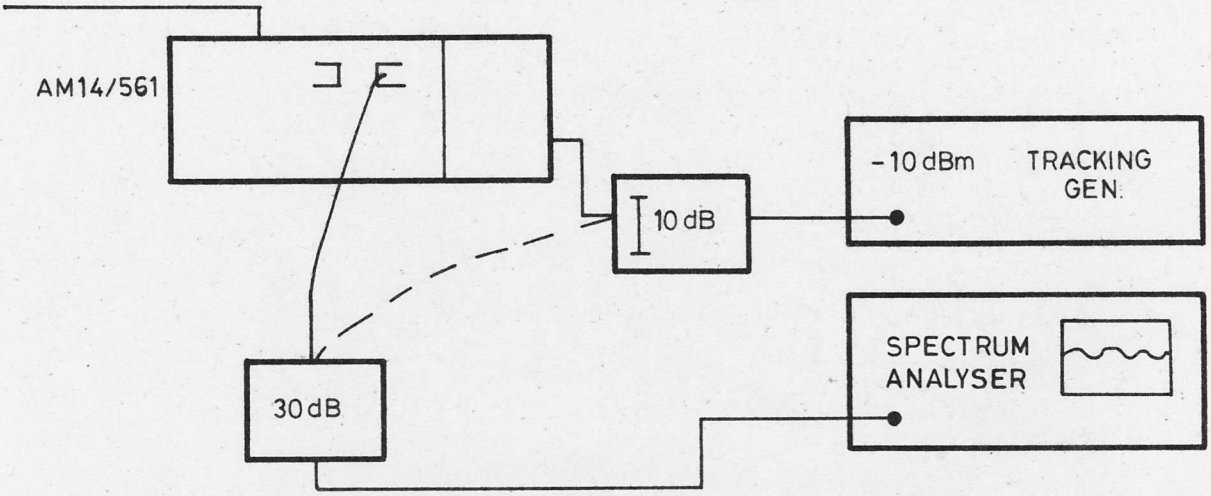
7.5 Alignment of Driver Stage (TR201/2)

Figure 7.5.1



7.5.1 Ensure that trimmers are pre-set as in Figure 7.2.2 and that the small lid is on the hybrid pre-amplifier stage. Set the analyser to centre frequency 660MHz, 100MHz/div., and 1 or 2dB/div.

Calibrate the test system by connecting the 10dB attenuator directly to the 30dB attenuator as shown above (Figure 7.5.1), adjust attenuators on the analyser to display the response, and make a note of it.

Reconnect the cables as shown, with open ended cable connected directly to the output of the driver stage in place of LK2.

Adjust the attenuators to display the frequency response.

Adjust trimmer capacitors (C205, 206), C213, 214), C217 and C218 to obtain maximum gain consistent with flat frequency response (taking into account the frequency response of the measurement system noted above). Trimmers bracketed together should be adjusted so that their capacitances are approximately equal.

7.5.2 The gain should be 45 ±3dB with a variation $<$ ±1dB from 470 to 860MHz. Unsolder the cable and replace the copper tape LK2.

7.5.3 If the gain is low the fault may be isolated by connecting the cable to the output of the hybrid amplifier stage in place of LK1.

7.5.3.1 If the gain of the hybrid amplifier stage is low (it should be between 23dB and 27dB) check the dc voltage at: pin 4 IC1 and at pin 4 IC2 - it should be 23 - 24V.

(Failure of one of the hybrid amplifiers (IC101 or 102) would cause a loss of gain of about 6dB).

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7.5.3.2 If the gain of driver amplifier stage (TR201/2) is low (it should be between 19dB and 21dB) check dc voltages at:

Pin 2 IC201 wrt +28V supply (Pin 1) - should be -5V ±0.3V.

Pin 2 IC201 wrt +28V supply (Pin 1) - should be -5V ±0.3V.

Pin 3 IC201 wrt ground - should be 14 - 21V.

Pin 3 IC202 wrt ground - should be 14 - 21V.

Junction L201/R202 (680Ω 2.5W) - should be 0.75 - 1.00V.

Junction L203/R206 (680Ω 2.5W) - should be 0.75 - 1.00V.

7.6 Alignment of Output Stage TR203/4

7.6.1 Set up the equipment as shown in Figure 7.5.1 but with the 30dB attenuator connected to PLG and link LK2 fitted.

Carry out the procedure as 7.5.1 but adjust the trimmer capacitors (C221, 230), (C222, 223), (C231, 232), (C227, 236) and (C235, 237) to obtain the specified frequency response.

Capacitors bracketed together should be adjusted in such a manner that their capacitances are approximately equal, see Figure 7.2.2.

7.6.2 The gain should be 54 ±3dB with a variation of ±1dB from 470 to 860MHz, when the amplifier is warm, (the gain at 860MHz can drop up to 0.5dB more than the gain at 470MHz when the amplifier is allowed to warm up from cold). Put the large lid on and check that there is no significant change in frequency response.

7.6.3 If the gain of the output amplifier stage is low (it should be between 8dB and 10dB) check dc voltages:

Pin 2 IC203 wrt +28V supply (Pin 1) - should be -5V ±0.3V.

Pin 2 IC204 wrt +28V supply (Pin 1) - should be -5V ±0.3V.

Pin 3 IC203 wrt ground - should be 14 - 21V.

Pin 3 IC204 wrt ground - should be 14 - 21V.

Junction L204/R211 (680Ω 2.5W) - should be 0.75 - 1.0V.

(Failure of one half of the output amplifier stage would result in a reduction in gain of about 6dB).

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7.7 Re-check for Spurious Outputs

7.7.1 Connect a 50Ω termination to PLF and connect PLG through a 30dB attenuator to the spectrum analyser.

Sweep analyser from 10MHz - 1.2GHz.

7.7.2 Check that there are no spurious outputs caused by instability.

7.8 To Check Intermodulation Products (IP's)

Figure 7.8.1

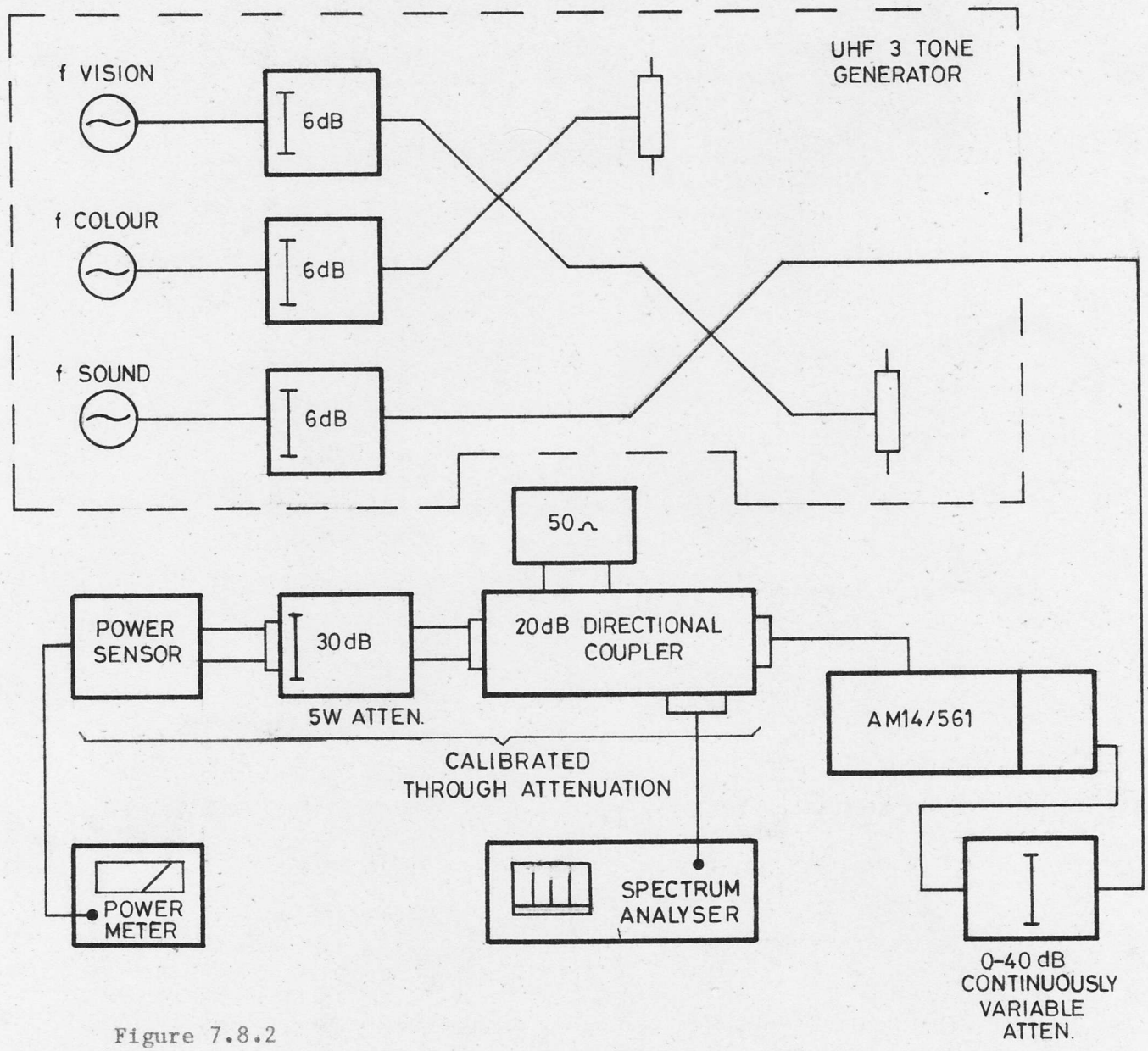
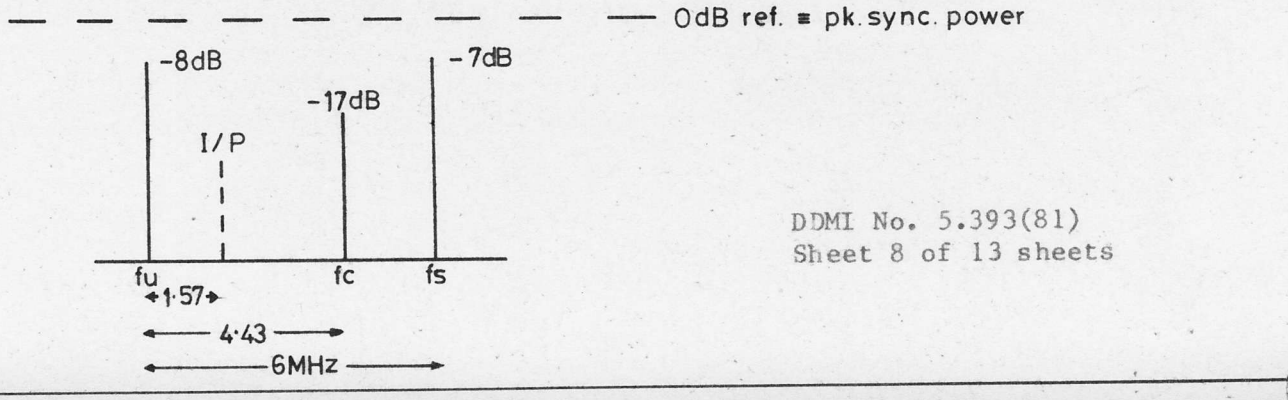


Figure 7.8.2



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NOTES

The through attenuation of the directional coupler and 30dB attenuator should be measured at the frequencies the IP's are to be checked at (470 - 660MHz and 860MHz) and noted.

If the attenuation is exactly 30dB, then the power meter will read -1.2dBm when the AM14/561 is producing rated output (the peak envelope rated power is 33dBm, and mean power is 4.2dB below this, therefore the meter reading should be +33dBm -4.2dB - 30dB).

Take care not to exceed the spectrum analyser's input level when making measurements (the analyser input attenuator should be switched to 20dB).

The power meter sensor, 30dB attenuator, andd 20dB coupler should be connected directly together without cables, and the input to the coupler should be connected directly to PLG.

7.8.1 Set the three oscillator frequencies as shown in Figure 7.8.1 with fv at 860MHz. Then adjust their relative levels, to an accuracy of ±0.2dB as follows:-

Set the spectrum analyser to 1dB/division, 30kHz bandwidth, 1MHz/division scan width and 20dB RF attenuation. Adjust the continuously variable attenuator on the input of the AM14/561 so that the amplifier is producing less than rated output power. Adjust the IF attenuators on the analyser so that the sound oscillator is in the centre of the screen, then adjust the level of the vision oscillator to be 1dB lower; reduce the IF attenuation by 10dB and adjust the level of the colour sub-carrier oscillator to be in the centre of the screen.

Increase the IF attenuator by 10dB check the levels of the vision and sound oscillators, then switch to 10dB/division. The oscillators should now be set to -8dB, -17dB and -7dB relative to peak envelope power for the vision, colour and sound oscillators respectively.

Reduce the amplifier input attenuation to obtain +33 ±0.1dBm at PLG and increase the spectrum analyser IF attenuation until the vision carrier is 8dB from the top of the screen. The level of the IP at fv ±1.57MHz should be as in 7.8.2.

Repeat the measurement with fv at 470MHz and 660MHz.

7.8.2 Lower than 53dB from the top of the screen. If it is higher, then read section 7.8.3.

7.8.3 Without adjusting the input level to the AM14/561 measure the IP values at the output of the driver stage (LK2) and the output of the hybrid amplifier stage (LK1). They should be better than -60dB and -70dB respectively.

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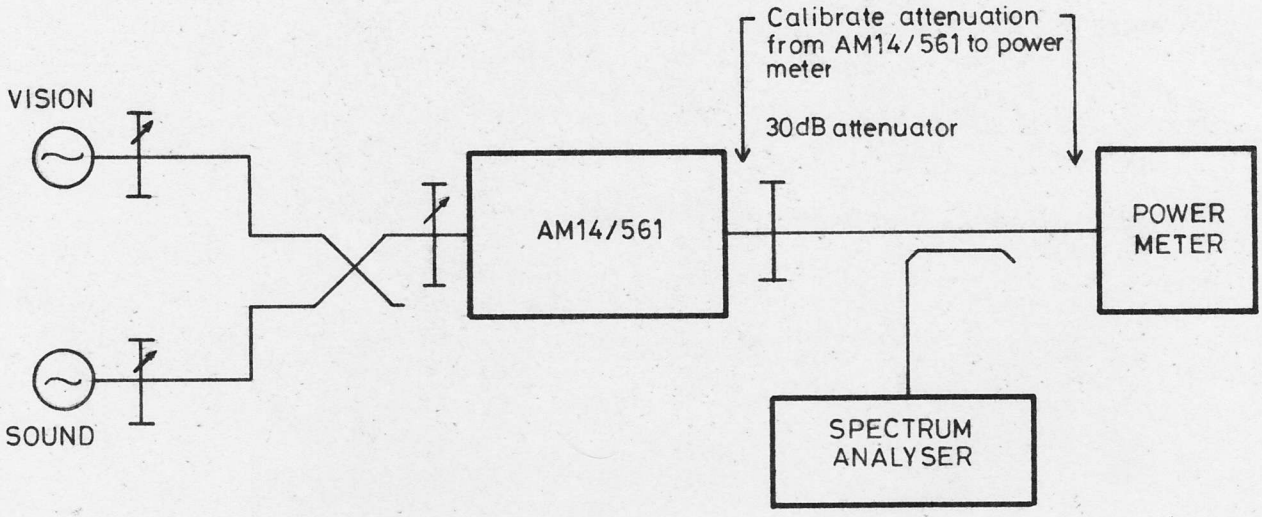
7.9 To Measure Crossmodulation

7.9.1 Connect the test equipment as shown in Figure 7.9.1.

Figure 7.9.1



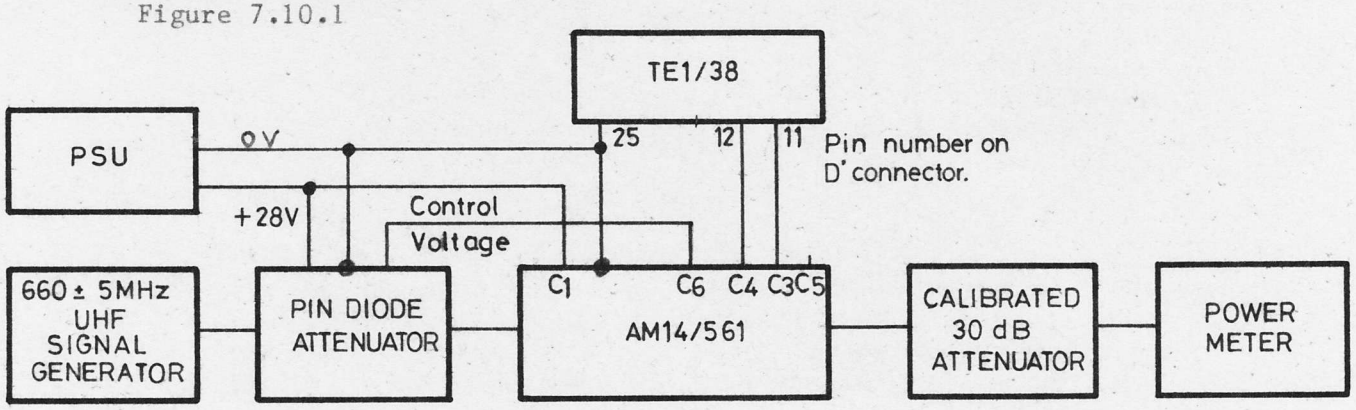
Switch off the sound oscillator and adjust the level of the vision frequency signal to obtain an output of +33 ±0.1dBm from the AM14/561. Set the spectrum analyser to 1 or 2dB/div and adjust its attenuator so that the trace is on the top line of its graticule. Switch on the sound oscillator and adjust its level to 7 ±0.1dB below the vision carrier level, but note that the vision carrier may drop in level due to the effect of crossmodulation. Increase the level of both signals until the vision carrier is on the top line of the graticule (i.e. vision carrier at +33dBm and sound carrier at +28dBm).

Switch off the vision oscillator and set the spectrum analyser to linear with the sound carrier on the top line of the graticule. Switch on the vision carrier and measure the percentage reduction in sound carrier level.

7.9.2 The reduction (static crossmodulation) should be less than 9% (typically 5%).

7.10 To Check the Peak Detector in the AGC Circuit

Figure 7.10.1



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7.10.1 Set up the equipment as shown above but remove the control voltage from the PIN diode attenuator. Set the signal generator to obtain +33 ±0.5dBm output from the amplifier (+3dBm on power meter). Measure the voltage across R305.

7.10.2 It should be 1±0.3 with the end connected to pin A (nearest edge of board) positive.

7.10.3 If the voltage is outside this range check the following voltages:-

7.10.3.1 Pin A (should be +11 ±0.5 volts).

7.10.3.2 Pin B wrt pin A (should be -1 ±0.3 volts).

7.11 To Check the Temperature Compensation Circuit

7.11.1 With the conditions the same as 7.10 measure the voltage on IC302a pin 1.

7.11.2 It should be +8 ±0.5 volts.

7.11.3 If the voltage is outside this range check the voltage across D303 (should be 0.2 ±0.04 volts).

7.12 To Check the Maximum-gain Control Circuit

7.12.1 Switch off the generator output. Set the gain and power switches on the TE1/38 to 'fixed'. Measure the gain control voltage on the 'filtercon' C6 (to AM21/506).

7.12.2 It should be +10 ±0.5 volts.

7.12.3 If the voltage is outside these limits check the following voltages:-

7.12.3.1 Pin A (should be +11 ±0.5 volts).

7.12.3.2 IC302b pin 10 (should be +8.5 ±1 volts).

7.12.3.3 IC302d pin 12 (should be +4.5 ±0.25 volts).

7.12.3.4 IC302d pin 14 (should be +6 ±1 volts).

7.13 To Check the AGC Loop and Calibrate the Output Power Control

7.13.1 Connect the control voltage to the pin diode attenuator. Adjust the signal generator output to -10 ±5dBm in order to set the PIN diode attenuator within its operating range. Set the maximum gain switch to 'var' and the control fully clockwise (max. gain). Measure the output power.

7.13.2 Power should be +33 ±0.2dBm.

7.13.3 If the power is +33 ±2dBm adjust R316 (if the power is low reduce R316, approximately 0.4dB change per step in value). Other wise check the following voltages:-

7.13.3.1 IC303a pin 12 (should be 1 ±1 volts).

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7.13.3.2 IC303b pin 10 (should be +27 ±1 volts).

7.13.3.3 IC303a pin 1 (should be 8.6 ±1 volts).

7.13.3.4 IC303b pin 7 (should be -0.23 ±0.05 wrt IC303a pin 1).

7.14 To Check the Output Power Range

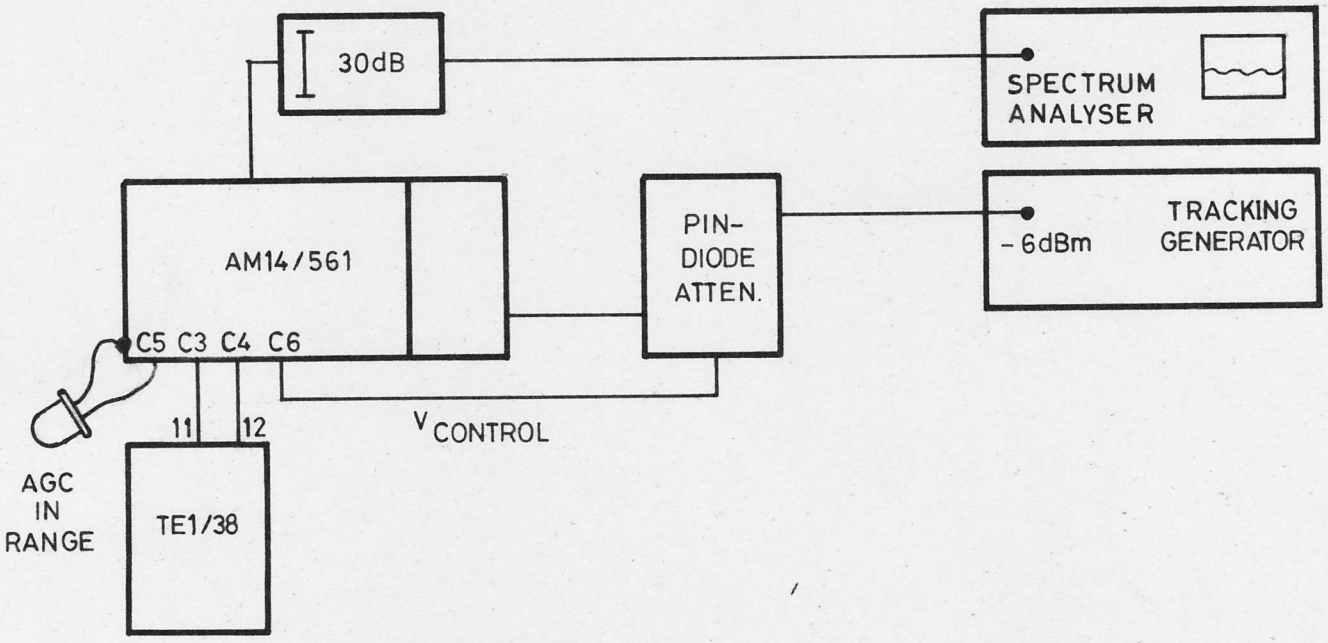
7.14.1 Switch the output power switch to 'var'. Adjust the output power potentiometer over its full range and measure the maximum and minimum power from the amplifier. Ensure that the PIN diode attenuator stays within its operating range.

7.14.2 The power range should be at least +34 to +23dBm.

7.14.3 If this range is not achieved check the range of voltage on IC302b pin 10 (should be at least +7.5 to +10 volts). If this is correct remove the control voltage from the PIN diode attenuator and set the output power switch to 'fixed'. The check that the control voltage swings from +3 to +26 volts (at least) when the output power is adjusted from +32 to +34dBm, using the level control on the signal generator.

7.15 To Check Closed Loop Output Power Variation with Frequency

Figure 7.15.1



7.15.1 Switch TE1/38 to fixed power, and maximum gain control to 'var' with pot fully clockwise (power normal LED should be lit). Set analyser sweep speed to very slow, (i.e., 2 sec./div.), and 50MHz/div. with 660MHz as centre frequency.

Calibrate the system by disconnecting the 30dB attenuator from the AM14/561 and reconnecting it directly (without a lead) to the tracking gen. Not the variation in response

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from 470 - 860MHz (due to attenuator, lead and analyser). (NB AGC system will automatically compensate for frequency response errors due to input cable etc.).

Reconnect the 30dB attenuator as shown in Figure 7.15.1 and observe the response.

7.15.2 The variation should be less than ±0.75dB from 470 - 860MHz, taking into account the variation noted in 7.15.1, if it is not see section 7.15.3.

7.15.3 Check the video detector circuitry on board 2 and check the mechanical fixing of the triplate cover on the 20dB coupler.

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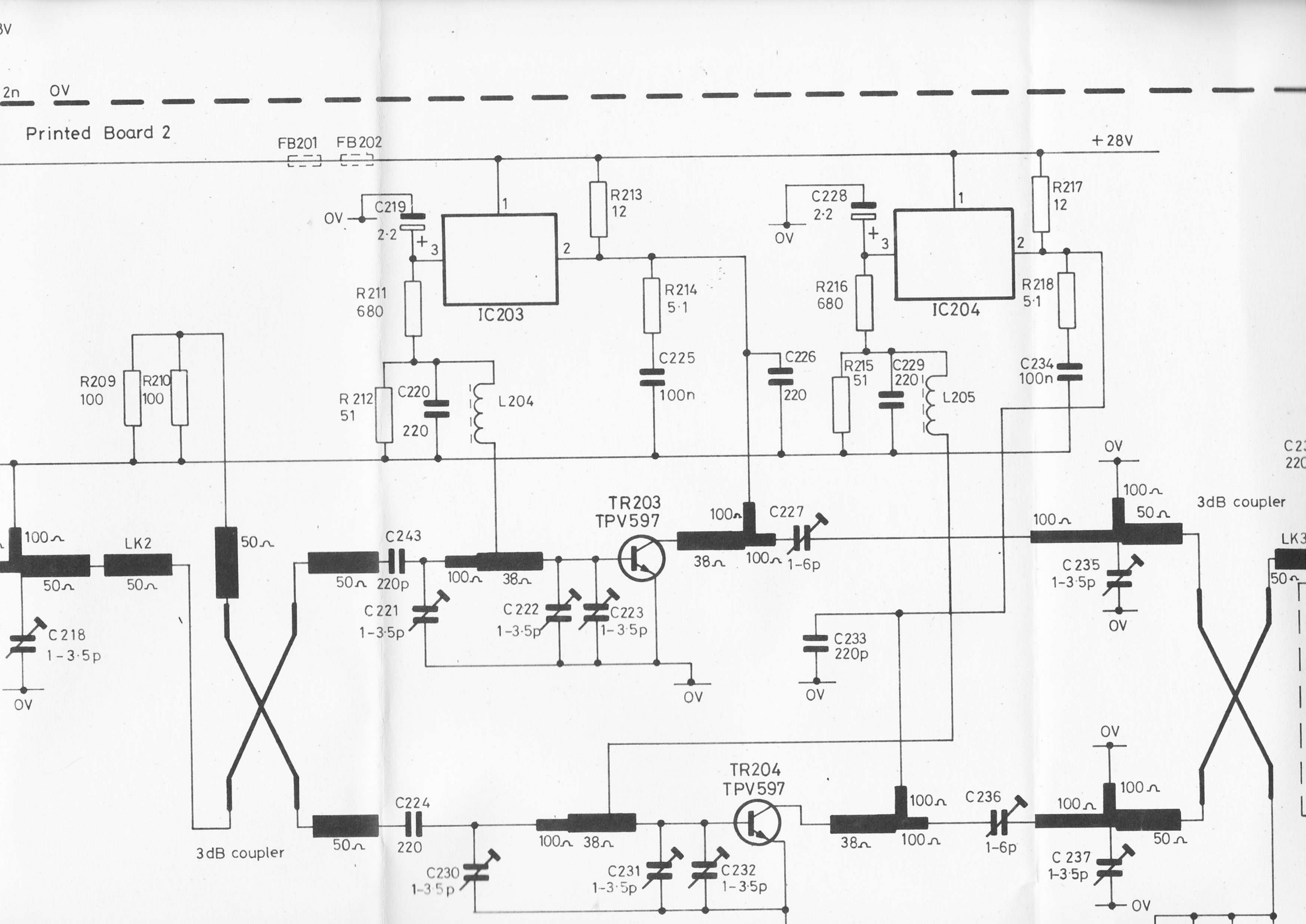
Printed Board 2
FB201
FB202
+28V
OV
C219
2·2
R213
12
IC203
R211
680
R214
5·1
C225
100n
C226
220
C228
2·2
R217
12
IC204
R216
680
R218
5·1
C234
100n
R215
51
C229
220
L205
R209
100
R210
100
R212
51
C220
220
L204
TR203
TPV597
C227
1-6p
C243
220p
C221
1-3·5p
C222
1-3·5p
C223
1-3·5p
C233
220p
C235
1-3·5p
C218
1-3·5p
LK2
LK3
3dB coupler
3dB coupler
TR204
TPV597
C224
220
C230
1-3·5p
C231
1-3·5p
C232
1-3·5p
C236
1-6p
C237
1-3·5p
50Ω
100Ω
38Ω

CHANGE	ISS.
18-6-81	1
RM. 30.6.81.	1A
TT. 28-7-81	2

AM14/561 P. LIST
U.H.F. POWER AMPLIFIER.

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
			DRAWING NUMBERS		
			CIRCUIT D49937 A1		
			P. LIST D49938 A4		
			ASSEMBLY D49939 A1		
			DETAILS D49940 A1		
			P.B No 1 (2 SHEETS) D49941 A2		
			" " ASSY INFORMATION D49942 A2		
			" " DRILLING D49943 A3		
			P.B No 2 (2 SHEETS) D49944 A1		
			" " ASSY INFORMATION D49945 A2		
			" " DRILLING D49946 A2		
			P.B No 3 (3 SHEETS) D49947 A2		
			" " COMP LOC D49948 A2		
			" " DRILLING D49949 A3		
			WIRING D49950 A2		
			LABEL D49951 A4		
			FURTHER INFORMATION REQUIRED FOR MANUFACTURE :		
			UNIT ASSY INFORMATION EA 10484		
			UNIT WIRING INFORMATION EA 10137, EA 10139, EA 10140		
			BERYLLIUM WARNING LABEL D40615 A4		
			COUPLER TUBE D49983 A4-CP		
			ETCHED BRACKETS D49981 A2-CP, D49982 A2-CP		
			SPEC. ED/AM14/561		
1	1	>	LARGE EXTRUSION		D49940 A1 DET 1
2	1	<	SMALL EXTRUSION		" DET 2
3	1		REAR PLATE		" DET 3
4	1		FRONT PLATE		" DET 4
5	4		TIE ROD		" DET 5
6	1		CABLE CLAMP BAR		" DET 6
7	1	^	COVER (SMALL)		" DET 7
8	1	v	COVER (LARGE)		" DET 8
9	1		DIVIDING PLATE		" DET 9
10					
11	1	*+	BOX EXTRUSION (2 METRES LONG).		0423504
12	1	*+	COVER EXTRUSION (2 METRES LONG).		0423512.
13					
14	1	*	P. BOARD No 1 TO SPECIFICATION ED/PB/AM14/561/PTH/1		D49941 A2, D49942 A2 D49943 A3 - 0436815
15	1	*	P. BOARD No 2 — SEE NOTE BELOW		
16	1	*	SCREEN — SEE NOTE BELOW		
			ITEMS 15 & 16 MADE FROM 1 COMPOSITE PRINTED BOARD TO SPECIFICATION ED/PB/AM14/561/PTH/2		D49944 A1, D49945 A2 D49946 A2 - 0436823

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BBC

DS/PLA4

AM14/561 PARTS LIST

U.H.F POWER AMPLIFIER

DRN.	K. TURNER	DESIGNS DEPARTMENT
TPD.		
CKD.	M.T.E	D49938 A4
APPD.		

FOR COMPONENT CONFIGURATION
SEE DRAWING D49948 A2

30 94 IN 2 POSN ON P.B 2
(SEE NOTE 5)

15 65 FOR COMPONENT CONFIGURATION
SEE DRAWING D49945 A2.

30 94 IN 2 POSN. ON P.B 1
(SEE NOTE 5)

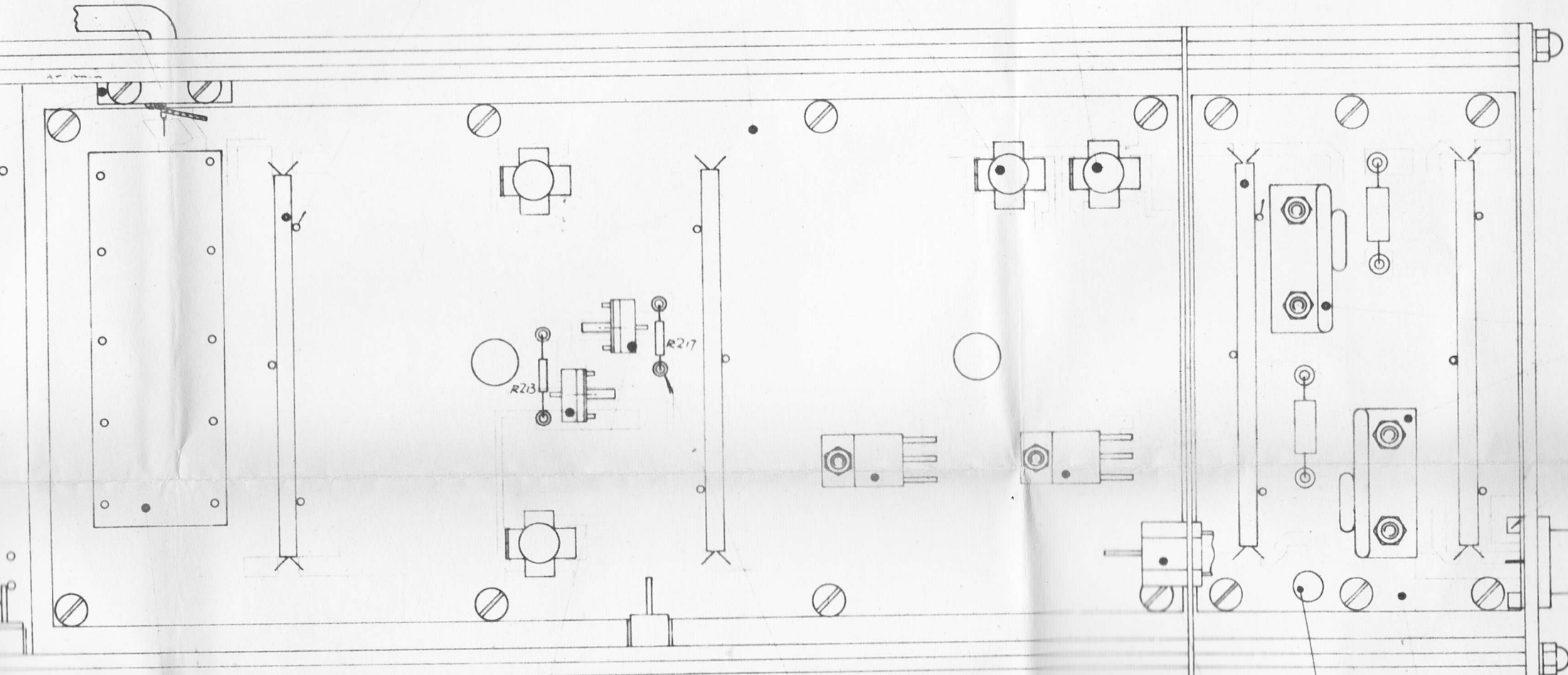
FOR METHOD OF TERMINATION
& CLAMPING OF CABLE
SEE SKETCH B.

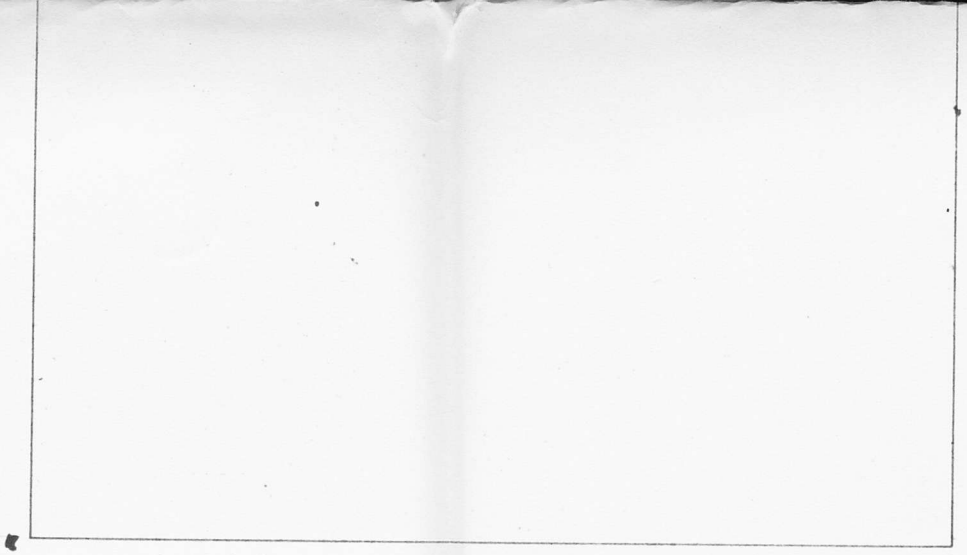
37 IN 6 SIMILAR POSN.
ON P.B 2, TO PROJECT
ON COMP SIDE OF
BOARD (SEE NOTE 5)

138 IN 3 POSN
SEE NOTE 4

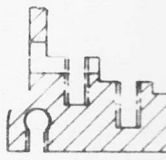
137 SEE NOTE 4

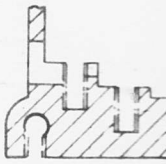
37 IN 6 SIMILAR POSN.
ON P.B 1, TO PROJECT
ON COMP SIDE OF
BOARD (SEE NOTE 5)





BOTH VIEWS
ON ℄ OF





THRO OUTER
PART ONLY

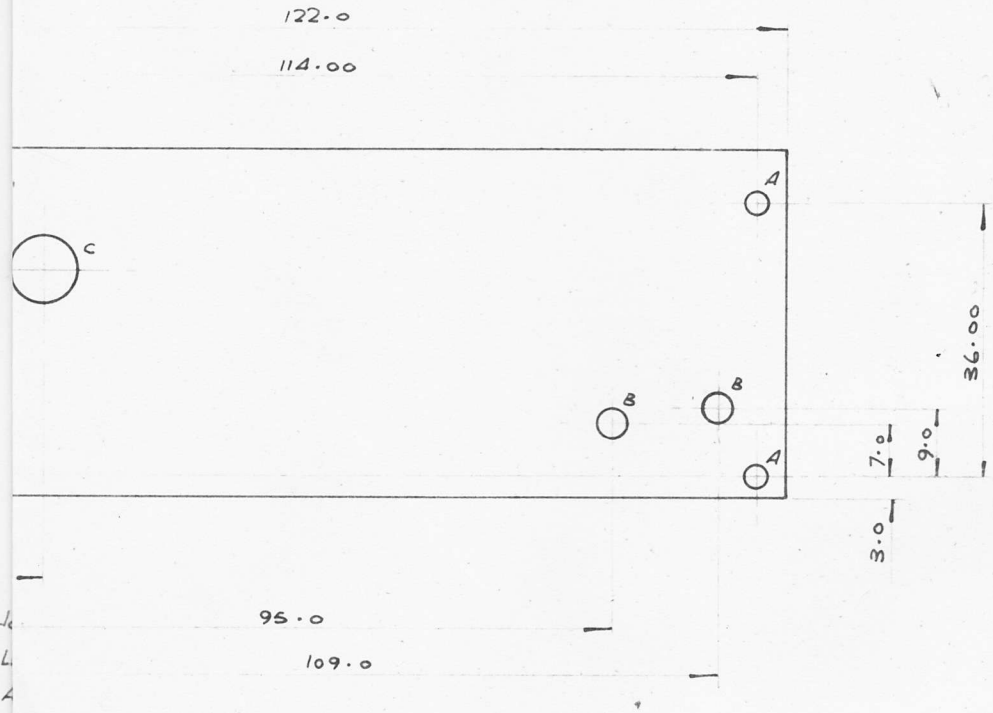
DRILLING DATA

A DR 3.2 DIA
B DR 4.5 DIA
C DR 9.0 DIA
D DR 4.2 DIA & C'B
14.0 DIA X 4.0 DE
E SEE SKETCH ABOV

SMALL)
LARGE)
N, INDALEX TYPE BBC 111

DETAIL	LENGTH 'L'
7	64.5 ± .2
8	283.5 ± .2

D49940 A1



IN A
EXTON
DEP

PLATE
AL. ALLOY
NS4-H3

DRILLING DATA

A DR 3.4 DIA
B DR 4.0 DIA
C DR 9.0 DIA

D49940 A1

VE ALL SHARP EDGES, CORNERS
RRS

P. LIST D49938 AA
SCALE 1:1 EXCEPT WHERE STATED OTHERWISE

SCALE –

THIRD ANGLE PROJECTION

114/561 DETAILS

BBC
DS/A1/1

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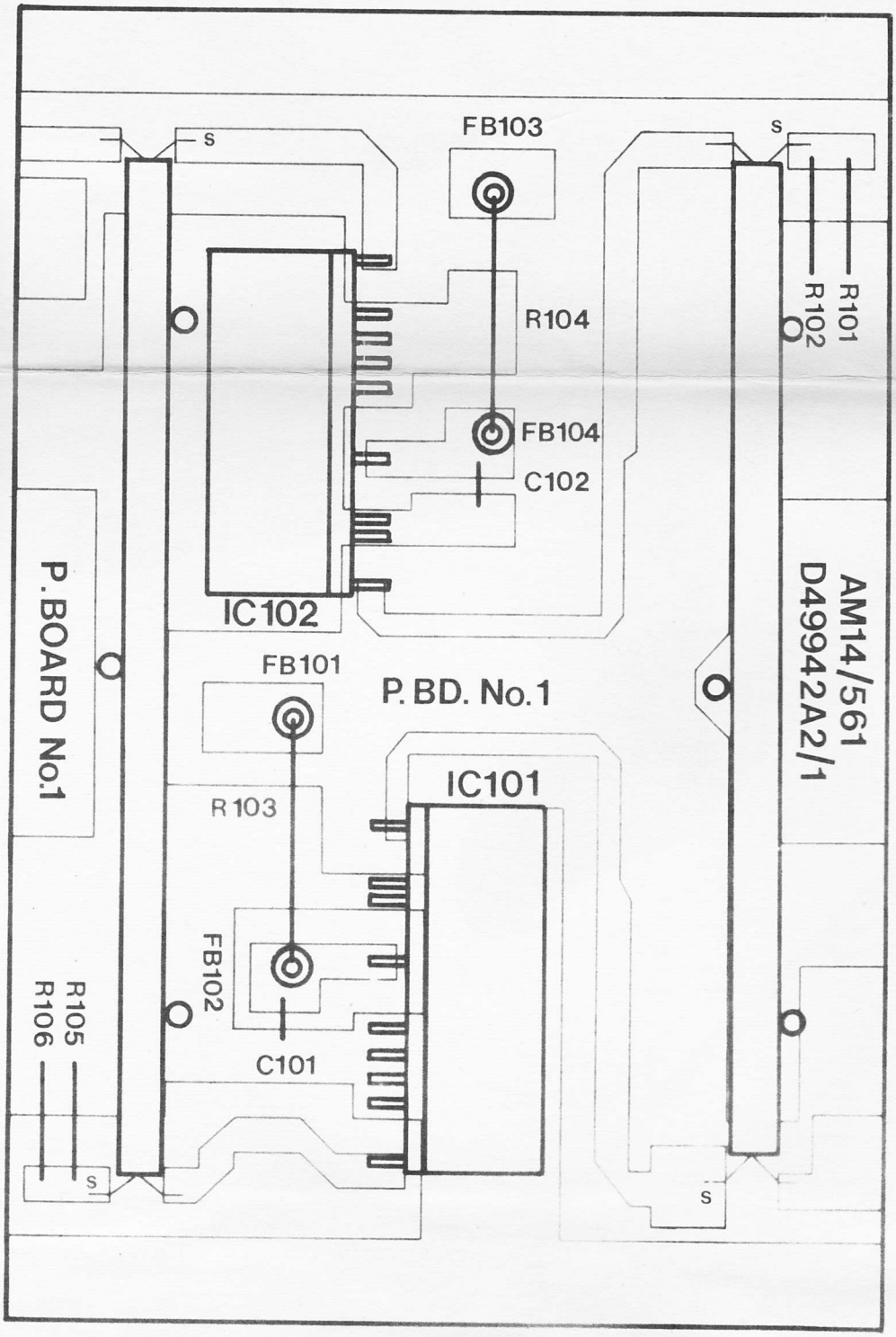
permission

llimetres unless otherwise stated :
— ± 1 mm unless
— ± 0·3 mm otherwise
s — ± 0·1 mm stated

DRN.	K. TURNER	DESIGNS DEPARTMENT
TCD.		
CKD.	M.T.E.	D49940 A1
APPD.		

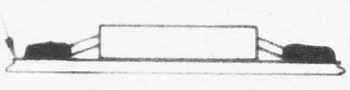
S & H LTD L5429



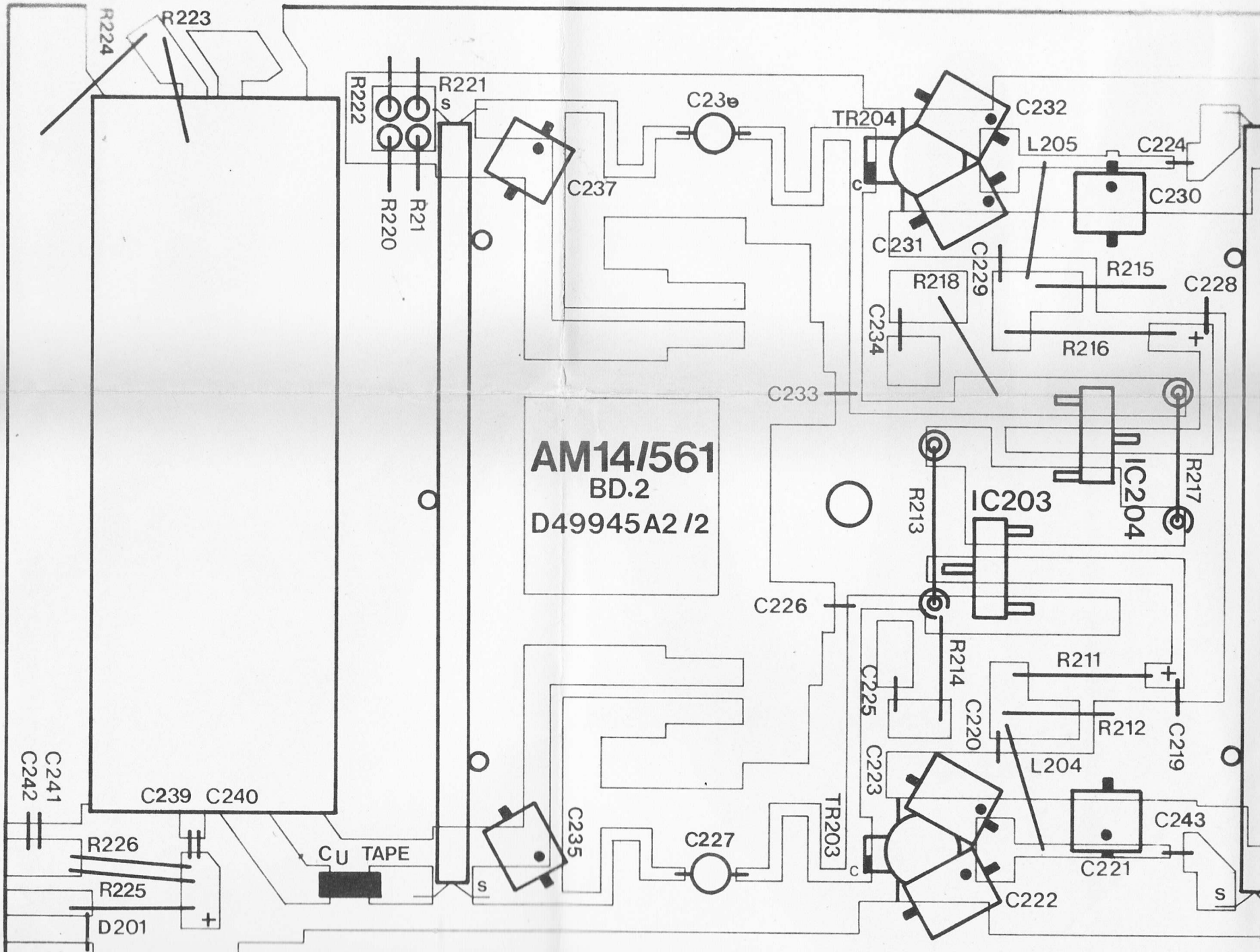
mount chip capacitors

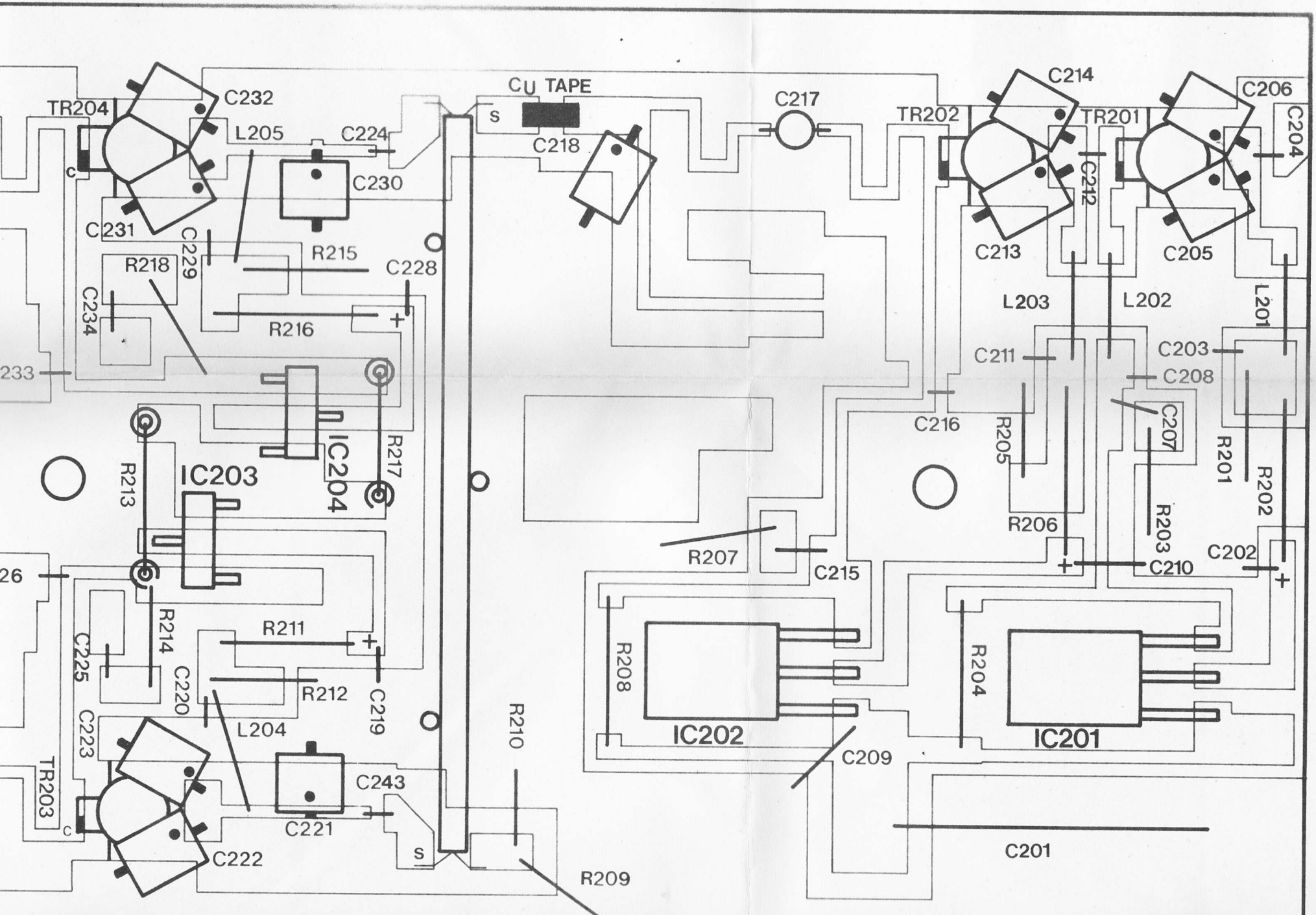
lting point solder to DIN 1707
minal.

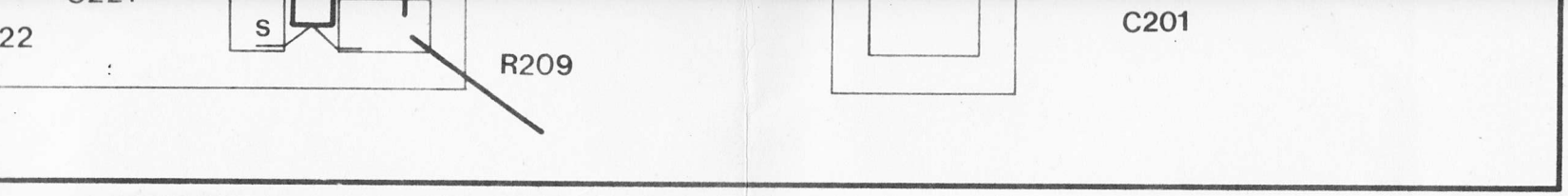
ent as shown in sketch A

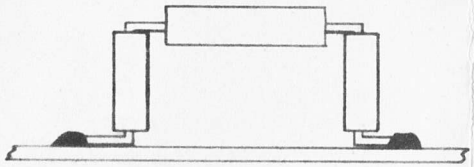


Sketch 'A'


AM14/561
BD.2
D49945A2/2
R223
R224
R222
R221
R220
R21
C237
C236
TR204
C232
L205
C224
C230
C231
C229
R215
C228
R218
C234
R216
C233
IC204
IC203
R217
R213
C226
R214
C225
R211
C220
R212
L204
C219
C223
TR203
C243
C221
C222
C227
C235
C239
C240
C241
C242
R226
R225
D201
CU TAPE

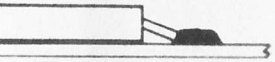

TR204
C232
L205
C224
Cu TAPE
C217
TR202
C214
TR201
C206
C204
C230
C218
C212
C231
C229
R215
C228
C213
C205
R218
L203
L202
L201
C234
R216
C211
C203
C208
233
C216
C207
R205
R201
R202
IC203
IC204
R217
R213
R206
R203
C202
R207
C215
C210
26
R214
R211
R208
R204
C225
C220
R212
C219
IC202
IC201
C223
L204
C209
R210
TR203
C243
C221
C201
C222
R209

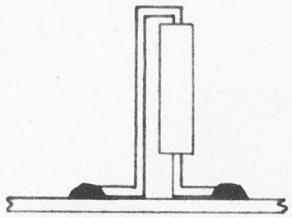




Sketch 'B'

Method of mounting R213 & R217

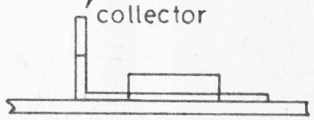




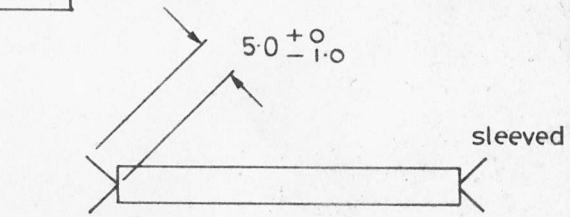
Sketch 'C'

Method of wiring components R219–R222 to printed board

Collector on TR201, TR202, TR203 & TR204 to be bent at 90° and then soldered to printed board as shown.



Sketch 'D'



Sketch 'E'

Coupler terminations
Outer insulation of wire to be cut to same length as tube (75·0)

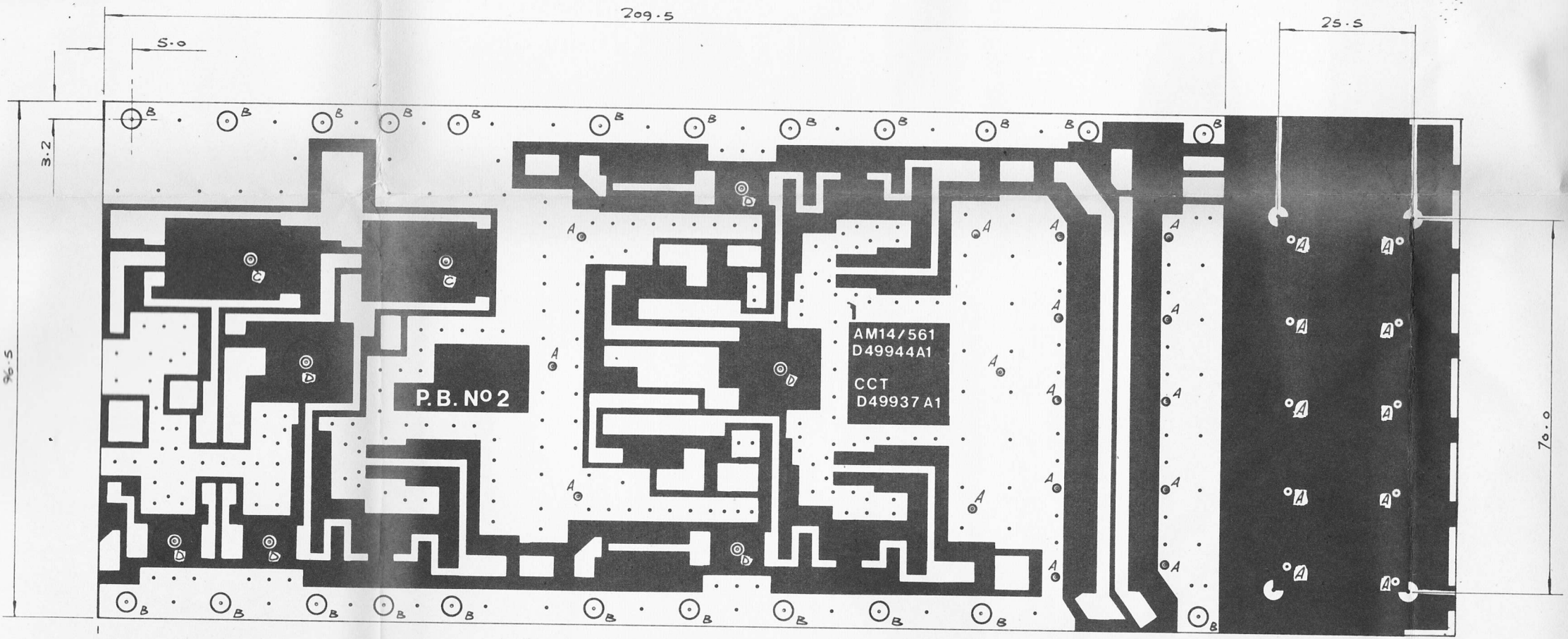
AM14/561

PRINTED BOARD No. 2 ASSEMBLY INFORMATION

All dimensions in millimetres unless otherwise stated :
Normal tolerances :
no decimal place — ± 1 mm unless
one decimal place — ± 0·3 mm otherwise
two decimal places — ± 0·1 mm stated

DRN.	K.T.	DESIGNS DEPARTMENT
TCD.	S.A.T	D49945A2
CKD.		
APPD.		

S&H LTD L5064



P. BOARD 2

SCREEN.

CUT-HERE

APPROXIMATE NO. OF HOLES = 306