Issue 1
1/2/79

DESIGNS DEPARTMENT MANUFACTURING INFORMATION

No. 6.332 (78)

AUDIO DELAY UNIT

UN14/12

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for Head of Designs Dept.

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D.N. Davison

GP

D.D.M.I. No. 6.332 (78)
Title Sheet

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C O N T E N T S

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Audio Delay Unit UN14/12

1. Introduction

This unit, which forms part of Audio Delay Equipment EP1M/23, will delay an audio signal by a preset time between 1.5 and 6m in 10µS steps or between 3 and 12ms in 20µS steps. It consists of two boards, one contains "bucket brigade" delay lines and the other contains a frequency synthesiser to provide the necessary clock pulses for the delay lines.

Two "bucket brigade" integrated circuits are used and each integrated circuit contains two 512 stage analogue shift registers. They are connected in a parallel/push-pull configuration to obtain optimum performance. Low pass filters with a cut off frequency of 10kHz are connected before and after the delay lines to prevent aliasing and remove sampling frequency components respectively.

The delay time is proportional to the reciprocal of the clock frequency, so by passing the output of a fixed oscillator through a programmable divider, a delay proportional to the division ratio is obtained. In order to use a low power programmable divider it is operated at a 512th of the required frequency and a phased locked loop is used to multiply its output by 512.

The delay may be set by DIC switches plugged into DIL sockets or, for more permanent installation soldered wire links. Eleven links are used and they are BCD coded such that the delay is easily related to the code number.

Pins 6 and 7 are joined so the presence of the unit may be detected. By using this facility the EP1M/23 switches to bypass if the UN14/12 is removed.

2. Specification

Performance Data:

Inputs:	Audio input	Unbalanced
	Audio input impedance	5KΩ
	Audio input level	zero programme volume
	Power consumption	+25 ± 1 volts at 60 ± 10mA
Outputs:	Audio output	Unbalanced
	Audio output impedance	<50Ω
	Audio output level	zero programme volume

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Delay range	1.5 to 12mS (plus delay in low pass filter)
Delay increments	10µS or 20µS
Delay tolerance	±0.01% from 10° to 50°C
Frequency response	±0.5dB from 100Hz to 6.5kHz
Gain variation with delay	±0.5dB from 1.5 to 12mS delay
Total Harmonic separation	Better than 50dB for an input signal of 1kHz at +8dBm into 600Ω
Signal to noise ratio	better than 50dB4w

Mechanical Data:

Chassis: CH1/65A
Indexing positions: 1,12,15
Plug Indexing positions: A1
Weight: 0.5kg

Installation Data:

Mount in PN3/55 and wire to pins as follows:-

1 - chassis earth

2 - audio input, balanced

3 - audio input, balanced

4 - not used

5 - not used

6 - These pins are joined in the unit and they may be used to detect
7 - that the unit is in position.

8 - not used

9 - power supply earth (0 volts)

10 - not used

11 - not used

12 - audio output (unbalanced live)

13 - audio output (earth)

14 - not used

15 - not used

16 - not used

17 - power supply positive (+25 volts)

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Audio Delay Unit UN14/13

PRODUCTION TEST SCHEDULE

1. Description

This unit will delay an audio signal by a preset time between 1.5 and 6mS in 10µS steps or between 3 and 12mS in 20µS steps. It consists of two boards one contains "bucket brigade" delay lines and the other contains a frequency synthesiser to provide the necessary clock pulses for the delay lines.

The frequency synthesiser should be tested first, as it is needed to drive the delay lines. It consists of a 1MHz crystal oscillator, which drives a CMOS integrated circuit that contains a divide-by-10 followed by three programmable decade dividers. The output from this divider is then multiplied by 512 by phase-locking its output with the output of a 9-bit counter. The input to the counter, which is driven from a VCO, is the required output frequency from the synthesiser.

The audio delay is provided by two "bucket brigade" integrated circuits, each of which contain two 512 stage analogue shift registers. The two shift registers within each integrated circuit are connected in a "parallel-multiplier" configuration, which means that the audio signal is alternately sampled by the two shift registers. The two pairs of shift registers are connected in a differential (push-pull) configuration, that is, they are driven in anti-phase and their outputs are summed in a differential amplifier. This arrangement provides some circuit redundancy, because if one bucket brigade I.C. fails the output only drops 6dB. Switching transients and even harmonic distortion are also minimised.

In order to obtain optimum performance from the "bucket brigade" shift registers it is necessary to drive them at the correct level, so two A.O.T. gain controls are provided. The first is used to set the "bucket brigade" input level and the other is used to adjust for 0dB gain. It is also necessary to optimise the d.c. bias on the audio input to the "bucket brigade" shift registers and an A.O.T. resistor is provided for this purpose.

Low pass filters with a cut off frequency of 10kHz are connected before and after the delay lines to prevent aliasing and remove sampling frequency components respectively.

2. Information:

a)	Design Section:	Transmission Section
b)	Designer:	M.T. Ellen
c)	Engineer Responsible:	D.C. Savage
d)	Handbook:	Part of Handbook No. 6.163 (78) for Audio Delay Equipment EP1M/23
e)	Technical Instruction:	Not available 1.7.78
f)	Other information:	
g)	Pre-production batch:	This Production Test Schedule has been tested on a pre-production batch in Designs Department.

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3. Manufacturing Performance Specification

a) Input requirements:
Low distortion sine wave 20Hz to 15kHz at +10dBm max.

b) Outputs:
Similar to input but delayed by up to 12mS

c) Power Supply:
+25 ± 0.5 volts at 60 ± 10mA

d) Performance:

Gain:	0 ± 0.5dB at 1kHz over full delay range
Frequency Response	±0.5dB from 100Hz to 6.5kHz
Total Harmonic separation:	better than 50dB from an input signal of 1kHz at +8dBm into 600Ω
Signal to Noise ratio:	better than 50dB4w

4. Warnings:

a) No voltages above 50V d.c. or 30V a.c. are connected to this unit.

b) This unit contains MOS devices. Ensure that they are not subjected to electrostatic discharges.

5. Test Apparatus Required:

1 off 0 to 30 volt variable power supply up to 100mA, fitted with an ammeter and current limit control.
1 off Frequency counter, maximum frequency > 1MHz
1 off Oscilloscope, B/W > 10MHz
2 off Oscilloscope probes
1 off A.C. Test Equipment type EP14/1
1 off A.V.O.

6. Inspection:

a) Check that the slot positions of the coding comb are correct.

b) No mains voltages are connected to this unit. Check all the connections between PCB1 and PCB2.

c) Check that the following components are correctly inserted.

i) Capacitors 1C1 - 1C15, 2C1 - 2C8
ii) Resistors 1R1 - 1R31, 2R1 - 1R17
iii) Integrated Circuits 1IC1 - 1IC11, 2IC1 - 2IC4
iv) Crystal 2XL1
v) Plug
vi) DIC switches

7. Test Procedure:

7.1 To check current consumption

a) Connect the PSU (set to 0 volts) to PLA 9 (-ve) and PLA 17 (+ve). Gradually increase the voltage to 30 volts while monitoring the current.

b) The current should increase to 60 ± 10mA when the voltage reaches 18 volts and then stay constant up to 30 volts.

c) If the current is incorrect remove the power supply link to PCB 2 and repeat the test. For this test the current should be 55 ± 10mA, if so the fault is on PCB 2 otherwise it is on PCB 1.

7.2 To check crystal oscillator

a) Connect the frequency counter and the oscilloscope to 2IC 1 pin 1. Measure the frequency and amplitude of the waveform.

b) The frequency should be 1MHz ± 100Hz and the waveform should be an approximately square wave between 0 and +15 volts.

c) If the frequency is wrong check the crystal, 2C1 and 2C2. If the amplitude is wrong check 2IC2.

7.3 To check variable divider

a) Connect the frequency counter and the oscilloscope to 2IC1 pin 23. Measure the frequency and shape of the waveform with the switch settings shown in section b.

b) The waveform should be a positive pulse (+15 to 0 volts) with a duration of 1μs i.e. one cycle of the input waveform.
The frequencies should be as follows:

Table 1

Switch position (1 means on, 0 means off)												Frequency Hz
Hundreds			Tens				Units					
13	12	11	9	8	7	6	4	3	2	1		
1	0	0	0	0	0	0	0	0	0	0		250
0	1	0	0	0	0	0	0	0	0	0		500
0	0	1	0	0	0	0	0	0	0	0		1000
0	0	0	1	0	0	0	0	0	0	0		1250
0	0	0	0	1	0	0	0	0	0	0		2500
0	0	0	0	0	1	0	0	0	0	0		5000
0	0	0	0	0	0	1	0	0	0	0		10000
0	0	0	0	0	0	1	1	0	0	0		5555.6
0	0	0	0	0	0	1	0	1	0	0		7142.9
0	0	0	0	0	0	1	0	0	1	0		8333.3
0	0	0	0	0	0	1	0	0	0	1		9090.9
0	0	1	0	1	0	1	0	0	0	0		666.7
1	1	0	0	0	0	0	0	0	0	0		166.7

c) If there is no output waveform check 2IC1. If the frequencies are wrong check that the switches change the logic levels on the "jam" inputs of 2IC1.

7.4 To check the VCO and 9/10 bit divider

a) Short 2IC4 pin 9 to 0 volts then connect the frequency counter and oscilloscope to 2IC3 pin 10 and pin 14 in turn. Set U-Link to 6mS. Check the frequency and amplitude of the waveform at both points. Remove the short.

b) The waveform at both points should be a square wave between 0 and +15 volts. The frequency at pin 10 should be 110 ± 20kHz. The frequency at pin 14 should be a 512th of the frequency at pin 10. Set the U-link to 12mS. The frequency at pin 14 should now be a 1024th of the frequency at pin 10.

c) If the amplitude of the waveform is wrong check 2IC3 and 2IC4. If the frequency at pin 10 is wrong check 2R16, 2R17 and 2C7. If the division ratio is not 512/1024, check 2IC3.

7.5 To check the phase locked loop

a) Connect the frequency counter to 2IC2 pin 6.
Set the switches to the positions shown in the last two lines of table 1 and set the 'U' link to 6mS (section 7.3), in turn.
Check the frequency for each setting.

b) The frequencies should be 682667 ± 68Hz and 170667 ± 17Hz respectively.

c) If one frequency is incorrect the VCO range may need adjustment (see section 7.6). If both frequencies are incorrect check the loop filter components 2R13, 2R14 and 2C3 as well as the phase detector 2IC4.

7.6 To check the VCO range and loop stability

a) Connect the oscilloscope to the VCO control input 2IC4 pin 9 and measure the voltage with the switches set as in section 7.5.

b) Both voltages should be within the range +1 volts to +12 volts. The voltage levels will take up to 5 seconds to settle but after this time there should be negligible a.c. ripple.

c) If one of the voltages is incorrect 2R6 should be adjusted to bring the voltages well within the specified range. If the d.c. voltage has an undamped a.c. ripple superimposed on it, check the loop filter components.

7.7 To check the frequency response

a) Set the switches to the settings shown in the last two lines of table 1 (section 7.3), in turn. Connect the A.C. Test Set oscillator (600Ω source, internal 600Ω termination and 0dBm) to pins 2 and 3. Connect the A.C. Test Set detector (high impedance, mean indication) to pins 12 and 13. Measure the frequency response.

b) The gain should be constant within ±0.5dB from 100Hz to 6.5kHz. The loss should be greater than 20dB at 15 and 10KHz relative to the level at 1kHz.

c) If the frequency response is incorrect check the input and output active filter components. Also, use a high impedance probe to check the response at the output of each operational amplifier in order to isolate the fault.

7.8 To check the distortion

a) Leave the equipment set up as in section 7.6 but increase the output from the oscillator to +8dBm and set it to 1kHz. Press the "mean" button and adjust the attenuator setting to obtain a centre reading on the meter. Then press the "1kHz harmonic" button and readjust the attenuator to obtain a centre reading. Note the difference between the two attenuator settings.

b) The difference should be greater than 50dB for both delay settings.

c) If this test does not meet the specification go to section 7.9 otherwise go to section 7.11.

7.9 To set the d.c. bias level (only if unit has failed section 7.8)

a) Leave the equipment set up as in section 7.8 but increase the output from the oscillator until clipping occurs on the UN14/12 output (use the oscilloscope to view the waveform). Adjust 1R12 to obtain equal clipping on positive and negative peaks.

b) The clipping should only appear at an input level greater than +11dBm.

c) If clipping occurs at a lower level it could be due to the two "bucket brigade" IC's (1IC4 and 1IC5) requiring very different bias levels. Therefore view the outputs from 1IC4 and 1IC5 to check that they limit at approximately the same input level and if they do not adjust 1R12 to a compromise setting.

7.10 To set the input gain control (only if unit has failed section 7.8)

a) Repeat section 7.8 but adjust 1R7 to reduce the harmonic separation.

b) Set 1R1 for a 51 $\pm$ 1dB harmonic separation.

c) If this figure cannot be obtained check the other amplifier stages.

7.11 To set the output gain control

a) Set up the equipment as in section 7.6 and adjust 1R30 to set the output level.

b) The output level should be 0 $\pm$ 0.5dBm for both delay settings (i.e a gain of 0 $\pm$ 0.5dB).

c) If 1R30 requires a very large adjustment 1IC4 or 1IC5 are probably faulty, resulting in excessive input attenuation to obtain the required distortion.

7.12 To measure the signal to noise ratio

a) Leave the equipment set up as in 7.11 and press the TPM button. Check that the TPM indicates 4 when the attenuator is a 0dB. Replace the

oscillator with a 600Ω resistor, press the "weighted" button and readjust the attenuator to make the TPM peak to 4. Note the new attenuator setting.

b) The reading should be better than 50dB (i.e. 50dB4w)

c) If this figure cannot be obtained 1IC4 or 1IC5 are probably faulty.

Δ45389A4

SHEET 1 OF 8 SHEETS.

ISS.	CHANGE

ITEM No.	No. OFF	DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
		DRAWING NUMBERS		
		CIRCUIT Δ45388A1		
		PARTS LIST Δ45389A4		
		ASSY & WIRING Δ45390A2		
		DETAILS Δ45391A2		
		P.B WIRING N°1 Δ45392A2		
		" " " (COMP SIDE) Δ45393A2		
		P.B N°1 COMP LOC Δ45394A3		
		" " DRILLING. Δ45395A3		
		P.B WIRING N°2 Δ45396A2		
		" " " (COMP SIDE) Δ45397A2		
		P.B N°2 COMP LOC Δ45398A3		
		" " DRILLING. Δ45399A3.		
		FURTHER INFORMATION REQUIRED FOR MANUFACTURE :		
		ASSY INFORMATION E.A 10484		
		WIRING INFORMATION E.A 10140		
1.	1	CHASSIS, CH/6SA, TO BE MODIFIED BY CONTRACTOR AS FOLLOWS :-		
		FRONT PANEL		Δ45391A2 DET 1
		CODING PLATE		" DET 3
		HANDLE		" DET 4
2.	1	PRINTED BOARD N°1		Δ45392A2, Δ45393A2 Δ45394A3, Δ45395A3
3.	1	PRINTED BOARD N°2		Δ45396A2, Δ45397A2. Δ45398A3, Δ45399A3.
4				
5				
6	12	SCREW, M2·5 x 6LG PAN HD MS Zn P		
7				
8				
9	4	IC SOCKET, 8 PIN, TEXAS TYPE C93082.		
10				
11	1	LINK, FREE MINIATURE, SHORTING, RED.	Lk 2	S-23790 - 0223319.
12	3	SOCKET, FIXED SINGLE POLE MINIATURE		S-27611 - 0236252.
13				
14.				

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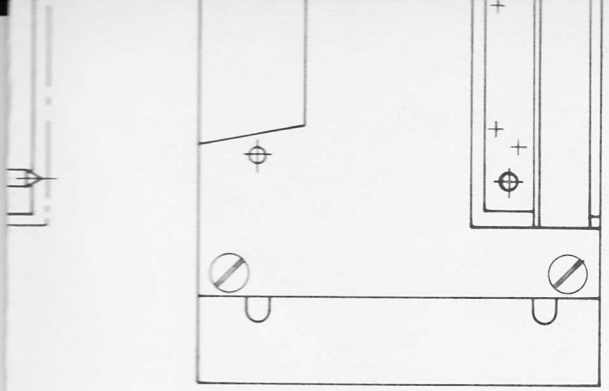
DS/PLA4

UN14/12, PARTS LIST
AUDIO DELAY UNIT.

DRN.	K. TURNER	DESIGNS DEPARTMENT.
TPD.		
CKD.		Δ45389A4
APPD.	GB	SHEET 1 OF 8 SHEETS



THROUGH HOLE PLATED BOARD, ALL LEADS PASSING THROUGH BOARD NOT TO BE BENT AFTER ASSEMBLY

CAUTION
CMOS IC DEVICES FITTED, HANDLE WITH CARE. SEE EA10140 NOTE 14.

NOTES

1 ASSEMBLY TO BE IN ACCORDANCE WITH DRAWING EA10484 NOTES 1,4,6,7

2 WIRING TO BE IN ACCORDANCE WITH ~~DRAWINGS EA10137 NOTES & EA10139 NOTES~~

3 COMPONENTS TO BE WIRED TO PRINTED BOARD IN ACCORDANCE WITH DRAWING EA10140 NOTES 1,4,11,13

4 THE COUNTERSUNK HOLES IN THE FRONT PANEL AND HANDLE MUST HAVE THE ANODISED FINISH REMOVED BEFORE ASSEMBLY

5. * DENOTES EXISTING WIRE. ALL OTHER WIRE TO BE PUN1/1M IN COLOUR SHOWN.

6. CODING PINS OF PLUG (ITEM 173) TO BE SET IN POSITIONS AS SHOWN PRIOR TO MOUNTING OF PLUG TO BOARD, FOR METHOD OF CODING SEE DSk 17963 44.

PARTS LIST D 45389 A4
CIRCUIT D 45388 A1.

THIRD ANGLE PROJECTION

All dimensions in millimetres unless otherwise stated:

Normal tolerances	
no decimal place:–	±1 mm
one decimal place:–	±0.3mm
two decimal places:–	±0.1mm
unless otherwise stated	

UNI4/12

ASSEMBLY & WIRING

DRN.	TCD.	CKD.	APPD.
K. TURNER			GR

DESIGNS DEPARTMENT

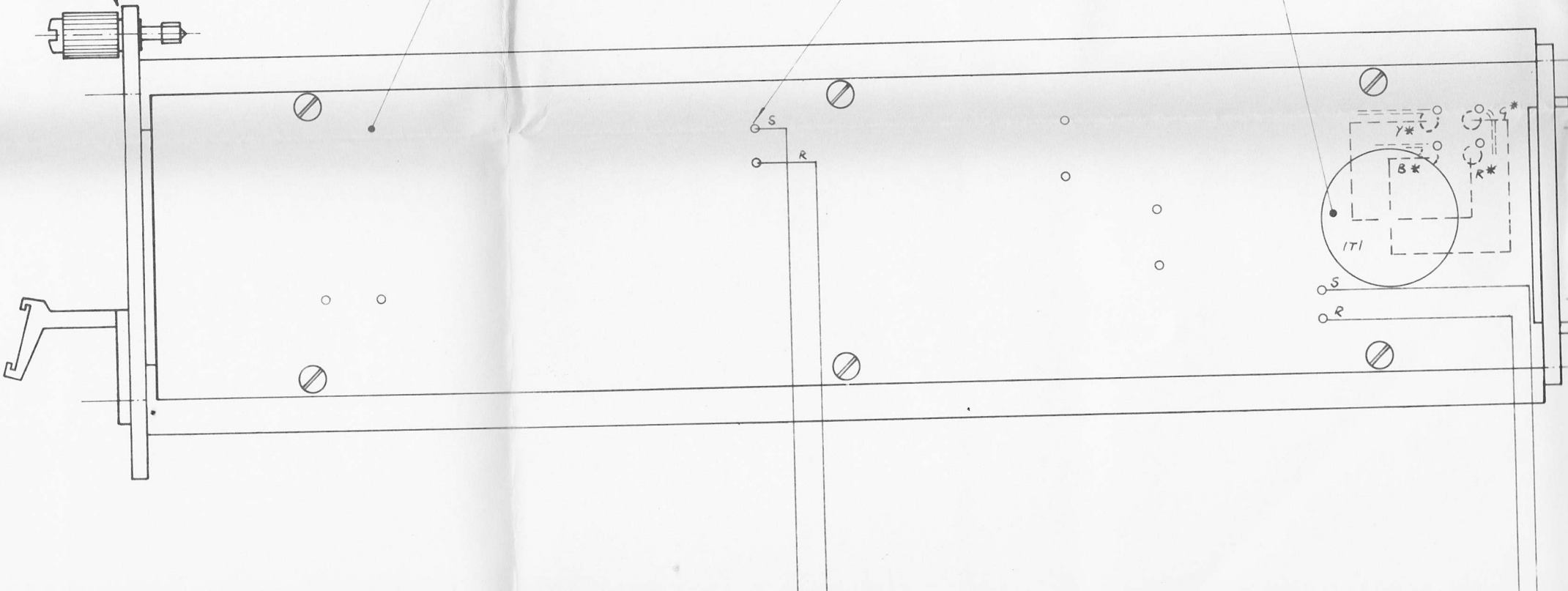
D 45390 A2

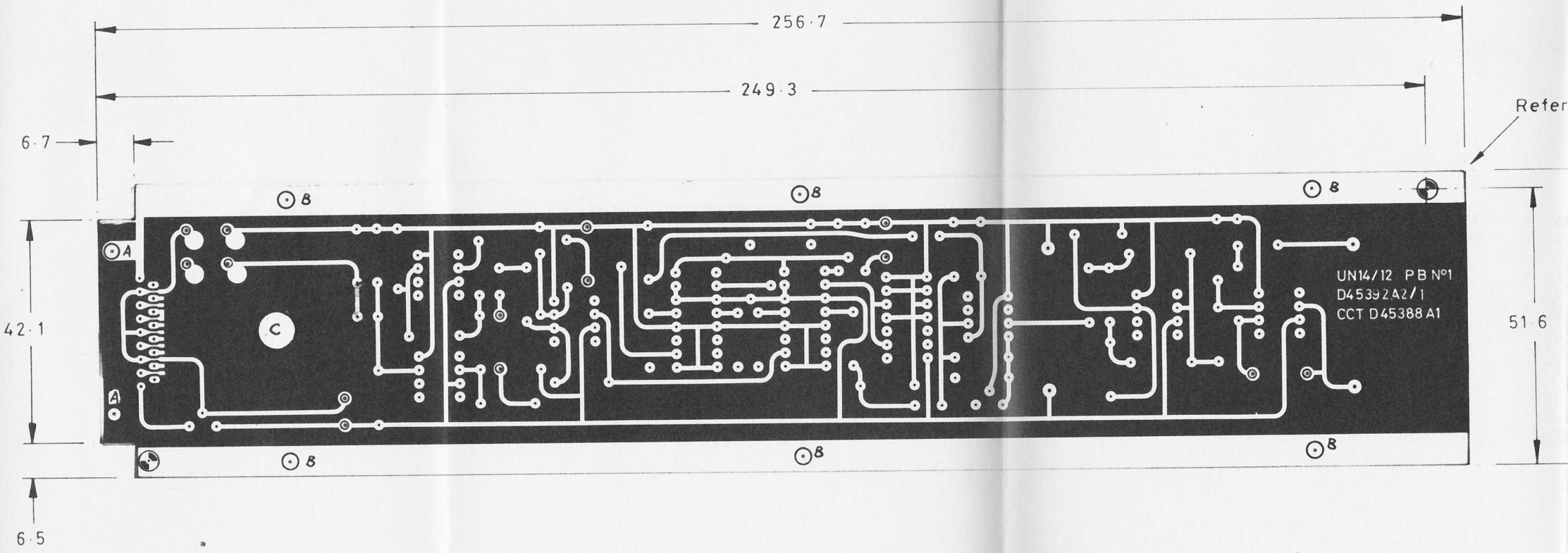
WASHER TO BE FITTED BETWEEN
KNOB & PANEL FRONT

(2)(6) FOR COMPONENT CONFIGURATION SEE DRAWING D45394 A3

(101) IN 14 POSITIONS TO PROJECT ON COMP SIDE OF BOARD.

(152)

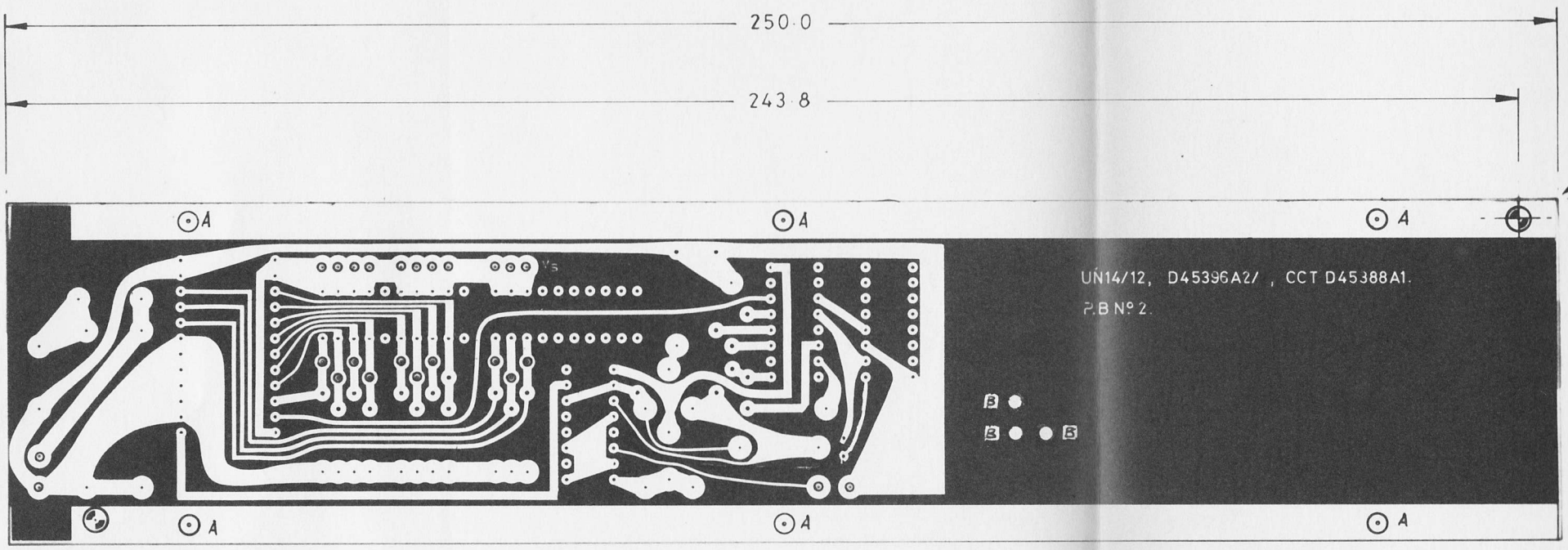




TRIM BOARD TO DIMENSIONS SHOWN

MATERIAL : 1·6 THK TO BS 4584 + CL 5·2 EP-GC-CU-3, 35/35 1 60 $\pm$ 0 20

D45399A3.



TRIM BOARD TO DIMENSIONS SHOWN

MATERIAL : 1·6 THK. TO BS 4584, + CL 5·2, EP-GC-CU-3, 35/35 1·60 +/−