Issue 1
30.8.77

DESIGNS DEPARTMENT MANUFACTURING INFORMATION

No.6.308(77)

Variable Frequency Oscillator OS3/10

.....J.O'Clarey.....
(J.W.H. O'Clarey)

Written by: M.T. Ellen

BBC

DS/SPA4

JW

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Variable Frequency Oscillator OS3/10

C O N T E N T S

D R A W I N G S

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Variable Frequency Oscillator OS3/10

1. INTRODUCTION

This unit has been designed for use as part of a voice frequency telephone signalling system. It can be set to generate a single continuous tone within the range 450 to 2000Hz. The output frequency is derived from a crystal oscillator operating at 4MHz and it therefore has a high long term frequency stability.

The output frequency is set by means of internal links and no test equipment is needed when resetting the frequency.

All the standard signalling frequencies may be set within a tolerance of 0.16%.

2. SPECIFICATION

Performance Data

Frequency range:	450 to 2000Hz approx.
Frequency increments:	Variable between 1Hz at low frequencies and 18Hz at high frequencies.
Output level:	0dBm from pins 2 and 6 into 600 ohms. -6dBm from pins 2 and 4 into 600 ohms (may be set to lower level if required).
Output level variation with frequency:	±1dB without resetting output level control.
Harmonic outputs:	Better than -30dB.
Frequency stability:	±2 ppm/volt supply voltage variation. ±10 ppm ageing over first year. ±100 ppm 0 to 40°C.

Mechanical Data

Chassis:	CH1/65J
Weight:	0.2kg

Installation Data

Power requirements:

Either	pin 9 -ve and pin 11 +ve	32V to 53 volts at 60±10mA
or	pin 9 -ve and pin 13 +ve	13V to 35 volts at 60±10mA
or	pin 9 -ve and pin 15 +ve	11.5V to 13 volts at 60±10mA

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Note 1: remove LK1 when pin 15 is used.

Note 2: power supply may be floating, positive earth or negative earth.

Index pins: 1, 7 and 12.

Chassis Extender: CH1A/45

Frequency Setting: The frequency is set by means of 10 links numbered 1 to 10. Link 10 is the most significant bit (MSB) and the linked condition is logic 0.

$$S = 1024 - \text{integer part of}\left(\frac{222222.2}{(\text{Output frequency in Hz}} + 0.5\right)$$

where S is the decimal equivalent of the binary number to be set on the frequency setting links.

Actual output frequency: $\frac{222222.2}{1024 - S}$ Hz

Settings for standard frequencies:

Nominal frequency Hz	Link settings 10 9 8 7 6 5 4 3 2 1	Actual frequency Hz	Error %
450	1 0 0 0 0 1 0 0 1 0	449.84	.035
600	1 0 1 0 0 0 1 1 1 0	600.60	.1
700	1 0 1 1 0 0 0 0 1 1	701.02	.145
777	1 0 1 1 1 0 0 0 1 0	777.00	.0001
860	1 0 1 1 1 1 1 1 1 0	861.33	.154
1900	1 1 1 0 0 0 1 0 1 1	1899.34	.035

Output filter settings: Four links control the cut-off frequency of a low pass filter. The links should be in position for frequencies below 950Hz.

Output connection: 0dBm from PLA2 and 6 into 600 ohms. -6dBm from PLA2 and 4 into 600 ohms.

Earth connections: PLA1, 3, 5, 7 and 17.

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DESIGNS DEPARTMENT MANUFACTURING INFORMATION NO.6.308(77)

Variable Frequency Oscillator OS3/10

PRODUCTION TEST SCHEDULE

1. Description

This oscillator can be set to generate a single continuous tone within the range 450 to 2000Hz. The output frequency is derived from a 4MHz crystal oscillator whose output is divided in frequency to give the required voice frequency output. IC1 divides by 3, and IC2, IC3 and IC4 divide by a number which may be programmed by wire links, then the signal is split into two paths. The first path passes through IC5 (divide-by-3) then half of IC6 (divide-by-2) and the second path passes through the other half of IC6 (divide-by-2). The output of the second path is the third harmonic of the first path output and the two signals are differenced in R14 to produce a waveform with a low third harmonic content. The signal is then filtered and amplified to produce a sine wave at OdBm.

2. Information

a)	Design Section:	Transmission Section, D.D.
b)	Designer:	M.T. Ellen
c)	Engineer responsible:	M.T. Ellen
d)	Handbook:	Not available 1/8/77.
e)	Technical Instruction:	Not available 1/8/77.
f)	Other Information:	None.
g)	Pre-Production batch:	This P.T.S. has not been tested on a pre-production batch.

3. Manufacturing Performance Specification

a)	Input requirements:	None.
b)	Output level:	OdBm from PLA2 and 6 into 600 ohms. -6dBm from PLA2 and 4 into 600 ohms. (May be set to lower level if required.)
	Output frequency range:	450 - 2000Hz approx.
	Output frequency:	$\frac{222222.2\text{Hz}}{1024 - S}$ where S = decimal equivalent of binary number set on the frequency setting links.

c) Power requirements: Either 12±.5 volts PLA15 (+ve) and PLA9

or 13 to 33 volts PLA13(+ve) and PLA9

or 32 to 53 volts PLA11 (+ve) and PLA9

at 60±10mA

d) Performance:

Output level variation with frequency setting: Better than ±1dB without resetting output level control.

Output frequency stability: Better than ±1Hz from 0 to 40°C over the specified voltage range.

4. Warning

No voltages above 50 volts d.c. or 30 volts a.c. are connected to this unit.

5. Test Apparatus Required

PSU variable from 0 to 60 volts, current limited to 100mA.

General purpose oscilloscope - Grade II.

Digital voltmeter, 0.1% accuracy.

Frequency counter 5MHz.

AC test set EP14/1.

6. Inspection Checks

a) Check for overall mechanical defects. In particular check that the voltage regulator IC8 is correctly mounted on its heat sink bracket (detail 4).

b) The OS3/10 does not contain any mains wiring. Check that the transformer T1 has been mounted and wired correctly.

c) Check that the following components are correctly orientated by ensuring that they conform with either the board legend or D 41673 A3.

Capacitors C1 to C15
Resistors R1 to R27
Diodes D1 and D2
Transistors TR1 to TR4
Integrated circuits IC1 to IC8
Crystal oscillator XL1
Fuse FS1
Test points TP1 and TP2
Plugs PLA

7. Test Procedure

7.1 To Check Current Consumption and 5 Volt Regulator

a) Remove LK15 and connect a variable PSU (set to 0 volts and 100mA current limit) to PLA15 (+ve) and PLA1 and 9 (-ve). Gradually increase the voltage to 12 volts while monitoring the current. Also use a DVM to observe the voltage across D1.

b) Check that the current drawn is 60±10mA and that the voltage across D1 is 6.8±0.2 volts.

c) If the current consumption is not within the specification remove R12 and the current should fall to 5±2mA. If it does the fault is in the oscillator and divider part of the circuit; if it does not the fault is in the filter and amplifier part of the circuit. If the voltage across D1 is incorrect check R12 and D1.

7.2 To Check the Crystal Oscillator

a) With an oscilloscope observe the signal on IC1 pin 5 then connect this point to a frequency counter.

b) The signal should be a squarewave with a negative peak less than +1.4 volts and a positive peak more than +3.5 volts with respect to IC1 pin 8 (0 volts). Its frequency should be 4MHz±500Hz.

c) If the amplitude is wrong disconnect the crystal oscillator output from IC1 pin 5 and measure the oscillator output. If it now meets the specification IC1 is at fault, otherwise the crystal oscillator is at fault.

7.3 To Check IC1 Divide-By-3 Circuit

a) Use an oscilloscope and counter to check the signal on IC2 pin 2, IC3 pin 2 and IC4 pin 2.

b) The logic levels should be 1.4 volts and 3.5 volts and the frequency should be 1.333333MHz±200Hz.

c) If the logic levels are wrong disconnect pin 2 of IC2, 3 and 4 then if the levels are still wrong the circuit associated with IC1 is at fault. If the frequency is wrong check the connections to the data and load inputs of IC1.

7.4 To Check the Programmable Divider Circuit

a) Connect links in the following positions 1, 3, 4, 6, 7, 8 and 9, and observe the signal at IC5 pin 5 with an oscilloscope and counter. Then reconnect the links in the following positions 3, 5, 6 and 7 and observe the waveform at the same point.

b) The waveform should be a negative going pulse with a duration of of 750±50nS with logic levels of 1.4 volts and 3.5 volts. The frequency should be 2699±2Hz and 11396±2Hz for the two link settings respectively.

c) If this test is not passed remove R13, this should set the frequency

to 325±1Hz. If it does check the connections to IC7 then replace R13 with a 20K variable resistor and adjust it until test 7.4 b) is passed then replace it with the nearest preferred fixed resistor value. If the output frequency does not go to 325±1Hz when R13 is removed then disconnect IC5 pin 5 and IC6 pin 3 to isolate the fault to either IC2, 3 and 4 or IC5 and 6.

7.5 To Check IC5 Divide-By-3 Circuit

a) Connect links in the following positions (as in test 7.4) 3, 5, 6 and 7 and observe the signal in IC6 pin 11.

b) The waveform should have logic levels of < 1.4 volts and > 3.5 volts. Its frequency should be 3799±1Hz.

c) If the logic levels are wrong disconnect IC6 pin 11 and check IC5 pin 11. If the waveform is now correct the fault is associated with IC6 otherwise check IC5. If the frequency is wrong check the connections to the data and load inputs of IC5.

7.6 To Check IC6 Divide-by-2 Circuits

a) Connect links in the following positions (as in tests 7.4 and 7.5) 3, 5, 6 and 7 and observe the waveform on IC6 pins 9 and 12 in turn.

b) The waveform should have logic levels of ≤ 0.2 volts above PLA9 and ≤0.2 volts below IC6 pin 14. The frequencies should be 1889±1Hz and 5698±1Hz respectively.

c) If the logic levels are not correct check the value of R14 and adjust it to approximately its mid position. If the test is still not passed check the circuit associated with IC6.

7.7 To Minimise Third Harmonic Output

a) Connect links in the following positions (as in test 7.6) 3, 5, 6 and 7. Check that links are not in positions 11, 12, 13 and 14. Use an oscilloscope to observe the waveform at the emitter of TR3 and adjust R14 to obtain a sinewave.

b) The frequency of the waveform should be 1899±1Hz and suitable adjustment of R14 should minimise the third harmonic distortion.

c) If the waveform distortion is not affected by R14 it is probable that the filter cut-off frequency is too low (should be 3dB down at 2.6kHz) so check all the filter components. If the waveform contains very much distortion (worse than -30dB) then it is probable that the filter cut-off frequency is too high.

7.8 To Set Output Level

a) Connect links in the following positions (as in test 7.8) 3, 5, 6 and 7. Check that links are not in positions 11, 12, 13 and 14. Use an oscilloscope to observe the waveform at the collector (can) of TR4 and connect an EP14/1 (set to 600 ohms I/P impedance) to PLA2 and 2. Adjust the output level to OdBm with R24.

b) The waveform should be a sinewave without clipping of either peak.

c) If either peaks are clipped replace R15 with a 50K potentiometer and adjust it to a central position where no clipping occurs then replace it with the nearest preferred fixed value and readjust the output level.

7.9 To Check Output at Minimum Frequency

a) Connect links in positions 1, 3, 4, 6, 7, 8, 9, 11, 12, 13 and 14. Use an oscilloscope to observe the waveform at the collector of TR4 and use an EP14/1 to measure the output level at PLA2 and 6½

b) The waveform should be approximately sinusoidal with no peak clipping and the output level should be 0±1dBm.

c) If this test is not passed check C5, C8, C9 and C11.

7.10 To Check the Output Attenuator

a) Use an EP14/1 to measure the output level at PLA2 and 4. (R26 and R27 should be determined by the output level required by the customer).

b) The output level should meet the customers requirements.

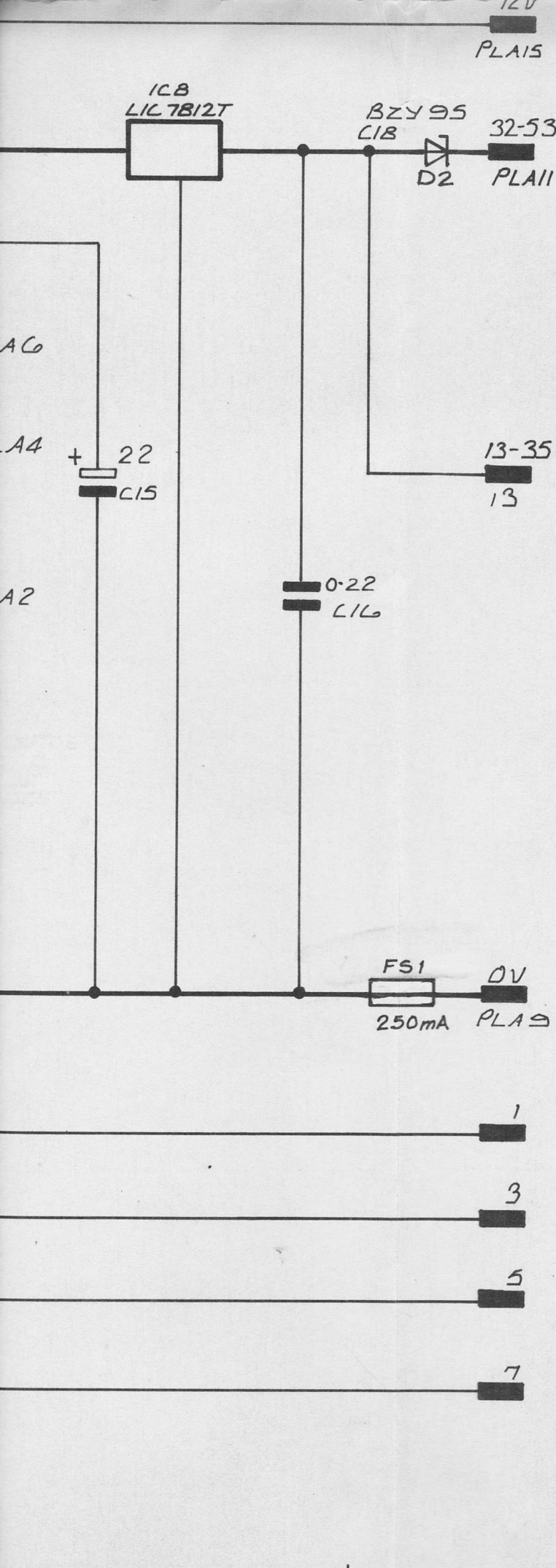
c) If an accurate output level is required R24 may be used to provide +0, -2dB variation.

7.11 To Check the 12 Volt Regulator

a) Reconnect the PSU to PLA9 and 1 (-ve) and PLA11 (+ve). Connect LK15 and monitor the voltage across PLA9 (-ve) and PLA15 (+ve) with a DVM. Adjust the PSU from 0 volts to 53 volts.

b) The voltage at PLA15 should be 12±0.5 volts when the PSU is set in the range 32 to 53 volts.

c) If this test is not passed check IC8 and C18.



THIRD ANGLE PROJECTION

All dimensions in millimetres unless otherwise stated:

Normal tolerances

no decimal place:–	±1 mm
one decimal place:–	±0.3mm
two decimal places:–	±0.1mm

unless otherwise stated

DS3/10 VARIABLE FREQUENCY OSCILLATOR

DRN.	TCD.	CKD.	APPD.
J L S		M.T.E	M.T.E

DESIGNS DEPARTMENT

D41668 A1

D41669A4 SHT. 1 OF 8 SHTS.

ISS. 1

CHANGE 26_1_78

OS3/10. VARIABLE FREQUENCY OSCILLATOR PARTS LIST.

ITEM No.	No. OFF	DESCRIPTION		C'C'T REF.	BBC REF. OR DRG. No.
		DRAWING NUMBERS			
		CCT	D41660B A1		
		P/LIST	D41669 AA		
		ASSY	D41670 A2		
		PB WIRING	D41671 A2		
		PB WIRING COMPSIDE	D41672 A2		
		PB COMP LOC	D41673 A3		
		PB DRILLING	D41674 A3		
		DETAILS 1-3	D41675 A3		
		DETAIL 4	D41825 A3		
		FURTHER INFORMATION REQ° FOR MANUFACTURE			
		UNIT ASSY INFORMATION	EA10484		
		UNIT WIRING INFORMATION	EA10140		
1	1	CHASSIS CH1/60SJ MODIFIED AS FOLLOWS:-			
		FRONT PANEL			D41675A3 DET 1
		CODING PLATE			" 2
		HANDLE			" 3
2	1	HEAT SINK			D41825 A3 " 4
3					
4					
5	1	PRINTED BOARD			D41671 A2, D41672 A2, D41673A3 & D41674A3.
7	95	PINS SEALECTRO A0013619G/T			0239333
8	34	PINS SEALECTRO A0013620G/T			0239341
9					
10					
		FIXINGS	FOR FIXING:-		
		SCREWS			
11	6	M2·5x 6 LG PAN HEAD M/S ZN PL	5 & 2		
12	1	M2·5 x 10 LG PAN HEAD M/S ZN PL	147		
13					
		WASHERS			
14	4	M2·5 PLAIN M/S ZN PL	5		
15	2	M2·5 SHK. PRF. MS Z/N PL	2		
16					
		NUTS			
17	1	M2.5 HEX. FULL M.S ZN. PL.	147		

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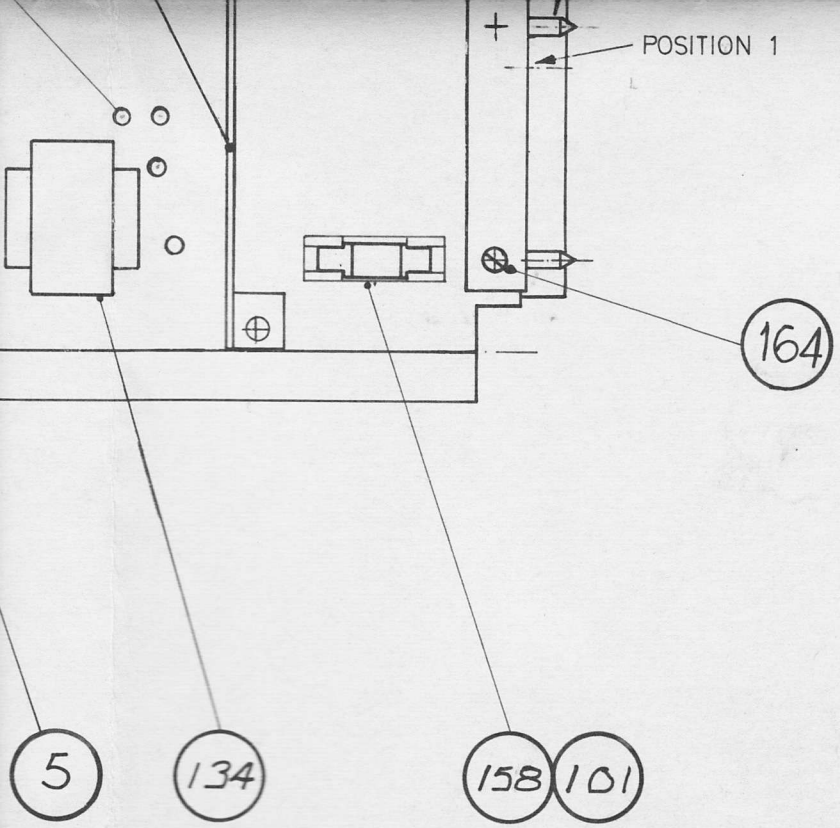
DS/PLA4

OS3/10 VARIABLE FREQUENCY OSCILLATOR, PARTS LIST.

DRN. JLS
TPD.
CKD. M.T.E
APPD.

DESIGNS DEPARTMENT

D41669 AA
SHT. 1 OF 8 SHTS



CAUTION
CMOS IC DEVICES FITTED,
HANDLE WITH CARE.
SEE EA10140 NOTE 14.

OVERALL DIMENSIONS
LENGTH 290
WIDTH 27
HEIGHT 86

PARTS LIST D 41669 A4
CIRCUIT D 41668 A1

THIRD ANGLE PROJECTION

All dimensions in millimetres unless otherwise stated.

Normal tolerances

no decimal place	± 1 mm
one decimal place	± 0.3mm
two decimal places	± 0.1mm

unless otherwise stated

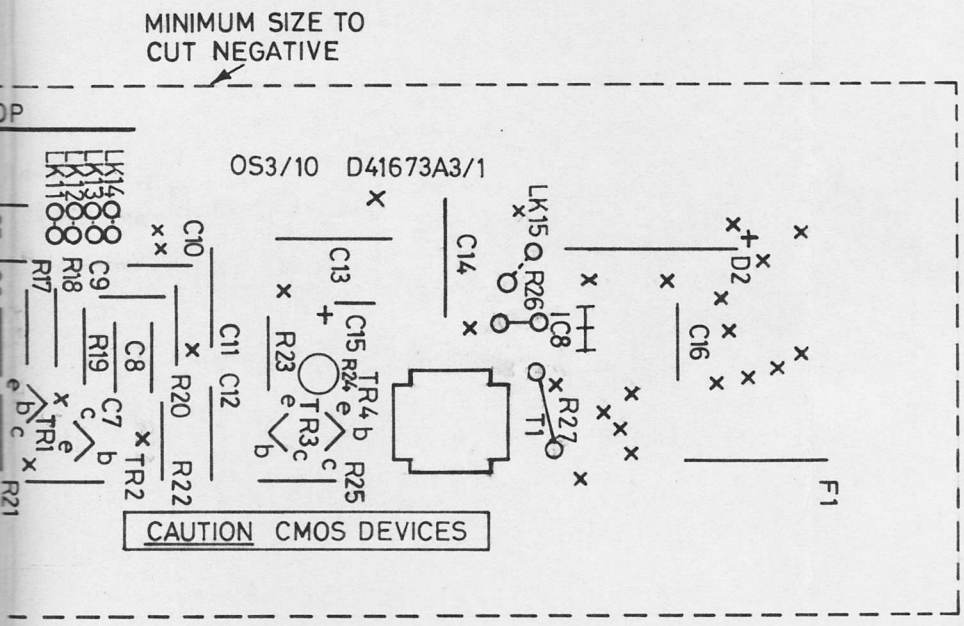
OS3/10
ASSEMBLY

DRN	TCD	CKD	APPD
JLS		M.T.E	M.T.E

DESIGNS DEPARTMENT

D 41670 A2

CHANGE	ISS
26_1_77	1



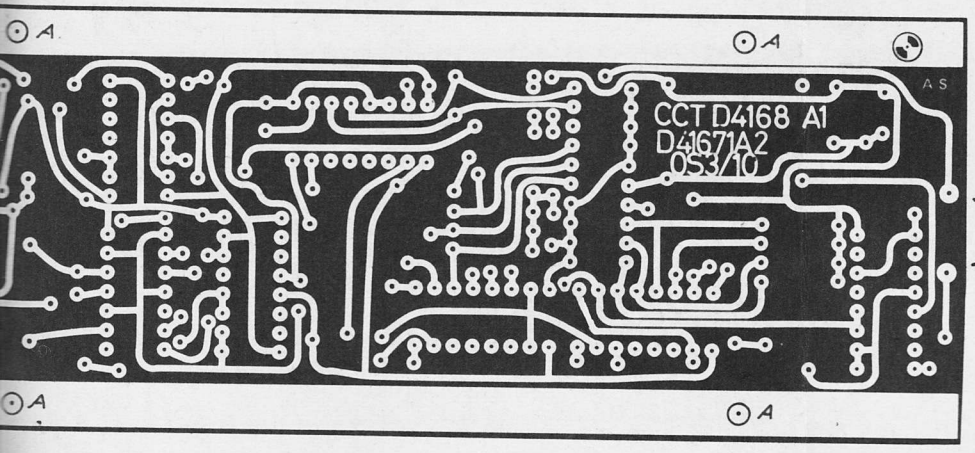
S TO BE PRINTED ~~WHITE~~ / BLACK
EVERSE SIDE OF BOARD IS D41675A3

SCALE 1:1

IT LOCATION.

DRN.	J L S	DESIGNS DEPARTMENT
TCD.	JC	D41673 A3
CKD.	M.L.E	
APPD		

CHANGE	ISS
26—1—78	1



TO BS4584, +CL5·2, EP-GC-Cu-3,
6±0·20 (EPOXIDE WOVEN GLASS
CLAD ON [redacted]/BOTH SIDES
5µm THK. COPPER)

TO D41671 A2 D41672 A2 & D41673 A3

NNED.

SCALE

DRILLING.

DRN	JLS	DESIGNS DEPARTMENT.
TCD		
CKD	M.T.E	D41674 A3
APPD		

Original Frame Size 277mm · 400mm

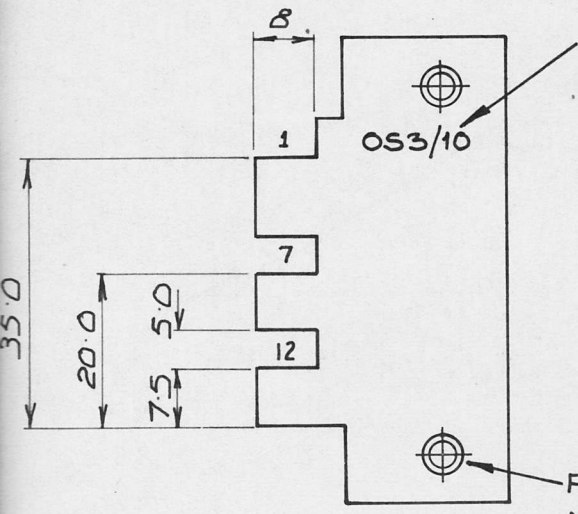
BBC

CH1/65J

BMM112A3

CHANGE	ISS
26—1—78	1

FOR BBC REF ONLY
SLOT POSITIONS ARE
NOS 1, 7. & 12.

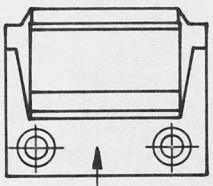


SIGNWRITE CODE IN 3 HIGH CHARS.

FOR BBC REF ONLY. AFTER NOTCHING C'SINK 2 HOLES 90° TO 5·0 DIA. ENSURE CORRECT ORIENTATION OF NOTCHES TO C'SUNK HOLES.

DETAIL 2 CODING PLATE
MATERIAL PART OF CH6/65J CHASSIS
FINISH CLEAN

D41675 A3



SERIAL N° TO BE STAMPED IN 2·5 HIGH CHARACTERS CENTRALLY DISPOSED BETWEEN FIXING HOLES ON THIS SURFACE

DETAIL 3 HANDLE
MATERIAL PART OF CH1/65J CHASSIS
FINISH AS SUPPLIED

D41675 A3

PARTS LIST D41669 A4

THIRD ANGLE PROJECTION

All dimensions in millimetres unless otherwise stated.

Normal tolerances	
no decimal place	±1 mm
one decimal place	±0.3mm
two decimal places	±0.1mm

unless otherwise stated

OS3/10 DETAILS 1, 2, & 3.

DRN	TCD	CKD	APPD
JLS		M.T.E	M.T.E

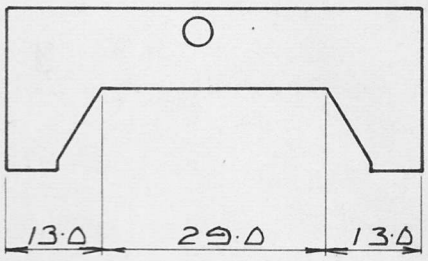
DESIGNS DEPARTMENT

D41675 A3

Original Frame Size
277mm × 400mm

BBC
DS/A3

CHANGE	ISS
26—1—78	1



EARENCE

MATERIAL: 16 SWG ALLUMINIUM ALLOY

FINISH: CLEAN

THIRD ANGLE PROJECTION

All dimensions in millimetres unless otherwise stated:

Normal tolerances	
no decimal place:–	±1 mm
one decimal place:–	±0.3mm
two decimal places:–	±0.1mm
unless otherwise stated	

053/10
DETAIL
4

DRN.	TCD.	CKD.	APPD.
JLS		M.T.E	M.T.E

DESIGNS DEPARTMENT.

D41825 A3

APPLICATION FOR EQUIPMENT CODE AND DESIGNATION

Please complete Section A when applying for a Code and send form to Drawing Office Manager, Room 408, Western House. Section C will be completed by the Drawing Office and the form returned to you. You should complete Section B when the design of the coded item is complete.

C.A. No. 7751

Code ~~OS2/47~~ OS3/10

A **From** M.T.ELLEN **Department** DESIGNS

To: H.D.D. (Attn. Drawing Office Manager) **Date** 29/9/76

Will you please allocate a code and designation to the following apparatus in accordance with D.D. Specification No. 4.16(65) – Guide to Coding of Equipment:–

Suggested code OS3/ Suggested Designation OSCILLATOR, VOICE FREQUENCY

(1) Function and Description (This information will form initial entry in R.D. and C.E.)

This oscillator has been designed for use as a voice frequency ringing oscillator to replace the OS2/33. It may be set to produce any integer submultiple of 222222·2 Hz between 450 and 2000 Hz by means of wire straps on the PCB. The output level may be adjusted up to a maximum of 1mW into 600Ω, and the frequency ~~stability~~ accuracy is determined by a temperature compensated crystal oscillator. Front panel monitor sockets are provided.

(2) Other relevant information, including mechanical details affecting coding (e.g. L- or M-codes)

CH1/65J

B **Please complete this section when job is completed and send form to Liaison Engineer, Designs Department**

(1) Function and Description

(2) Other relevant details

(3) Principal coded items within apparatus, if any. (Give codes only) .....

.....

(4) Proposed first use as sub-unit in (code) .....
(designation) .....

(5) Chassis type (or size/construction) .....

Indexing positions ..... Weight (if relevant) .....

Power requirements: mains supply/internal battery/powered by parent equipment/ separate supply requires as follows:-

(6) D.D.M.I. No ..... Handbook No .....

C **This section to be completed by Drawing Office, Designs Department, and form returned to applicant**

Allocated Code ~~OS2/47~~ OS3/10 Designation OSCILLATOR, ~~FIXED~~ VARIABLE FREQUENCY

E/681. Signature ..... Date 30 SEP 1976