DESIGNS DEPARTMENT MANUFACTURING INFORMATION

No. 6.294(77)

U.H.F. Flat Delay. Line Equaliser

EQ4/22

Written By. M.T. Ellen

J.W.H. O'Clarey

(J.W.H. O'Clarey)
for Head of Designs Department

D.D.M.I. No. 6.294(77)
Title Sheet

BBC

DS/SPA4

Issue 1
27.7.77

DESIGNS DEPARTMENT MANUFACTURING INFORMATION

No. 6.294(77)

O.B. Flat Delay, Line Equaliser

EQ3/33

C O N T E N T S

D R A W I N G S

Issue 1
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DESIGNS DEPARTMENT MANUFACTURING INFORMATION

No. 6.294(77)

O.B. Flat Delay, Line Equaliser

EQ3/33

Introduction

This unit may be set to give a differential delay between two audio signals that are passed through it. If the front panel selector switch is set to "bypass" the inputs are connected directly to the outputs, in the other positions each signal passes through a separate audio delay circuit. One of the delay circuits may be set to a delay within the range 500 µs to 5,500 µs while the other is set to 500 µs, thus giving 0 to 5 ms differential delay. The front panel selector switch allows the variable delay to be in either channel A or channel B, and code switches on the front panel control the variable delay. The code switches indicate the differential delay.

Specification

Performance data

Inputs

A channel input	unbalanced
A channel input impedance	600 Ω
A channel input level	zero programme volume (+8dBm max.)
B channel	same as A channel
Power consumption	+12 ± 0.4 volts at 0.16 ± 0.02 Amps. -12 ± 0.4 volts at 0.12 ± 0.02 Amps. + 5 ± 0.1 volts at 0.8 ± 0.1 Amps.

Outputs

A channel output	unbalanced
A channel output impedance	600 Ω
A channel output level	zero programme volume.
B channel	same as A channel
Differential Delay Range	0 to 5,000µs
Differential Delay Increments	10 µs
Delay tolerance	± 0.06% between 10 and 50°C
Frequency response (each channel)	+0.2 dB to -0.8 dB relative to the gain at 1 KHz over the range 100 Hz to 13 kHz.

Maximum difference in gain between channels at 1 kHz.	1.5 dB
Maximum difference in frequency response of each channel assuming equal gain at 1 kHz	0.3 dB
Total harmonic distortion (0 dBm 1 kHz input)	
minimum delay	better than -42 dB
Maximum delay	better than -60 dB
Signal to Noise Ratio	
Minimum delay	better than 60 dB4w
Maximum delay	better than 48 dB4w

Mechanical Data

Chassis - CH1/65B

Indexing positions - 1, 6 and 14

Plug indexing position - A1

Weight 0.6 kg.

Installation Data

Mount in PN3A/55, and wire to pins of rear socket as follows:-

pin 1 chassis earth	pin 9 channel B input (earth)
2 channel A output (signal)	10 channel B output (signal)
3 channel A output (earth)	11 channel B output (earth)
4 channel A input (signal)	12 not used
5 channel A input (earth)	13 not used
6 not used	14 -5 volt input
7 not used	15 +12 volt input
8 channel B input (signal)	16 -12 volt input
	17 0 volt input (earth)

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DESIGNS DEPARTMENT MANUFACTURING INFORMATION No.6.294(77)

O.B. Flat Delay, Line Equaliser EQ3/33

PRODUCTION TEST SCHEDULE

Description

This unit may be set to give a differential delay between two audio signals that are passed through it. If the front panel selector switch is set to "bypass" the inputs are connected directly to the outputs, in the other positions each signal passes through a separate audio delay circuit. One of the delay circuits may be set to a delay within the range 500µs to 5,500µs while the other is set to 500µs, thus giving 0 to 5ms differential delay. The front panel selector switch allows the variable delay to be in either channel A or channel B and code switches on the front panel control the variable delay. The code switch indicate the differential delay.

Printed boards 1 and 2 are similar, they each consist of a low pass filter, a "bucket brigade" delay circuit, a second low pass filter, an audio amplifier and a clock pulse amplifier. Channel A is permanently wired to printed board 1 and channel B is permanently wired to printed board 2, and the delay is each channel is determined by the clock frequency applied. Printed board 3 consists of a 51.2MHz oscillator which drives two divider circuits, one fixed and one variable, and their outputs are connected to the appropriate channels to provide fixed or variable delay, the selection being made by the front panel selector switch.

In the eventof a failure in either the + or -12 volt power supply input, the audio bypass relays will de-energise and connect the audio inputs directly to the audio outputs.

Information

a)	Designs Section:	Transmission Section
b)	Designer:	M.T. Ellen
c)	Engineer Responsible:	M.T. Ellen
d)	Handbook:	Part of Handbook 6.141(77) for stereo phase and delay equaliser panel PA1M/90.
e)	Technical Instruction:	Not available 1.3.77
f)	Other information	
g)	Pre-production batch:	This Production Test Schedule has not been tested on a pre-production batch in Designs Department.

Manufacturing Performance Specification

a) Input requirements

Low Distortion sine wave 20Hz to 15kHz at +10dBm max.

b) Outputs:

Similar to input but delayed by up to 5,500µs

BBC
DS/SPA4

c) Power supply:

+12 ± 0.4 volts at 0.16 ± 0.02 Amps.

-12 ± 0.4 volts at 0.12 ± 0.02 Amps.

+ 5 ± 0.1 volts at 0.8 ± 0.1 Amps.

d) Performance:

Gain of each channel	0 ± 0.75 dB at 1 kHz over full delay range.
Frequency response of each channel	+0.2 dB to -0.8 dB relative to the gain at 1 kHz over the range 100 Hz to 13 kHz.
Total Harmonic Distortion	
Minimum delay, 0 dBm 1 kHz input	better than -42 dB
Minimum delay, +10dBm 1kHz input	better than -30 dB
Maximum delay, 0dBm 1kHz input.	better than -60dB
Maximum delay, +10dBm 1kHz input.	better than -52 dB
Signal to Noise ratio	
Minimum delay	better than 60dB4w
Maximum delay	better than 48dB4w

Warning

a) No voltages above 50 V d.c. or 30 V a.c. are connected to this unit.

b) Note that 1IC3 and 2IC3 are "bucket brigade delay lines" which use MOS technology. They incorporate protection against electrostatic discharge, butthey can be damaged by a supply voltage greater than 18 volts.

Test Apparatus Required.

2-off 0-12 volt variable power supply up to 0.5 Amps., fitted with ammeter and current limit control.

1-off 0-5 volt variable power supply up to 1 Amp., fitted with ammeter and current limit control.

1-off DVM 0.1% accuracy.

1-off Frequency counter, maximum frequency ⩾ 60MHz.

1-off High frequency oscilloscope and probe, B/W = 50MHz.

1-off A.C. Test Equipment type EP14/1.

Inspection

a) Check that the slot positions of the coding comb are 1, 6 and 14 (see D 42022 A2 det 4)

b) No mains voltages are connected to this unit. Check all the connections between PCB1, PCB2, PCB3 and the components on the front panel. (see Assembly and Wiring D 42021 A1)

c) Check that the following components are correctly inserted:

i) Capacitors 1C1 to 1C19, 2C1 to 2C19, and 3C1 to 3C18.

ii) Resistors 1R1 to 1R45, 2R1 to 2R45, and 3R1 to 3R64.

iii) Inductor 3L1.

iv) Diodes 1D1, 2D1, 3D1 to 3D5.

v) Transistors 1TR1 to 1TR11, 2TR1 to 2TR11, and 2TR, and 3TR1 to 3TR10.

vi) Integrated circuits 1IC1 to 1IC4, 2IC1 to 2IC4 and 3IC1 to 3IC11
Note: 1IC3 and 2IC3 should be mounted in sockets.

vii) Plug 1PLA.

7. Test Procedure:

7.1 Adjust 17 volt Regulators:

a) Remove 1LK and 2LK, then connect power supplies (set to 0 volts) as follows:-

PSU1 (+12V) current limit 0.2 amps, -ve to PLA 17 and +ve to PLA 15.

PSU 2 (-12V) current limit 0.2 amps, -ve to PLA 16 and +ve PLA 17.

Slowly increase the voltages to the values shown in brackets, while monitoring the current, then measure the voltages between pins 1 and 5 of 1IC1, and between pins 1 and 5 of 2IC1 (use a DVM).

b) The current readings should not exceed 100mA and both voltages should be 17 $\pm$ 0.4 volts.

c) If the current consumption is over 100mA look for shorts OR incorrect components, and if the voltages are out of tolerance adjust 1R4 and/or 2R4 (reduce the resistance to increase the voltage).

7.2 Check current consumption:

a) Switch off P.S.U. 1 and P.S.U. 2, replace 1LK and 2LK, set front panel switch to 'A' then connect a third power supply (set to 0 volts) as follows:-

P.S.U.3 (-5V) current limit 1 amp, -ve to PLA 14 and +ve to PLA 17.

Slowly increase the voltage to 5 volts while monitoring the current, also switch on and note th current taken from PSU1 and PSU2.

b) The current taken should be within the following limits:-

PSU1 (+12V) - 0.16 ± 0.02 amps.

PSU2 (-12V) - 0.12 ± 0.02 amps.

PSU3 (- 5V) - 0.8 ± 0.1 amps.

c) If the current taken from PSU1 or PSU2 is out of limits fault location may be eased by removing 1LK and/or 2LK. If the current taken from PSU3 is out of limits the fault is probably on PCB 3.

7.3 Check 10 volt regulator:

a) Measure the voltage across 3C3 (use a DVM), and vary PSU2 from -11.6 volts to -12.6 volts.

b) The measured voltage should be 10 ± 0.3 volts and it should not vary by more than 0.02 volts when PSU2 is adjusted.

c) If the voltage is out of tolerance adjust 3R3 (increase the resistor value to increase the voltage).

7.4 Check oscillator frequency range:

a) Set 3R7 fully anti-clockwise, then adjust 3R8 to obtain a sine wave on 3IC3 pin 13 (amplitude 1 ± 0.5 volts peak-to-peak). Now connect a frequency counter to 3IC3 pin 13 and adjust 3C4.

b) Check that the frequency range obtainable is at least 50 to 51.4MHz, then set the oscillator to 51.2 ± 0.1MHz.

c) If the oscillator does not have the required range check that 3L1 has been made in accordance with the drawings. Also check that the leads on all the oscillator components are as short as possible.

7.5 Set oscillator amplitude and d.c. level:

a) Connect an oscilloscope to 3IC3 pin 13, an adjust 3R7 and 3R8 to set the amplitude and d.c. level respectively.

The oscilloscope and probe combination should have a bandwidth of 50MHz. The input should be d.c. coupled, with ground potential on the top line of the graticule and 0.5 volts/division sensitivity at the probe tip.

b) The positive peak of the waveform should be -1 ± 0.2 volts w.r.t. ground and the negative peak should be -1.5 ± 0.2 volts w.r.t. ground. The waveform should be approximately sinusoidal.

c) If this waveform cannot be obtained check the connections to 3IC3, 3IC5, 3IC6, 3IC7, 3IC8, 3IC9 and terminating resistors 3R46 and 3R47.

7.6 Check divide-by-50 circuit:

a) Use an oscilloscope and frequency counter to check the waveform and frequency on the collector of 3TR6.

b) The waveform should be a 70 ± 20nS negative pulse with a positive level higher than -2.6 volts and a negative level lower than -4.2 volts. Its frequency should be 1024 ± 2kHz.

c) If the waveshape is wrong check the circuit associated with 3TR4 3TR6. If the frequency is wrong check 3IC8 and 3IC9.

7.7 Set the oscillator frequency:

a) Connect a frequency counter to the collector of 3TR6 and adjust 3C4 to set the frequency.

b) The frequency should be 1024 ± 0.1kHz.

c) If the frequency cannot be set tests 7.4 to 7.5 have not been carried out sucessfully.

7.8 Check programmable divider (set to divide-by-50):

a) Set the front panel code switches to 000 (this sets the programmable divider to divide by 50). Use an oscilloscope and frequency counter to check the waveform and frequency on the collector of 3TR7.

b) The waveform should be a 70 ± 20nS negative pulse with a positive level higher than -2.6 volts and a negative level lower than -4.2 volts. Its frequency should be 1024 ± 0.1 kHz.

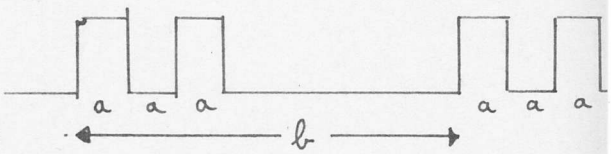
c) If the waveshape is wrong check the circuit associated with 3TR7 3TR9 and 3TR10. If the frequency is wrong check the wiring to the code switches. If no fault is found but the test has not been passed carry out the tests in 7.9.

7.9 Fault isolation in the programmable divider.
(only to be carried out if the unit does not pass test 7.8):

a) Remove the feedback to the three cascaded divide-by-10 circuits by connnecting 3IC7 pin 5 to earth (3IC7 pin 16), this should set the divider to divide by-1000 and its output frequency (3TR7 collector) should be 51.2kHz. Use an oscilloscope (B/W > 50MHz) to measure the circuit nodes given in b).

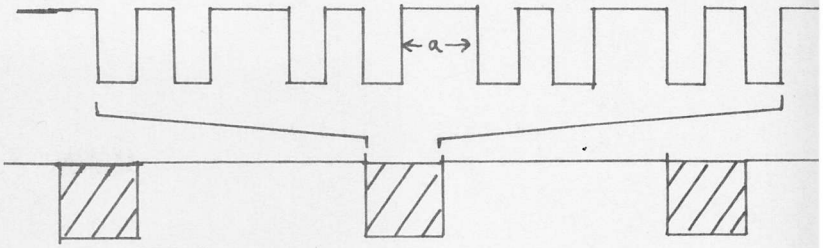
b) Each of the following waveforms should have two logic states, logic 1 should be higher than -0.96 volts and logic 0 should be lower than -1.65 volts at 25°C. However, due to the limited bandwidth of the oscilloscope the waveforms in tests ii) and iii) will be slightly different; see test 7.5 for details. All the times given below are accurate to ± 3% only.

Circuit Node:	Waveform:
i) 3IC3, 3IC5 and 3IC6 pin 9	logic 1
ii) 3IC3, 3IC5 and 3IC6 pin 13	logic 1 for 20nS every 40nS
iii) 3IC7 pin 6	logic 1 for 20nS every 40nS
iv) 3IC5 pin 10	logic 0 for 20nS every 200nS
v) 3IC6 pin 10	logic 0 for 20nS every 2µS.
vi) 3IC2C pin 3	



a = 200nS
b = 2µS

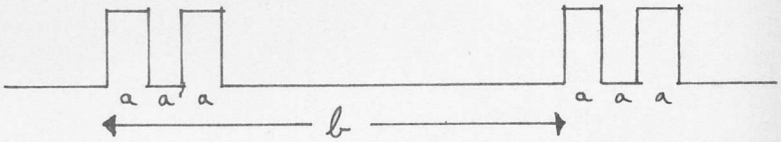
vii) 3IC4b pin 2



a = 800nS
b = 20µS

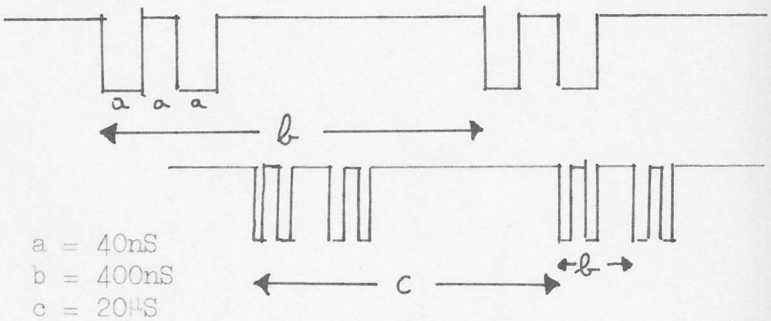
viii) 3IC2d pin 2 — logic 1 for 2µS every 20µS

ix) 3IC2b pin 14



a = 200nS
b = 20µS

x) 3IC2a pin 14



a = 40nS
b = 400nS
c = 20µS

xi) 3IC4 pin 15	logic 0 for 20nS every 20µS
xii) 3IC7 pin 7	logic 0 for 20nS every 20µS

c) If the waveforms are checked in the given order, then incorrect waveforms lead to probable faults associated with the following IC's:

Test failed	Probable fault location
i) ii) and iii)	3IC3, 3IC5, 3IC6, 3IC7
iv)	3IC3, 3IC5, 3R19
v)	3IC5, 3IC6, 3R28
vi)	3IC2a, 3R23, 3R30, 3IC2b, 3R29
vii)	3IC4b, 3R31, 3R32, 3R37, 3R38, 3R22, 3IC4a
viii)	3IC2d, 3R39, 3R40, 3R41, 3IC2b
ix)	3IC2b, 3R11, 3IC2a
x)	3IC2a, 3R10, 3R11, 3R12, 3IC4a
xi)	3IC4a, 3IC7, 3R63, 3R64, 3TR10
xii)	3IC7

Remove the earth on 3IC7 pin 5.

7.10 Check digital changeover switch:

a) Use an oscilloscope to check the waveforms on pins P and S with the code switch set to 500(0)μS. Operate the selector switch on the front panel to check the table given in b).

b) The waveform should be a positive 20nS pulse with a base line lower than +0.8 volts and a peak higher than +2.4 volts.

The approximate period between pulses is shown in the following table:-

Selector switch	P	S
By pass	1μS	11μS
A	11μS	1μS
B	1μS	11μS

c) If the waveform amplitudes are wrong check all the components connected to pins P and S. If the periods are wrong check 3IC10 and SA7.

7.11 Check clock driver circuits:

a) Set the code switches to 000(0)μS and use an oscilloscope to check the waveforms on 1IC3 pin 1, 1IC3 pin 4, 2IC3 pin 1 and 2IC3 pin 4.

b) In each case the waveform should be a square one with a period of 1.95μS and 16 ± 0.5 volts amplitude (-11.5 to +4.5 volts approx.).

c) If the waveshape is wrong check the relevant three transistor drive circuit, and if the frequency is wrong check 1IC2 and/or 2IC2.

7.12 Set audio gain:

a) Connect PO jack leads as follows:-

PLA 4 (tip), PLA 5 (ring)	channel A input
PLA 2 (tip), PLA 3 (ring)	channel A output
PLA 8 (tip), PLA 9 (ring)	channel B input
PLA 10 (tip), PLA 11 (ring)	channel B output

Connect the oscillator output (set to 1kHz, 0dBm, 600Ω, unterminated) of the AC test set to channel A input. Connect channel A output to the AC test set input, select "MEAN - FLAT" and set the attenuators to 0dB. Now set the code switches to 050(0)μS, the selector switch to A and adjust 2R42 to set the output level. Repeat the above with channel B, selector switch to B and 1R42.

b) The output level should be 0dBm.

c) If the output level cannot be set correctly check the relevant low pass filters and output amplifier. If the output level cannot be changed check the power supply detector circuit (test 7.17).

7.13 Check frequency response:

a) Connect the AC test set as described in test 7.12, then adjust the oscillator frequency and input attenuators to check the frequency response of each channel in turn.

b) The frequency response should fall within the following limits:-

1. +0.2dB to -0.8dB relative to the gain at 1kHz over the range 100Hz to 13kHz.

2. At 20kHz the gain should be at least 18dB less than the gain at 1kHz.

c) If the frequency response does not meet the specification check the component values of the low pass filters.

7.14 Set distortion to minimum:

a) Connect the AC test set oscillator (set to 1kHz, ±10dBm, 600Ω unterminated) to the channel A input, connect the channel A output to the AC test set input and select "MEAN - FLAT" with the attenuator set to +10dB. Set the code switches to 000(0)μS and check that the output level is +10 ± 1dBm. Select "MEAN-1kHz HARMONICS" then change the attenuator to get a centre reading on the meter. Adjust 2R29 then repeat with channel B and 1R29.

b) Adjust for minimum distortion, and if a large adjustment is necessary repeat test 7.12.

c) If a minimum cannot be obtained within the range of R29 check R28, R29, R30 and R45.

7.15 Check distortion:

a) Connect the AC test set socillator (set to 1kHz, 0dBm, 600Ω unterminated) to the channel A input, connect the channel A output to the AC test set input and select "MEAN - FLAT". Set the code switches to 000(0)#S and adjust the attenuator to obtain a centre reading on the meter. Select "MEAN - 1kHz HARMONICS", re-adjust the attenuator to get the same reading and note the difference in attenuator settings (Harmonic separation).

Repeat with channelB.

b) The harmonic separation should be better than 42dB.

c) If this figure cannot be obtained the fault is probably in IC3.

7.16 Check signal to noise ratio:

a) Connect the AC test set oscillator (set to 1kHz, 0dBm 600Ω unterminated) to the channel A input, connect the channel A output to the AC test set input and select "TPM - NORMAL" with the attenuator set to 0dB. Set the code switches to 500(0)#S and the selector switch to A then check that the meter reads "4". Connect the channel A input to a 600Ω termination, select "TPM WEIGHED" then adjust the attenuator to obtain a reading of "4" on the meter, and note the difference in attenuator readings (S/N ratio in dB4w) change the front panel selector switch to B and repeat with channel B.

b) The signal to noise ratio should be better than 48dB4w.

c) If this figure cannot be obtained the fault is probably in IC3.

7.17 Check power supply detector circuit:

a) Connect the AC test set as detailed in test 7.12 and set the selector switch to A. Switch off the -5 volt power supply and note the audio output signals disappear from both channels. Now decrease either the + or -12 volt supply until the audio output signals re-appear when sum of the outputs from PSU 1 (+12 V) and PSU 2 (-12V) drops to 21.5 ± 1 volts.

c) If the relays de-energise at the wrong voltage check 3D4, 3R56, 3R57 and 3TR8.

7.18 Check "out of range" LED:

a) Set the left hand code switch to each of its 10 positions in turn and note whether the out of range LED is on or off.

b) It should be on for numbers 8 and 9 only (it should not be affected by the positions of the other code switches.

c) If this test is not passed check the wiring to the LED and code switch.

D42020A4 SHEET 1 OF 14

CHANGE
3 1/4 * ADDED. ITEM 1 REVISED. SPEC ADDED TO ITEM 2. L.F.M. 1.2.77
NO CHANGE W.H.V. JOR. 1.3.77.

EQ3/33. EQUALISER, LINE, O.B. FLAT DELAY P/LIST

ITEM No.	No. OFF		DESCRIPTION	C'CT REF.	BBC REF. OR DRG. No.
			DRAWING NUMBERS		
			CIRCUIT D42019A1		
			P/LIST D42020A4		
			ASSY & WIRING D42021A1		
			DETAILS 1-4 D42022A2		
			P/BRD 1 WIRING D42023A2		
			P/BRD 1 WIRING COMP SIDE D42024A2		
			P/BRD 1 COMP LOC D42025A3		
			P/BRD 1 DRILLINGS D42026A4		
			P/BRD 2 WIRING D42027A2		
			P/BRD 2 WIRING COMP SIDE D42028A2		
			P/BRD 2 COMP LOC D42029A3		
			P/BRD 2 DRILLINGS D42030A4		
			P/BRD 3 WIRING D42031A2		
			P/BRD 3 WIRING COMP SIDE D42032A2		
			P/BRD 3 COMP LOC D42033A3		
			P/BRD 3 DRILLINGS D42034A4		
			FURTHER INFORMATION REQ'D FOR MANUFACTURE		
			UNIT ASSY INFORMATION EA10484		
			UNIT WIRING " EA10137, EA10139		
			P/BRD WIRING " EA10140		
			INDUCTOR " E13127AA		
			INDUCTOR L/1682.		
			BRACKET. D37350 A3-CP-		
1	1	*	CHASSIS CH1/65B1 ASSEMBLED & MODIFIED BY CONTRACTOR AS FOLLOWS :-		552227-034943X
			FRONT PANEL DRILLED & ENGRAVED TO :-		D42022A2. DET 1
			HANDLE MARKING TO :-		D42022A2. DET 3
			NOTE. CODING PLATE SLOT POSITIONS I, G & H MODIFIED BY B.B.C. WORKSHOPS BEFORE ISSUE TO CONTRACTOR.		D42022A2. DET 4
2	1	*	PRINTED BOARD 1 TO SPEC ED/PB/EQ3/33/1 COMPRISING ALL ITEMS WITH CIRCUIT REF'S PREFIXED BY FIGURE 1		D42023A2. D42024A2 D42025A3. D42026A4
3					
4					

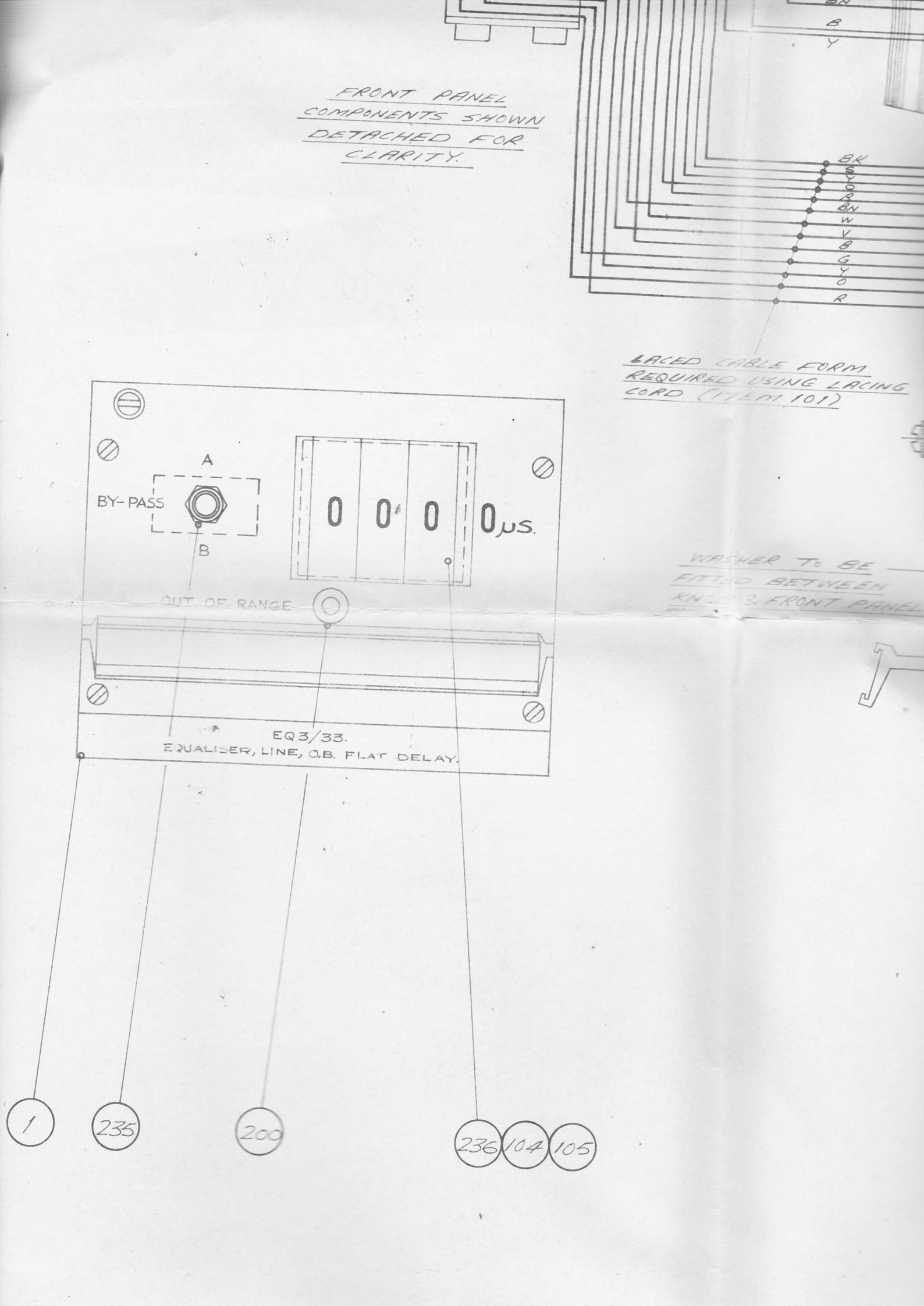
BBC DS PLA4

EQ3/33. EQUALISER, LINE, O.B. FLAT DELAY P/LIST.

DRN. E.W.W. TPD. CKD. APPD. C.R.C.

DESIGNS DEPARTMENT

D42020A4 SHEET 1 OF 14


FRONT PANEL COMPONENTS SHOWN DETACHED FOR CLARITY.
BK
BN
W
V
B
G
Y
O
R
LACED CABLE FORM REQUIRED USING LACING CORD (ITEM 101)
A
BY-PASS
B
0 0 0 0 µS.
OUT OF RANGE
EQ3/33.
EQUALISER, LINE, O.B. FLAT DELAY.
WASHER TO BE FITTED BETWEEN KNOB & FRONT PANEL
1
235
200
236
104
105

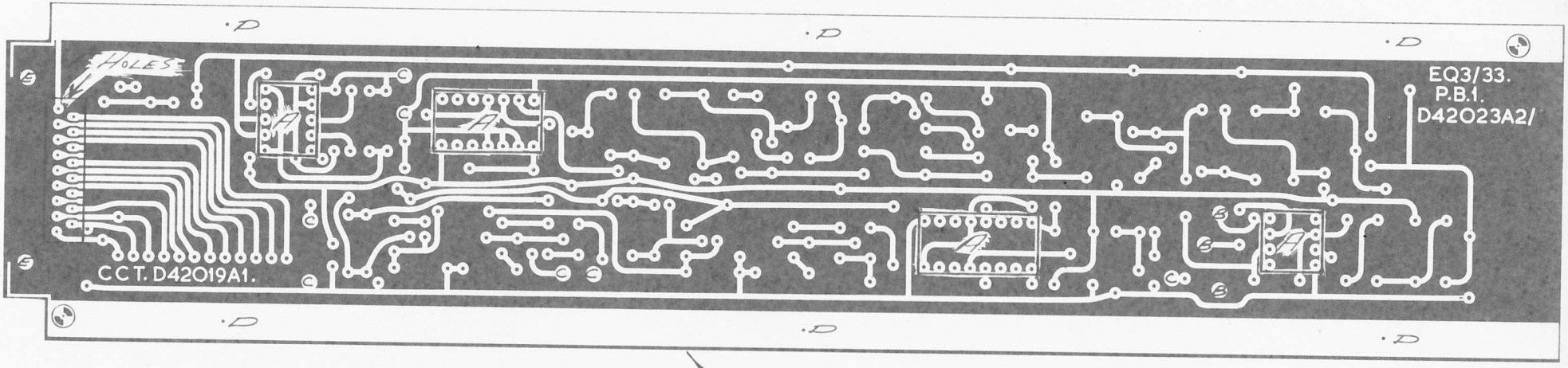
BBC

EQ3/33 PRINTED BOARD DRILLING P.B.1

D42026A4

CHANGE	ISS
31/1/77	1

PRINTED BOARD DRILLING EQ3/33 P.B.1



HOLE REF.	DRILL NO. OR SIZE	DIAMETER DEC.	DIAMETER MM
A			.75
B			1.2
C			1.0
D			3.2
E			2.7
F			0.9
⊕			3.0
UN-LETTERED			.85

APPROX NO OF HOLES : 309

CUT BOARD TO OUTER EDGE OF COPPER SCALE 1:1

MATERIAL 1·6 THK TO BS4584, +CL 5·2, EP-GC-Cu-3, 35/1, 1·6±0·20 (EPOXIDE WOVEN GLASS FABRIC, CLAD ON ~~ONE~~ / BOTH SIDES WITH 35μm COPPER)

FINISH TINNED

MANUFACTURED TO D42023A2. D42024A2 D42025A3

DESIGNS DEPARTMENT

DRN GMW

TCD

CKD

APPD CJC

D42026A4

VM246A4

BBC

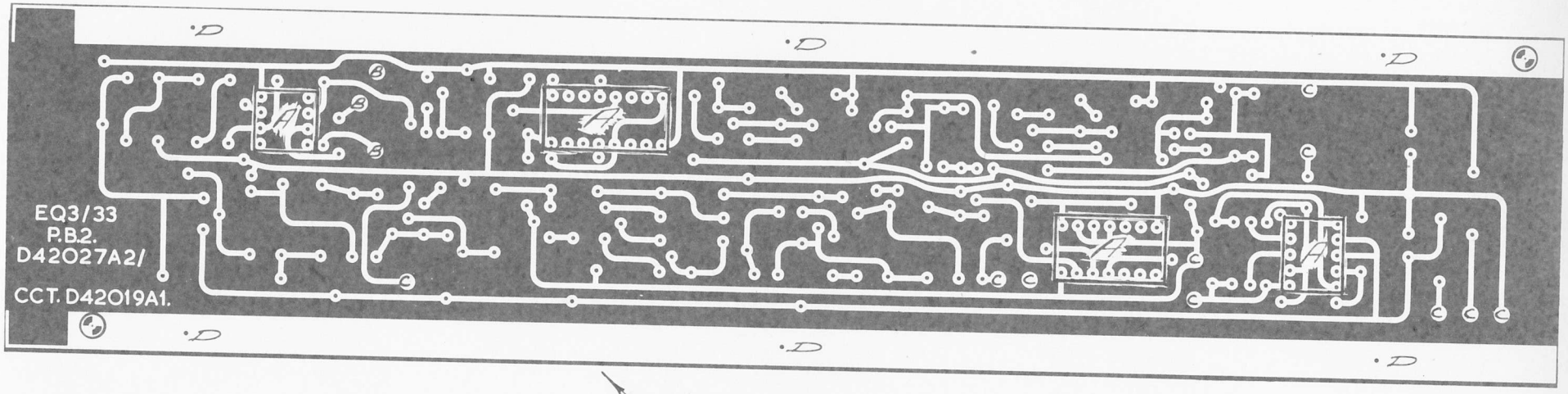
EQ3/33 PRINTED BOARD DRILLING
P.B.2

D42030A4

PRINTED BOARD DRILLING

EQ3/33
P.B.2

CHANGE	ISS
31/1/44	



CUT BOARD TO OUTER EDGE OF COPPER SCALE 1:1

HOLE REF.	DRILL NO. OR SIZE	DIAMETER DEC	DIAMETER MM
A			·45
B			1·2
C			1·0
D			3·2
⊕			3·0
UN-LETTERED			·85

APPROX NO OF HOLES: 325

MATERIAL 1·6 THK. TO BS4584, +CL 5·2, EP-GC-Cu-3, 35/1, 1·6±0·20 (EPOXIDE WOVEN GLASS FABRIC, CLAD ON ~~ONE~~/BOTH SIDES WITH 35μm COPPER)

FINISH TINNED

MANUFACTURED TO D42027A2 D42028A2 D42029A3

APPD	CKD	TCD	DRN
CEC			GMW

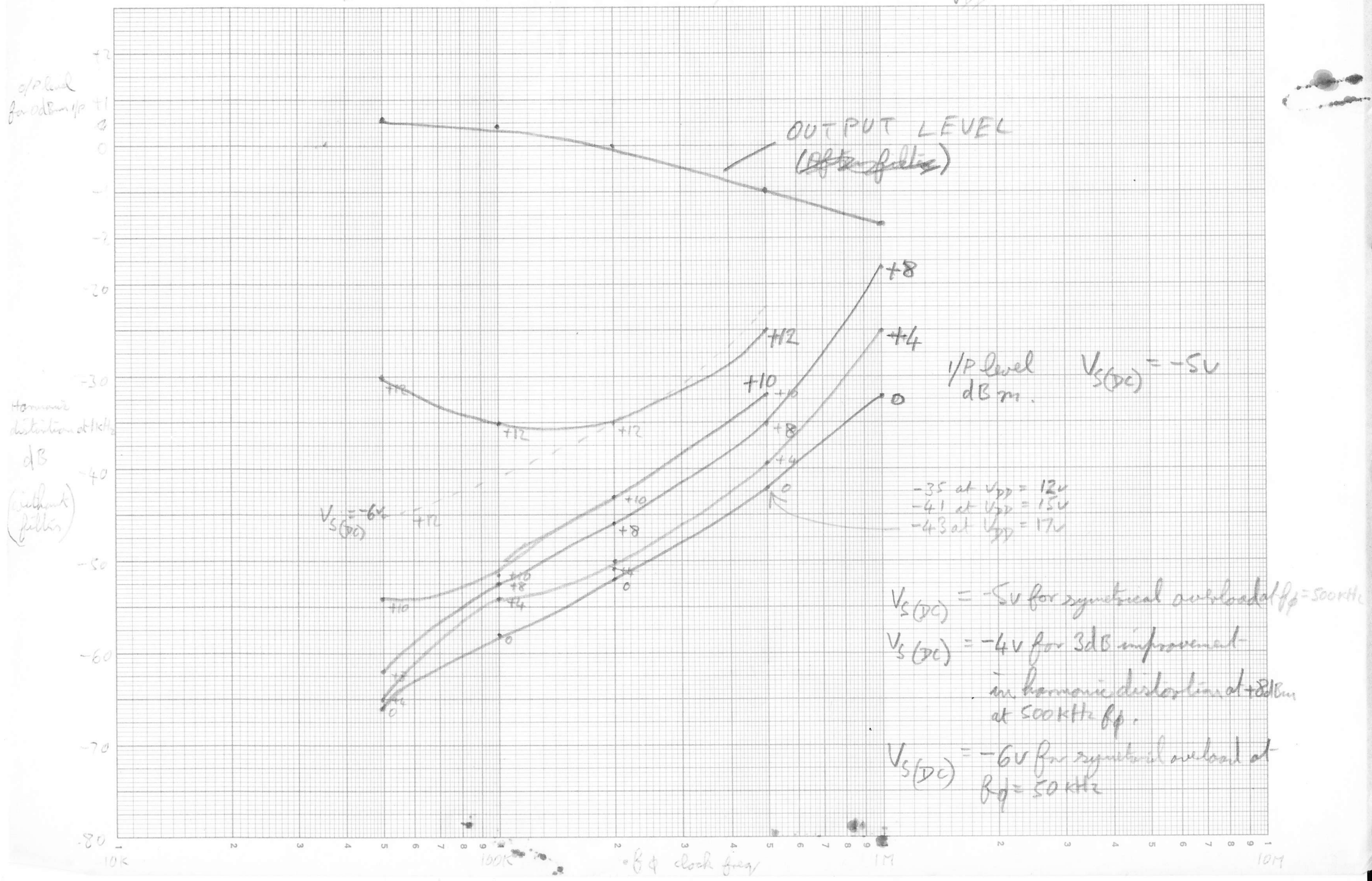
DESIGNS DEPARTMENT

D42030A4

M.J. ALLEN 12/10/78

BUCKET BRIGADE DELAY LINE TDA 1022

$V_{DD} = -16V$



$V_{S(DC)} = -5v$ for symetrical overload $f_p = 500kHz$

$V_{S(DC)} = -4v$ for 3dB improvement in harmonic distortion at +8dBm at 500kHz f_p.

$V_{S(DC)} = -6v$ for symetrical overload at $f_p = 50kHz$

S/N measurements on Bucket Brigade delay line

15/6

M. Ellis

S/N measured by adjusting bias on pin 5 to produce minimum distortion, then adjusting the input level to give -42 dB harmonic separation at 1kHz. The resulting output level was then set to give 1mW (0 dBm) at the PPM. The input to the EQ3/33 was then terminated and the PPM level was adjusted to give 4 on the PPM and the new weighting network selected. The difference in attenuator setting was then recorded.

S/N

dB

EQ3/33

RD'

RD

both channels of EQ3/33 in cascade

mS.

RD' now refers to 1kHz at level that gives 1% dist with bias adjusted to optimum (CCIR)
RD' as above but up 4dB to convert to new 468 weighting.

BUCKET BRIGADE DELAY LINE
for analogue signals

TDA1022

The TDA1022 is a MOS monolithic integrated circuit, generally intended to delay analogue signals (e.g. delay time = $512/2\ f_\phi$).
It can be used with clock frequencies in the range 5 kHz to 500 kHz.
The device contains 512 stages, so the input signal can be delayed from 51,2 ms to 0,512 ms.
Applications in which the device can be used:

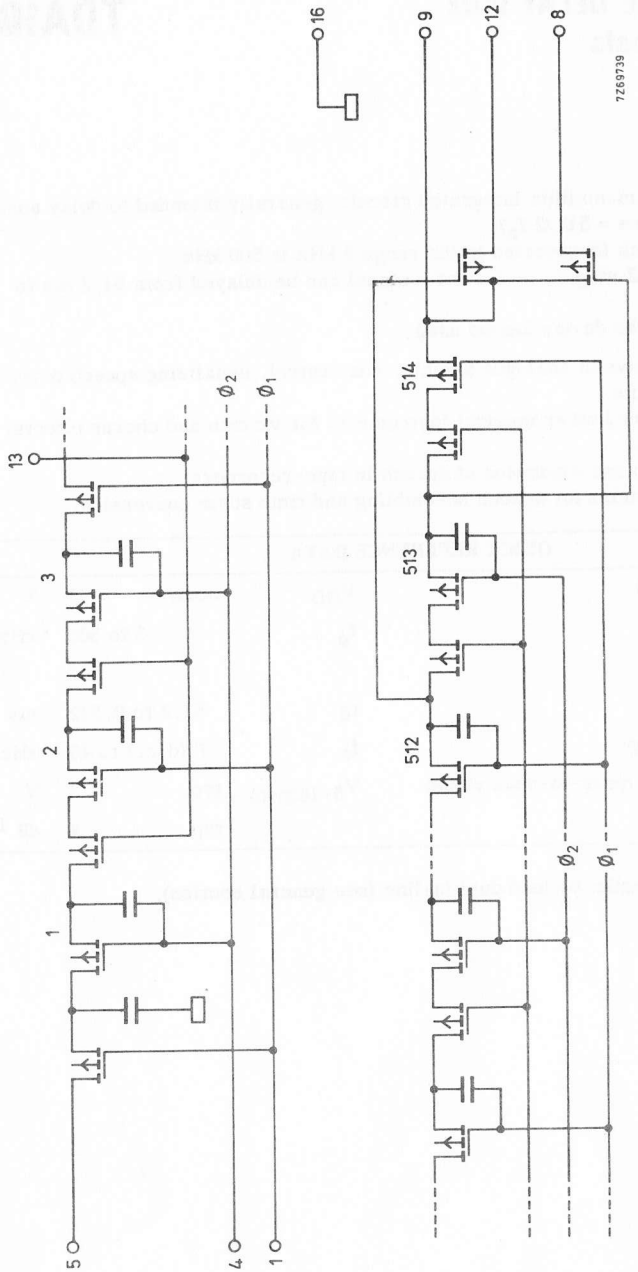
- variation of fixed delays of analogue signals, vox control, equalizing speech delay in public address systems;
- in electronic organs and other musical instruments for vibrato and chorus effects;
- reverberation effects;
- variable compression and expansion of speech in tape-recorders;
- in communication systems for speech scrambling and time scale conversion.

QUICK REFERENCE DATA				
Supply voltage (pin 9)	V_{DD}	nom.	−15	V
Clock frequency	f_ϕ		5 to 500	kHz
Number of stages			512	
Signal delay range	t_d		51,2 to 0,512	ms
Signal frequency range	f_s		0 (d.c.) to 45	kHz
Input voltage at pin 5 (peak-to-peak value)	$V_{5\text{-}16(p\text{-}p)}$	typ.	7	V
Line attenuation		typ.	4	dB [1]

PACKAGE OUTLINE plastic 16-lead dual in-line (see general section).

[1]) See note 1 on page 4.

CIRCUIT DIAGRAM



PINNING

1. Clock input 1 (V_{CL1})
2. Not connected
3. Not connected
4. Clock input 2 (V_{CL2})
5. Signal input
6. Not connected
7. Not connected
8. Output 513
9. Negative supply (V_{DD})
10. Not connected
11. Not connected
12. Output 512
13. Tetrode gate (V_{13-16})
14. Not connected
15. Not connected
16. Ground (substrate)

BUCKET BRIGADE DELAY LINE for analogue signals

TDA1022

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages (see note)

Supply voltage	9-16	0 to −20	V
Clock input, data input, output voltage and V_{13-16}		0 to −18	V

Current

Output current	I_8 ; I_{12}	0 to 5	mA

Temperatures

Storage temperature	T_{stg}	−40 to +150	°C
Operating ambient temperature	T_{amb}	−20 to +85	°C

Note

Though MOS integrated circuits incorporate protection against electrostatic discharge, they can nevertheless be damaged by accidental over-voltages.
To be totally safe, it is desirable to take handling precautions into account.

CHARACTERISTICS at T_{amb} = −20 to +55 °C; V_{DD} = −15 V; $V_{\phi 1} = V_{\phi 2}$ = −15 V; V_{13-16} = −14 V; R_L = 47 kΩ (unless otherwise specified)

Supply voltage range	V_{DD}		−10 to −18	V	[1]
Supply current	I_9	typ.	0,3	mA	
Clock frequency	$f_{\phi 1}$; $f_{\phi 2}$		5 to 500	kHz	[2]
Clock pulse width	$t_{\phi 1}$; $t_{\phi 2}$	≤	0,5T		[3]
Clock pulse rise time	$t_{\phi 1r}$; $t_{\phi 2r}$	typ.	0,05T		[3]
fall time	$t_{\phi 1f}$; $t_{\phi 2f}$	typ.	0,05T		[3]
Clock pulse voltage levels; HIGH	$V_{\phi 1H}$; $V_{\phi 2H}$		0 to −1,5	V	
LOW	$V_{\phi 1L}$; $V_{\phi 2L}$	typ.	−15	V	[1]
			−10 to −18	V	[1]

[1] It is recommended that $V_{13-16} = V_{\phi 1L} + 1\ V = V_{\phi 2L} + 1\ V$; V_{DD} more negative than $V_{\phi L}$.

[2] In theory the clock frequency must be higher than twice the highest signal frequency; in practice $f_s \leq 0,3\ f_\phi$ to $0,5\ f_\phi$ is recommended, depending on the characteristics of the output filter.

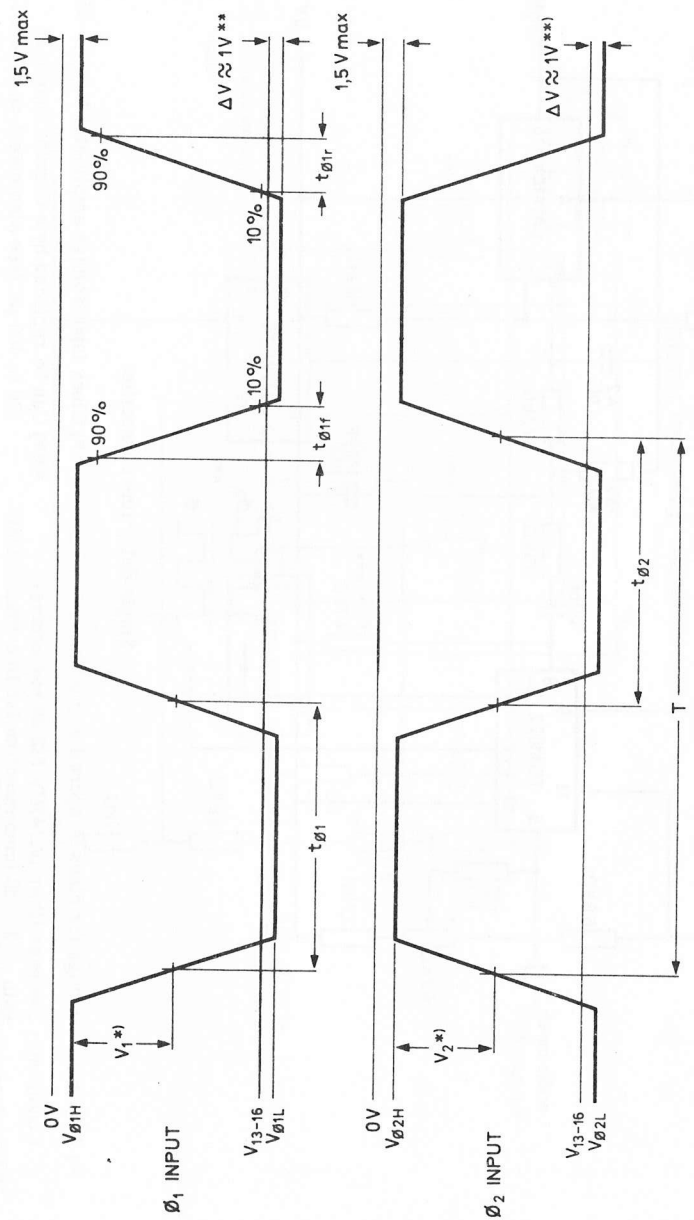
[3] T = period time = $1/f_\phi$. The data on fall and rise times are given to eliminate overlap between the two clock pulses. To be independent of these rise and fall times a clock generator with simple gating can be used. See also pages 5 and 8.

CHARACTERISTICS (continued)

Signal input voltage at 1% output voltage distortion (r.m.s. value)	$V_{s(rms)}$	typ.	2,5	V	
Signal frequency	f_s		0 (d.c.) to 45	kHz	
Attenuation from input to output f_ϕ = 40 kHz; f_s = 1 kHz		typ.	4	dB	[1]
		<	7	dB	
Change in output at f_s = 1 kHz; $V_{s(rms)}$ = 1 V when f_ϕ varies from 5 to 100 kHz		typ.	0,5	dB	
		<	1	dB	
when f_ϕ varies from 100 to 300 kHz		typ.	0,5	dB	
		<	1	dB	
D.C. voltage shift when f_ϕ varies from 5 to 300 kHz		<	0,5	V	
Noise output voltage (r.m.s. value) f_ϕ = 100 kHz (weighted by "A" curve)	$V_{N(rms)}$	typ.	0,25	mV	
Signal-to-noise ratio at max. output voltage	S/N	typ.	74	dB	
Load resistance	R_L	>	10	kΩ	[1]
		typ.	47	kΩ	

[1] Attenuation can be reduced to typ. 2,5 dB if load resistor is replaced by a current source of 100 to 400 μA.

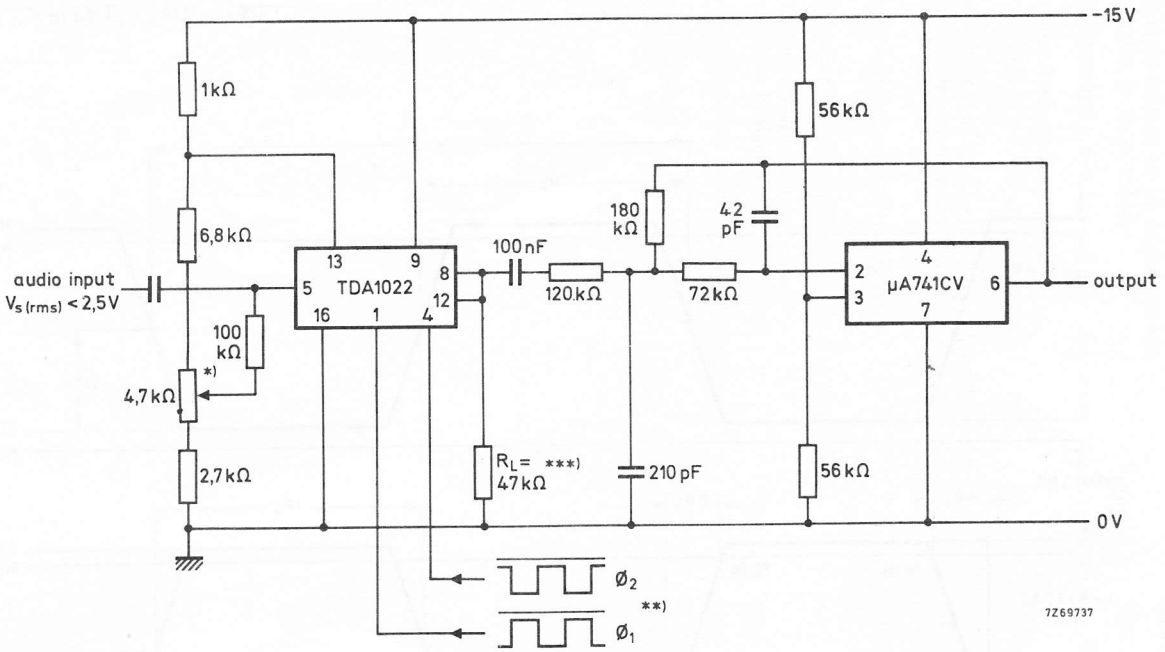
TIMING DIAGRAM



*) $|V_1 + V_2| \leq |V_{\phi 1L}|$; $V_{\phi 1L} = V_{\phi 2L}$.

**) For maximum dynamic range adjust V_{13-16} so that $\Delta V = V_{13-16} - V_{\phi L} \approx 1$ V.

APPLICATION INFORMATION



Single delay line connection

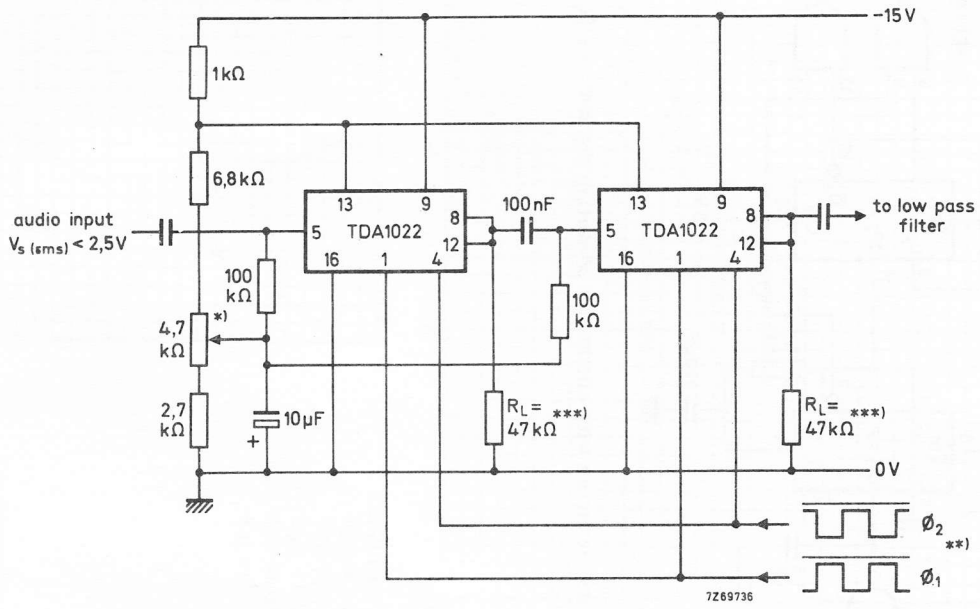
*) Adjust d.c. voltage for class-A operation (≈ 5 V).

Conditions: low pass filter μA741CV (12 dB per octave);
gain = +3,5 dB (compensation for line attenuation);
f_ϕ = 50 kHz (min.);
cut-off frequency = 15 kHz.

**) Clock input voltage amplitude: $V_{CL} = -15$ V.

***) Can be replaced by a current source of 100 to 400 μA (see also note 1 on page 4).

APPLICATION INFORMATION (continued)

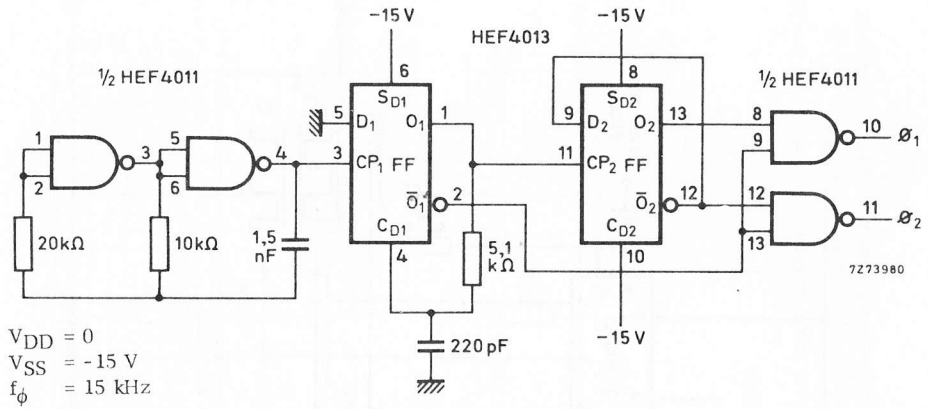


Series connection of two lines TDA1022

*) Adjust d.c. voltage for class-A operation (≈ 5 V).

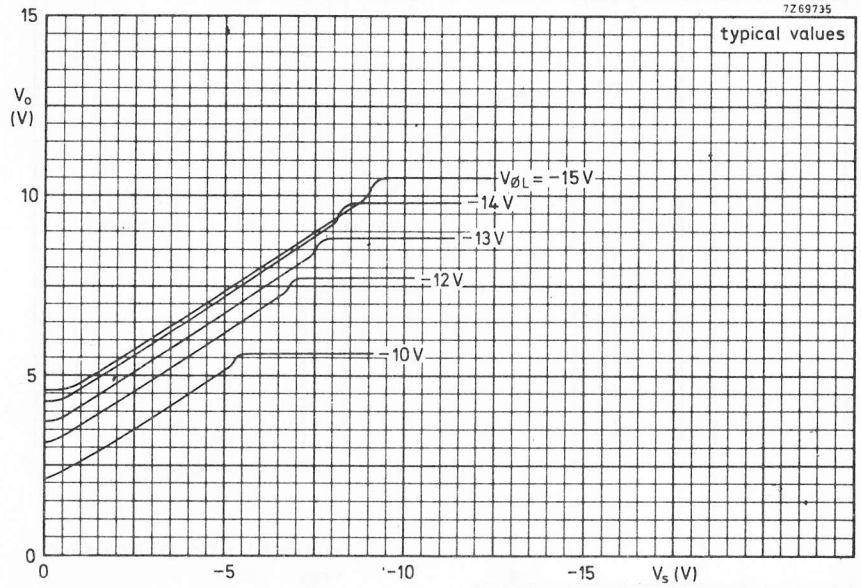
**) Clock input voltage amplitude: $V_{CL} = -15$ V.

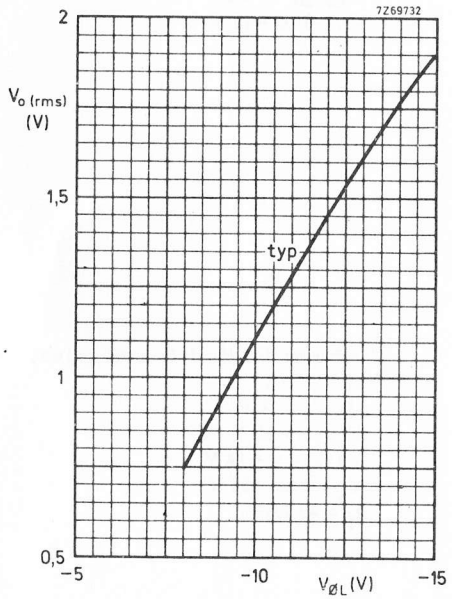
***) Can be replaced by a current source of 100 to 400 μA (see also note 1 on page 4).



V_{DD} = 0
V_{SS} = -15 V
f_ϕ = 15 kHz

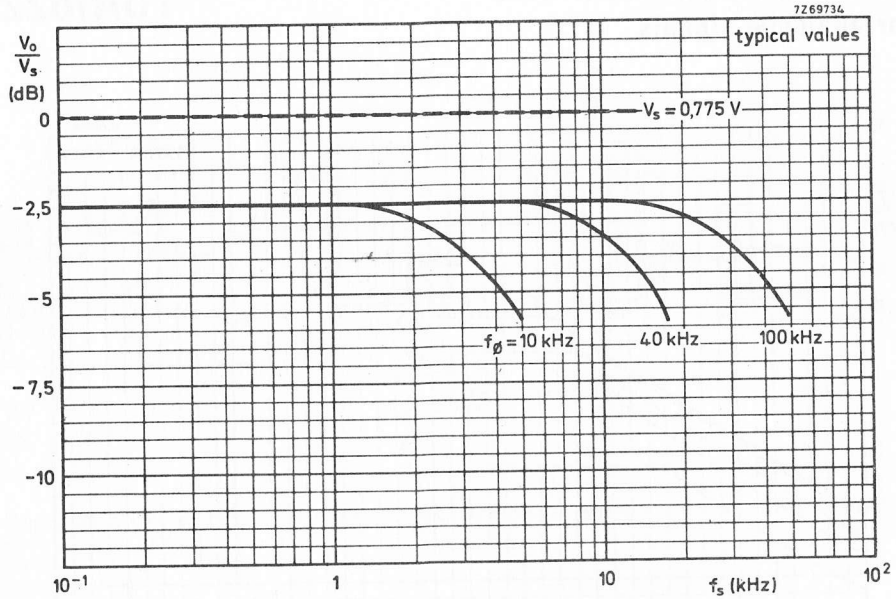
Clock oscillator and driver circuit with elimination of overlap (for max. 6 x TDA1022)





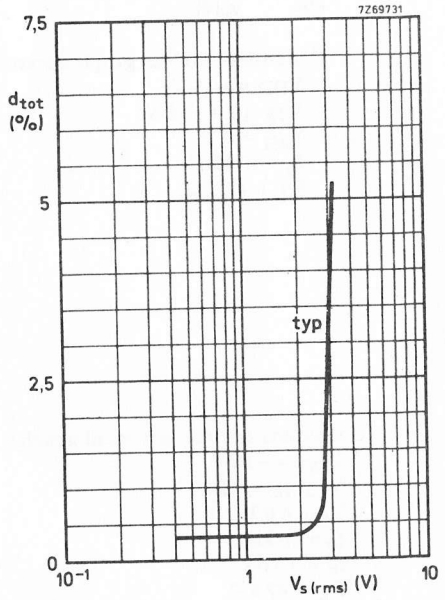
Conditions for the graph above:
V_{DD} = −15 V
V_{13-16} = −14 V
$V_{\phi H}$ = 0 V
f_ϕ = 40 kHz
R_L = 47 kΩ

Conditions for the left-hand graph:
V_{DD} = −15 V
V_{13-16} = −14 V
$V_{\phi H}$ = 0 V
f_ϕ = 40 kHz
f_S = 1 kHz
R_L = 47 kΩ



Conditions for the graph above:

V_{DD} = −15 V
V_{13-16} = −14 V
V_ϕ = 0 to −15 V



Conditions for the left-hand graph:

f_S = 1 kHz
V_S = −5,2 V
V_{DD} = −15 V
V_{13-16} = −14 V
V_ϕ = 0 to −15 V
f_ϕ = 40 kHz