DESIGN & EQUIPMENT DEPARTMENT

HANDBOOK A.1048(88)

CD3L/58 SIX-CHANNEL NICAM MKII DECODER

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for HD&ED

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1. INTRODUCTION

The CD3L/58 is the decoder for the next generation of NICAM equipment. The components that make up this unit are: UN26/99, UN26/100, CO9/13 (2 off) and PS4/51. The CD3L/58 may be a sub-unit of two different 6U coded units - a PA1/146 which holds two complete CD3L/58's or a PA1/145 which holds a CD3L/58 and a CD2L/41 6 channel MKII NICAM coder.

The CD3L/58 receives a 2048 kbit/s HDB3 encoded bitstream and produces six channels of audio, with corresponding signalling bits. The audio outputs are available in digital and analogue form. The analogue versions are duplicated with comparator monitoring between them to check for device failures. The digital versions (also duplicated) conform to the AES/EBU specification AES3-1985.

Along with the audio outputs there are eight signalling bits associated with each channel pair and one signalling bit at the 2048 kbit/s level.

In the event of a systematic fault there is error flagging for the complete system to facilitate remote change-over. A continuous self-checking procedure runs as a background task and flags any systematic errors.

2. SPECIFICATION

Performance Data:

For connection data see D62190A1

Inputs: 2048 kbit/s HDB3 into 75 Ω at nominally 4.7V p-p bipolar. ±10% on BNC socket (SKC)
Mains power 240V AC +10%-15% on XLRLNE connector SKU

Power Outputs: The output from the PSU is available on a 15 way D type socket (SKB)
Maximum available current is +5 V @ 1 A and ±18 V 200 mA each

Audio Outputs: There are 18 analogue outputs in total:

(i) 6 (one per channel) main outputs.
(ii) 6 (one per channel) external comparator-monitor reference outputs
(iii) 6 (one per channel) quality monitor outputs

The analogue outputs are electronically balanced. The output impedance is 45 ±j5 Ω. There is short circuit protection on these outputs. They are link selectable for cosited/alternate sampling.

Above Circuits fitted on 56 way Varicon connector (SKD)

(iv) 6 digital audio outputs. 3*2048 kbit/s AES/EBU stereo channels (duplicated to allow A/B checks) fitted to 6 XLR plugs (PLA-PLF)

Digital Outputs:

(i) 3 groups of signalling channel outputs (at the 676 kbit/s level) each comprising:

8 parallel bits data (open collector)
1 strobe pulse (5 - 10 µs) (open collector)
1 common anode supply (15 Ω resistor to +5 V)
1 signal earth

(ii) 1 signalling channel (at the 2048 kbit/s level) comprising:

1 data bit (open collector)
1 strobe pulse (5 - 10 µs) (open collector)
1 common anode supply (15 Ω resistor to +5 V)

fitted to 37 way D type socket (SKA)

(iii) 2048 kHz buffered clock output (at TTL signal level) fitted to BNC socket (SKE)

Monitoring outputs:

(i) 12 executive outputs: 2 * 6 channel fault indications (open collector)
(ii) 6 bit error rate greater than preset outputs (open collector)
(iii) 1 'Digit fault' output (open collector)
(iv) 1 'Comparator Fail' output (open collector)
(v) 1 HDB3/2048 lock output (open collector)
(vi) 1 'any one' error-rate output (open collector)

fitted to 25 way D type socket (SKB)

Displays:

(i) 3 error rate displays
(ii) 6 comparator 'ok' LEDs (green)
(iii) 6 'mute active' LEDs (red)
(iv) 1 2048 lock LED (green)
(v) 3 676 lock LEDs
(vi) 16 status LEDs showing copy of above monitoring outputs

Mechanical Data:

PA1/146 (2 off CD3L/58)
Chassis: 6U Eurocard Subframe (19 inch rackmount) 400 mm deep
Weight: 15 kg equipped with all plugins.

Installation data:

Power requirements: 240 V AC @ less than 100 VA
Chassis extender: CH4/15

Before the unit is put into use, there are several links and switches to adjust depending on operating conditions. The maximum bit error rate that will be accepted before an error is reported must be set. Cosited or interleaved sampling schemes are link selectable. The settings of these items is covered in Sections 3. and 4. below.

3. OPERATION

3.1. Power Supplies

The unit is mains powered from socket U via an LNE type mains connector.

3.2. HDB3 Input

The 2048 kHz HDB3 input goes into BNC socket C where it is terminated in 75 Ω.

3.3. Sampling Scheme

Before operation, the sampling scheme must be specified. There are two links on the UN26/100 for specifying the scheme for the main and reserve outputs. When the link is in the upper position the scheme is cosited, when in the lower position the scheme is alternate. The top link (LK1) affects the main outputs and the bottom link (LK2) the reserve outputs.

3.4. Comparator Links

The audio outputs from the system are duplicated and there is a comparator checking each pair of supposedly identical outputs. The CPU monitors the signals from the comparator to allow fault monitoring. The comparators for the first three channels are situated on the left hand C09/13 and those for the remaining three channels are on the right hand card. For normal operation, the links should be set up as follows:

Left-Hand card:

LK162, 262, 362:	REMOVED
LK161, 261, 361:	Position A
LK164, 163, 142 141, 264, 263, 242, 241, 364, 363, 342, 341:	Position A

Right-Hand card:

LK162, 262, 362:	REMOVED
LK161, 261, 361:	Position A
LK164, 163, 142 141, 264, 263, 242, 241, 364, 363, 342, 341:	Position B

4. LINE-UP PROCEDURES

There are few operator controls on MKII NICAM, but before a decoder is commissioned its input bit error tolerance must be set.

4.1. Error Thresholds

There is a facility for setting the maximum error rate that is considered acceptable for each channel and for each channel pair. If the threshold for an individual channel is exceeded the channel is flagged as failed. If the threshold for a channel pair is exceeded, a Bit Error Rate (BER) warning is flagged. There are nine switches on the front of UN26/99 for setting these parameters. Valid settings are between 2 and 7. Values 0 and 1 will never cause an error to be flagged, values 8 and 9 will cause a permanent fault to be reported.

The channel fails are 'slugged' so that a high error rate must exist for greater than 1s before the channel is failed. The BER outputs are not slugged in this way as they are only used as warnings, meaning that a short loss of bitstream will cause a warning but the channel will not be de-commissioned. The switches should be set up so that the particular bitstream must deteriorate considerably before a fault is reported.

If a link shows a very high bit error rate this should be investigated rather than setting a low tolerance for the link. The allocation of the switches is as follows:

TOP:
- □ CHAN.1 max error rate
- □ CHAN.2 max error rate
- □ CHAN.3 max error rate
- □ CHAN.4 max error rate
- □ CHAN.5 max error rate
- □ CHAN.6 max error rate
- □ X max error rate
- □ Y max error rate
- □ Z max error rate

5. CIRCUIT DESCRIPTION

The hardware of the MKII NICAM decoder is described graphically on D63598A1 and can be broken down in blocks as follows:

- o Power Supply
- o Clock and Data recovery
- o 2048 Locking
- o Sequencer
- o 676 Locking
- o System RAM
- o Gate Array block
- o CPU block
- o Executive outputs
- o Error counting system
- o Signalling bits
- o DAC block
- o Muting systems
- o Analogue outputs
- o Audio comparators
- o AES/EBU outputs

5.1. Power Supply

The power supply for the CD3L/58 is a switch mode unit the PS4/51 which provides +5 V at up to 10 A and ±18 V at up to 1.5 A each subject to a maximum loading of 75 W. A commercial module is used which is modified by removing R57 and R58 - if this is not done, the ±18 V supplies will be low (nominally ±15 V).

The unit is protected by a 3.15 A mains fuse and all supplies are output current limited. The power is distributed within the crate via the upper connector on the backplane. The digital and analogue grounds are joined by a link inside the actual power supply.

Supply	Pin No.
+18 V	2
-18 V	3
0 V(A)	4 & 5
+5 V	29 & 30
0 V(D)	31 & 32

All supplies are short circuit proof. The 5 V adjustment inside the actual PSU is factory set; it can be adjusted with a trimmer having first removed the PSU covers. See section 6.1. for details.

5.2. Clock and Data Recovery

This portion of the circuitry is located on the UN26/99. Refer to the circuit D62630A1 and block diagram D63603A3. The HDB3 input is a 3-level signal, with positive and negative excursions which are symmetrical about 0 volts. The peak-to peak amplitude is 4.74 volts. The amplitude of this incoming signal is monitored by means of the peak-to-peak rectifier, D5, D7, and the DC output of this rectifier is fed to the inverting input terminal of the voltage comparator U9. The other input of the comparator is a reference voltage, and hysteresis is provided by the feedback network D6 and R16. Thus, when the input signal level is below a pre-set threshold, the output of the comparator U9 is high (and flags a fault). This output is fed via an open collector transistor to socket SKB. When the input level reaches a satisfactory value, the output of the comparator goes low.

The incoming data waveform is sliced at the half-amplitude points by two comparators (within the dual package, U8) one of which deals with the positive part of the waveform, and one of which handles the negative part of the waveform. The reference levels for the comparators are provided by two rectifiers, which each provide DC of half the peak pulse amplitude. The slicing level of the comparators is in this way made adaptive to variations in incoming signal level, and is always at half-peak amplitude.

Half-amplitude is determined by R4, R9. The rectifiers are of the "infinite impedance" type, comprising an emitter-follower, with capacitive load C5/C6, as rectifier, followed by a complementary emitter-follower, so as to give first-order cancellation of Vbe potentials. The comparator outputs are two unipolar data streams, corresponding to the positive and negative parts respectively, of the HDB3 waveform; this is the format required by the following code-converter.

The HDB3 code contains a relatively high component of clock frequency: 2048 kHz. The CK output of the code-converter chip U10 supplies logic-level clock, but it is intermittent (depending on transmitted words) and has any jitter present on the incoming signal. The clock component is made continuous by a (low-Q) resonant circuit, L4, C11, which rings at the clock frequency. This resonant circuit is excited by the switched current source Q4/Q5, the current being determined by R13. The amplitude modulated sinewave across L4, C11, is coupled via C10, and the phase-shift network R51, C64 to the comparator U9, which slices the continuous sinewave at its zero crossings to provide a first continuous TTL clock.

This first recovered clock jitters in sympathy with the incoming data, and is therefore suitable for clocking the incoming data into the code converter U10, at pin 5; and for clocking data into the buffer store within U1 (U1, pin 8).

Data is clocked out of the FIFO buffer store U1 at a constant rate which is controlled by the crystal XL1, and by circuitry internal to the CS61600 chip, U1. The crystal oscillator actually operates at 4 times 2048 kHz, and the stable 8192 kHz waveform which is now frequency locked to the incoming data rate is 'squared up' by the CMOS inverter U6 to provide logic level system clock at U6 pin 4. A matching network on the input to U6 ensures the loading on the crystal is purely resistive.

The jitter reduction provided by U1, enables the system to operate from digital bearers such as provided by British Telecom which have jitter characteristics complying to CCITT G823.

5.3. 2048 Locking

Locking to the NICAM data stream at the 2048 kbit/s level is performed on the UN26/99. Refer to diagram D63602A3 for the block diagram. The circuitry comprises of: U33, 34 shift registers, U30 DETECTOR PAL, U27 MONITOR PAL, U32 MONITOR PROM, U29 latch and U28 'AND' gate.

Each of the 2048 frames starts with a frame alignment word. The frame alignment word (FAW) is one of the two 7-bit patterns defined in the NICAM 3 specification as FAW0 and FAW1 and alternates between FAW0 and FAW1 every frame (see DSK21831A2). Assuming the decoder is out of lock at the 2048 level, the 2048 bit shift register (U33,U34) and two 7 bit shift registers (U29 and one inside the DETECTOR PAL - U30) are used to "take a snapshot" of two 7-bit words of the incoming bitsream which are spaced by 2048 bits. The DETECTOR PAL looks at these two words and pulses its /DDET (double detect) output when they are FAWs of different type.

The /DDET output loads the sequencer counter (see section 5.4.) with 0000 000D 0010 0100. This ensures that the sequencer is 'locked' to the 2048 bitstream - i.e the sequencer count of zero will coincide with the beginning of a 2048 frame. After that the DETECTOR PAL switches into "single detect" mode. Now it only looks at one of the 7-bit words and pulses the /SDET (single detect) output when the internal 7 bit shift register contains a FAW of the expected type. (There is a flip-flop in the DETECTOR PAL that dictates the type of the frame alignment word expected for the next frame. This flip-flop is clocked every 1 ms by the /EOC (End of count) signal from the sequencer.) /DDET is now disabled for as long as the system stays in lock.

The aim of the 2048 locking system is to synchronise the sequencer to the incoming bitstream so that the sequencer is in state zero when the first bit of the 2048 frame arrives. The /DDET pulse sets the sequencer to a certain state. The sequencer will then provide a pulse (/EOC) every 1 ms which is expected to coincide with /SDET output pulse of the DETECTOR PAL. The MONITOR PAL (U27) and MONITOR PROM (U32) check that the pulses coincide at least 'n' times out of 't' before deciding that the system is in lock. Otherwise the PROM would issue a relock pulse to the DETECTOR PAL (U30) and the locking cycle would start again. Once in lock, the D0 of the PROM goes low and the PROM enters "in lock mode" where it would take 'm' "bad frames" out of 'k' to issue a relock pulse to the DETECTOR PAL, thus re-enabling /DDET generation.

Parameters m, n, t and k are determind by the software that creates the MONITOR-PROM. At present, n = 4, t = 5, m = 7, and k = 9.

DETECTOR PAL (U30)

This PAL is used to detect occurences of frame words in the NICAM 3 bitstream. The PAL has access to the bitstream in two 7-bit windows 2048 bits apart (register S (U29) - external and register P - implemented inside the PAL). After being cleared by the CLR line from the MONITOR PROM when a reload is needed, the PAL waits for valid frame words of the opposite sense in shift registers P and S. Once they are detected /DDET outputs a pulse, SNGL is set and OLDF takes the sense of the FAW in P register (SNGL and OLDF are signals generated and used inside the PAL).

From now on the PAL looks for a FAW in the P register of the opposite sense to OLDF. The sense of OLDF is toggled by the /EOC signal from the sequencer, so each time the sequencer count 'overflows' and resets to zero, the DETECTOR PAL will look for FAWs of the opposite sense. Whenever it finds one, it will pulse /SDET and the MONITOR PAL will check that a FAW appears at the same time as /EOC to confirm the 2048 kbit/s lock.

MONITOR PAL (U27)

This monitors good/bad frames of the 2048 kbit/s stream. The outputs of Q0 to Q8 represent the last nine frames: Q = 0 means that a frame alignment word of the correct sense arrived when expected (i.e the frame was "good"). For example, Q8 - Q0 = 0001 000D0 means that last five frames were "good", the frame before that was "bad" and the rest of the nine frames were "good".

The PAL has two logically independent parts: a 9-bit shift register and a 1-bit latch. The 9-bit shift register clocks whenever /EOC goes low and is fed with a zero if /SDET and /EOC and are low together (ie a FAW arrived when expected), or a 1 otherwise. The /CLR line is used to set the 9 outputs to the state 100011111 on the next positive clock edge whenever a 'relock' is sent from the monitor PROM. The 1-bit latch is used internally to decide whether the PAL is looking for /SDET and /EOC low together (in lock) or /DDET pulses (out of lock). When /DDET is used to force a lock, the state of the shift register output is set to 010011111.

5.4. Sequencer

The sequencer is the central control unit that controls the activity of the decoder signal processing hardware by driving the system address and system control busses. It can be thought of as a 'hardware CPU' where the instructions it executes are the outputs of the five resident PROMS and the program counter is the output from the sequencer counter chain. This operation is fairly straightforward as the 'program' is linear code with no breaks or jumps (except during relocking). The sequencer issues instructions at the same rate as the incoming 2048 kbit/s bitstream i.e one instruction per 488 ns. The 488 ns intervals are called sequencer slots. The sequencer executes 6144 commands (each taking 488 ns) before the sequence starts repeating. The sequence is repeated at the same rate as the 676 level frame duration - 3ms.

The sequencer is the main digital part of the system; it controls most of the digital components and resides on the UN26/100. Some of the components of this circuit are counters U2, 3, 4, 5 and and gate U1. The count of the sequencer is designed to start at the beginning of the 2048 data frame.

The count is clocked at 8.192 MHz giving a total of 6144 states in the 3 ms frame. PROM U10 advances the sequencer count by 0, 2048 or 4096

states depending on the state of A2 and A3 which come from the CPU and is used for delay fixing through the decoder. When the system is locking to the incoming bitstream the counter is preset to 0000 0000 0010 0100 when /DDET is received. Once in lock the counter is reset to zero every 3 ms by the output of IC1a.

The rest of the sequencer circuitry consists of:

64k PROMs U11, 26, 34, 43, 57 and latches U36, 44, 58.

The counter chain addresses the five sequencer PROMs three of whose contents are latched. The outputs from these latches form the instructions that control the processing. Because these instructions follow a 3 ms pattern it is possible to use signature analysis where the start and stop signals are taken from the reset signal to the CPU and the clock is taken from the 2.048 MHz pin. The addresses and data can be checked this way. A list of expected signatures is given in Appendix 1.

The digital processing in the decoder is carried out by executing the instructions supplied by the sequencer. It issues instructions at 488 ns intervals. The sequencer has no read/write memory thus almost all instructions involve the use of the system RAM.

The are several types of sequencer commands and these are summarised as follows:

A	Locked word to RAM (P Slot)	The sequencer provides the output enables for the buffer in the 676 locking circuitry and supplies the destination RAM address (which depends on the sample and channel numbers). Housekeeping words are similarly loaded into the system RAM.
B	Gate array command	The sequencer provides the correct signals for the gate array and a system RAM address. This address is where to read a compressed sample from or write an uncompressed sample to depending on the gate array command.
C	Output sample to DAC	The sequencer provides a series of signals which clock the DAC Interface PAL and enable the correct mode for the associated serialisers. The sequencer also provides at the correct point a system RAM address from which the output sample is read.
D	Ƶ80 CPU timeslot	The sequencer has a number of timeslots which allow the Ƶ80 processor access to the system RAM. If the CPU tries to use the RAM outside of these 'windows', it will be forced by hardware into a WAIT state until the next CPU slot is active.

These commands are mutually exclusive; some have to happen at fixed slots (locked word to RAM) and some at a fixed rate (Output sample to DAC) but the others can be 'slotted in' where they will fit. The sequencer PROM generation software allows for 'prioritising' in this manner.

Another output from the sequencer triggers a monostable which provides the pulse to clock out the 2048 signalling bit data. Other functions are also controlled by the sequencer - for instance the 676 locking system

uses several lines to control the READ/WRITE COUNTER PALS. See section 5.4. for details of these slots (type R, W and Q).

5.5. 676 Locking

The 676 locking process is performed on the UN26/100. Refer to diagram 63599A1. The 676 locking system consists of: RECEIVE REGISTER PAL (U68), 2 kbyte RAM (U49), WRITE COUNTER PAL (U60), three READ COUNTER PALs (U47, 48, 61), SUB-CONTROLLER PAL (U67), six DESERIALISER PALs (U69, 70, 71, 72, 73, 74), a 3 to 8 line decoder (U62) and some output buffers (U63, 64, 65).

The 2048 frame consists of an FAW, signalling bits, spare bits (also called justification bits) and the data to convey six audio channels (see DSK21831A2). The three justification bits immediately following the signalling bit are allocated to cure the variable delay problem present in the MKI system (see later in this section). Once the sequencer is locked to the 2048 frame, it "knows" the assignment of each incoming bit and therefore can separate the bits that belong to each audio channel. The audio channel bits have a frame structure and each channel makes a 338 kbit/s frame. One 338 frame lasts 3 ms. However, two channels are combined by interleaving their bits so that channel B bits follow corresponding channel A bits to form a 676 kbit/s frame (see fig 1 on DSK21831A2). The 2048 frame contains bits for three 676 frames.

The NICAM 3 specification does not restrict the 676 frame to start in any particular place relative to 2048. Thus the beginnings of the three 676 frames can be delayed relative to each other by any amount. The aim of the 676 locking system is to delay each of the three 676 channel pairs so that to the rest of the signal processing hardware they appear to have their frames starting at a predetermined count of the sequencer.

The 676 locking system receives its relock command from the CPU (pins 2, 3, 4 of U6). The Z80 CPU monitors the number of parity errors per channel pair per frame. If this number is higher than a certain threshold, the CPU will issue RELOCK commands for those channel pairs that contain the large number of parity errors. A RELOCK is also issued if 2048 lock is lost. The 6-bit shift register (Receive register PAL U68) converts the incoming 2048 bits into 6-bit words where bit 0 corresponds to audio channel 1 and so on. Once a 6-bit word has arrived it is written to the RAM (U49) at the address provided by the "write counter" (U60).

The SUBCONTROLLER PAL puts itself and the deserialisers into the relock state when it receives a RELOCK signal from the CPU. Each channel pair is relocked independently. The DESERIALISER PALs have two modes of operation. The /OPMODE signal determines whether the PAL will search for a FAW (pin 4 high - out of lock) or will deserialise the audio data (pin 4 low - in lock). Another input CHA (pin 5) tells the PAL to look for A or B channel FAWs. The WRITE COUNTER PAL puts successive 6-bit words into consecutive RAM addresses and the READ COUNTER PALs take out the data again but with an addressing offset to time align the 676 channel pairs.

The offset is arranged as follows:-

When a 676 channel pair is out of lock the two associated DESERIALISER PALs search for FAWs of the correct sense and 'freeze' the outputs of the relevant READ COUNTER PAL when the FAWs are found.

The START signal (pin 5 of U67) is issued by the sequencer when it expects the deserialisers to have complete frame alignment words. If the channel pair is in lock the START pulse is ignored. If the channel pair is not in lock and the 676 FAWs are not detected, the START is also ignored. If the channel pair is in lock and the FAWs have been detected (thus 'freezing' the read counter), the START pulse will 'un-freeze' the counter and the next word read after the START pulse will be the FAW. Therefore START determines where in the sequence the FAW is read. The 676 frames have FAWs towards the end of the frame thus START is issued towards the end of the sequence.

Consider the three channel pairs together. Once locked the deserialisers output 10/9 bit words to the system RAM under the sequencer control. The output buffers (U63, 64, 65) "untwist" the sample words only, leaving the housekeeping words unchanged, (i.e the system RAM receives sample words with bits arranged in order from lsb to msb and sign bit). The sample words are stored left justified which means that the sign bit of a sample corresponds to the most significant bit of the data bus.

SUB-CONTROLLER PAL (U67)

When out of lock the SUBCONTROLLER PAL monitors the state of the deserialisers. When a pair of deserialisers signals (via D9 of their common bus) the receipt of frame alignment words, the subcontroller stops the corresponding read counter and changes the mode of the deserialisers from FAW detect to deserialise. The read counter is released when the subcontroller receives a /START pulse from the sequencer.

This device consists of three identical blocks - one for each channel pair. Consider the relock sequence for block X:

The CPU instructs the CH1/CH2 676 locking system to go into relock mode by issuing a /RELOCKX (U67 pin 3 pulses low). The PAL instructs the CH1 and CH2 deserialisers to go into detect mode (In this mode the deserialisers look for FAWs instead of deserialising). The SUBCONTROLLER PAL monitors the state of bit 9 of the deserialisers' bus on pin 6. The deserialiser for channel 2 will output a low level on D9 when both CH1 and CH2 deserialisers simultaneously detect FAWs. The /IDENTX input to the PAL (pin 7) signals when CH2 data is on the bus. Once the FAWs for CH1/CH2 are detected, the PAL issues a /STOPX signal to the READ COUNTER PAL for CH1/CH2 (U47) and changes the mode of the deserialisers for CH1/CH2 to deserialise. When the /START pulse is received from the sequencer, the PAL allows the READ COUNTER PAL to start counting again.

DE-SERIALISER PAL (U69, 70, 71, 72, 73, 74)

This PAL performs two functions depending on the state of the /OPMODE input (pin 4). The two modes of operation are :

De-serialising: (/OPMODE is low). In this mode the PAL is a 10 bit shift register with shift enable, clear and tri-state output.

Detecting FAWs: (/OPMODE is high). In this mode the lower 7 bits of the shift register are the same as above. However, in this mode Q7, Q8 and Q9 have special functions:

Q7 becomes active (low) when Q0 - Q6 contain FAW0, Q8 becomes active (low) when Q0 - Q6 contain FAW1 and Q9 becomes active (low) when Q0 - Q6 contain FAW0 and the /DFAW0 (pin 7) input is active (low), or when Q0 - Q6 contain FAW1 and the /DFAW1 (pin 6) input is active (low), provided /DFEN (pin 9) is active. Thus when the deserialiser PAL is used for channel B of a channel pair, the Q9 output signifies that chA and chB de-serialisers have FAWs of same sense. (DFAW0 and DFAW1 are taken from Q7 and Q8 of the chA de-serialiser).

RECEIVE REGISTER PAL (U68)

This device has two independent blocks:

1 A Serial-to-parallel converter. A six bit shift register reads the 2048 input bitstream when the clock is enabled by /CKEN (pin 5). The sequencer controls /CKEN and ensures that the shift register reads only the 676 level bits of the 2048 bitstream, thus ignoring all the 2048 level housekeeping bits. Once the shift register is full the sequencer loads the 6-bit word to the 2 kbyte RAM by driving /OE (pin 13). Thus the 8 bit RAM word is allocated as follows: bit 0 - channel 1, bit 1 - channel 2 etc. (bit 6 and bit 7 are not used).

2 A 2048 signalling bit latch. This latch is clocked by the sequencer (using the /SIGEN input - pin 8) and stores the 2048 level signalling bit (SIGOUT - pin 14).

COUNTER PAL (U47, 48, 60, 61)

This PAL is a 10 bit modulo- 1014 'up' counter with tri-state outputs and a /STOP input. Internally it is a 'down' counter, but since the outputs are complemented it 'looks' like an 'up' counter. The counter counts up to 1012 then goes to 1023, missing 11 states, and then back to zero. When /STOP input is low the count is halted, when the /STOP line goes high again the count continues from where it stopped. This PAL is used for two purposes - write and read address count generation. When used as a write counter the PAL addresses the RAM and writes the 6-bit words from the RECEIVER REGISTER PAL. When used as a read counter, the PAL reads the 2 bit wide samples for a particular channel pair from the RAM and feeds them to the respective two DESERIALISER PALs. Therefore for the 676 locking system there are four counter PALs configured as one write counter and three read counters.

Sequencer Control Of 676 Locking

The sequencer allocates various slots to the 676 locking mechanism. The following is an explanation of these slots:

W slots: The six-bit word from the RECEIVE PAL (IC62) is written to the locking RAM at the address supplied by the write counter (IC57). The counter is then incremented. The six bits correspond to six channels; they are the six 676 level bits in the 2048 frame that arrived just before the write slot.

Rx slots: Deserialisers for channel 1 and 2 are loaded with one bit each from the locking RAM - address supplied by the read counter X (IC58).

Ry slots: Deserialisers for channel 3 and 4 are loaded with one bit each from the locking RAM - address supplied by the read counter Y (IC59).

Rz slots: Deserialisers for channel 5 and 6 are loaded with one bit each from the locking RAM - address supplied by the read counter Z (IC60).

Q slots: The six DESERIALISER PALs share a common output bus. During a Q slot, one of the PALs has its output enabled and places data onto the bus. A Q slot is used for two different purposes depending on whether the system is locked or not.

During 676 locking, the two deserialisers for a channel pair use bits 7, 8, and 9 of their common bus to communicate with each other and the SUB-CONTROLLER PAL. Consider the locking process for channels 1 and 2:

> The next slot after deserialiser 1 was loaded with the last bit in the frame alignment word it reports via the output bus (bit 7 or 8) to the deserialiser 2 that it received a frame alignment word and the sense of that word, (i.e bit 7 low = FAW0 , bit 8 low = FAW1). If the deserialiser 2 also has a frame alignment word of the same sense then the at the next slot it reports to the SUBCONTROLLER PAL (bit 9 of the bus) that channel pair X detected frame alignment words in both channels.

To summarise, during locking the two Q slots following the deserialiser pair load are used to enable frame check signalling between the left and right deserialisers and between right deserialiser and the subcontroller.

Once a channel pair is locked most of the Q slots for that channel pair are redundant. However the slots that coincide with a P slot (see later) enable the deserialiser to output its data (10 bit sample word or 9 bit housekeeping word) through the buffers to the system RAM (IC25, 26).

P slots: The buffers to the system bus open when a deserialiser writes a word to the system RAM. The sequencer produces a P slot when a deserialiser has a 9/10 bit word ready and a deserialisers' output (Q slot) is enabled.

Each W slot will be followed by three R slots - one for each channel. An R slot does not necessarily read the data written at the preceding write slot. The delay between writing a bit from the RECEIVE REGISTER PAL and reading it back to the deserialisers is called the locking delay. In fact all the 676 locking system does is to adjust the delay for each channel pair so that the rest of the decoder sees the three 676 frames starting at the beginning of the sequencer sequence.

Slot types R and W both use the locking RAM address bus and are thus mutually exclusive. However, since the RAM data and address buses are separate from the deserialiser common output bus, slot types P and Q can happen at the same times as each other or during an R or W slot. R, W and Q slots do not use the system RAM and can happen at any point without conflicting with the sequencer commands detailed in section 5.4.

CODEC DELAY

The 676 locking mechanism delays the channel pairs so that the 676 frames start at the same time. A 676 frame lasts 3 ms so a channel pair may be delayed by any amount up to this time. Coder and decoder digital processing takes 6 ms each and the digital oversampling filter in the decoder (SAA 7220) introduces about 800 µs delay. An additional delay of 1 msec occurs in the 2048 locking giving a total codec (MKII equipment) delay of between 13.8 and 16.8 msec.

This variation in delay is not satisfactory when two transmitters radiate to the same service area. The codec delay can be fixed at 13.8 ms by using some of the otherwise unused justification bits in the NICAM 3 bitstream to mark one of the three 2048 frames within a 676 frame (see DSK 21831A2). This is achieved in the MKII equipment as follows:

The MKII coder multiplexes the three 676 frames into the 2048 frame in such a way that they start in the same place - at the beginning of one of the 2048 frames. The decoder always locks its sequencer so that the beginning of the sequence coincides with the beginning of a 2048 frame. Thus there are three possible locked states:

A The sequence starts at the beginning of the 2D48 frame in which the 676 frames start.

B The sequence starts at the beginning of the 2048 frame <u>after</u> the one in which the 676 frames start.

C The sequence starts at the beginning of the 2048 frame <u>before</u> the one in which the 676 frames start.

In case A there is no additional delay due to the 676 locking circuitry, but in cases B and C an extra delay of 1 or 2 ms is added.

Clearly, to fix the delay every third 2048 frame should be "marked" so that the sequencer can then be "told" which 2048 frame should coincide with the beginning of the sequence. The three justification bits immediately following the 2048 signalling bit are used to "mark" the 2048 frames.

The three justification bits are all ones for one frame and then all zeros for the next two 2048 frames (in the MKII coder only). The CPU of the decoder reads the marked bits during the sequencer cycle - i.e three 2D48 frames. (The bits are shifted into a shift register - U48 on the UN26/100 - under sequencer control and then read in, in parallel form by the CPU).

On the basis of the marked bits, the CPU can decide if the sequencer 'phasing' needs to be adjusted. The CPU can advance the sequencer by 2048 or 4096 states simply by changing the state of the A_2 and A_3 lines of the DELAY FIX PROM (U10 on the UN26/100). This PROM alters the top two bits of the sequencer 13 bit address and so can advance the sequencer without disturbing the 2048 level lock. The 676 lock is disturbed (a relock command for all three channel pairs will be issued by the CPU) and therefore the above described procedure will disturb the audio output. The CPU checks all the relocking bits are consistent (ie. 6 bits must be in error out of 9) before undertaking this process. The MKII NICAM codec delay is thus fixed at 13.8 ms plus a small delay in the analogue anti-alias input filters (about 350 µs).

PARALLEL PROCESSING

There are three processing stages which can be regarded as "pipeline" stages. A 3 ms frame goes through each stage in turn in the decoding process. However there is only one central control element, the sequencer, which issues one command at a time. Therefore the pipelining is achieved not by parallel processing but by time multiplexing (or interleaving).

Within the sequencer is a 3 state counter that is clocked at the end of the 6144 sequence. The counter maps the logical page of the system RAM to the physical one. For example, the CPU and Gate-array always address page 2, samples from the locking system are read into page 0 and the DAC is loaded with the samples from page 1. The above page numbers refer to logical pages.

This page adjust counter makes sure that the logical to physical page mapping is such that the 96 samples (one 338 frame) for each of the six channels progresses through the pipeline stages in the correct order. The Gate-Array, DAC and the locking mechanism are controlled by the sequencer whereas the CPU executes the instructions in its program PROM quite independently of the sequencer, except when it wants to use the system RAM at the same time as the sequencer. In this case, the CPU is made to wait for RAM access until the next CPU slot. Any CPU instruction that doesn't need the system RAM causes no conflict.

5.6. System RAM

The system RAM is resident on the UN26/100 and consists of two 8 kbyte RAM chips (U15 and U30) which gives both 16 and 8 bit word access capability.

The system RAM address is 13 bits wide. Here is the breakdown:

	physical page no.	channel no.	channel workspace
bit:	12 11	10 9 8	7 6 5 4 3 2 1 0

(e.g. address 0100100000000 corresponds to page one and channel one.)

The area that would be occupied by channel 0 is used as a general workspace to store the signalling bits for all 6 channels as follows:

sample 0 space (ls byte) : Signalling word for ch.1 and 2
sample 0 space (ms byte) : Signalling word for ch.3 and 4
sample 1 space (ls byte) : Signalling word for ch.5 and 6

The signalling word is 8-bits wide. The four least significant bits are the signalling bits for the odd channel number and the four most significant bits are for the even channel number. The 256 byte blocks of channel workspace for channels 1 to 6 are allocated to the six NICAM channels divided as follows:

Bytes	Usage
0 - 95	: not yet processed samples
100 - 131	: 32 parity bits, lsb of each word
140 - 142	: three range codes
145 - 149	: parity bits arranged in words
150 - 156	: housekeeping words
160 - 255	: processed samples

(Channel space for channel 7 is not used.)

For the CPU to access the system RAM bit 15 of the address must be set, bit 14 is "don't care". Bit 0 enables access to the RAM by 8-bit wide words: if bit 0 is zero the lower portion of the 16-bit RAM word is accessed; if bit zero is 1 the high byte is accessed. This enables Z80's 16-bit load instructions to be executed on the system RAM.

The other components associated with the system RAM are the BUS-CONTROL PAL and the MISC PAL.

BUS-CONTROL PAL (U37)

This PAL controls access to the system RAM and the direction of the buffers that couple the CPU data bus to the gate array. The address to the RAM is provided by the CPU or the sequencer. The address is held by latches U14 and U29 which take their input from 2-input multiplexers U12, 13, 27 and 28. When the CPU accesses the RAM this PAL controls whether access is to the high or low byte RAM chip.

MISC PAL (U35)

This PAL controls the virtual to physical page mapping and CPU wait states. The RAM is split into four physical pages each of 2048 16 bit words. Physical pages 0 to 2 are allocated to pipeline stages 1 - 3 and the mapping is switched every 3 ms. Page 3 is a general purpose page and is not switched. The sequencer is responsible for changing the allocation of pages to pipeline stages every 3 ms in such a way that pages propagate through the pipeline.

The mapping between physical and logical pages is as shown in the following table.

Usage	Physical page			Function performed
	t	t+3	t+6 ms	
Locking system read (logical page 0)	page 0	page 1	page 2	Samples (unprocessed) fed to RAM
CPU and G-A (logical page 2)	page 2	page 0	page1	Samples processed and put back in RAM
DAC (logical page 1)	page 1	page 2	page 0	Samples read from RAM to DAC

The sequencer PROM generating software assigns page 0 to locking system reads etc. A PAL is then used to map the logical page number according to the 3 ms interval. The MISC PAL (U35) has an internal 0 to 2 counter which is clocked at the end of every 3 ms frame. The logical to physical page mapping is changed every 3 ms (at the beginning of the 6144 count sequence) according to the table. Page 3 is not switched and is used as scratch pad for storing bit error information.

When the CPU wishes to access the system RAM this PAL either grants the request, or if the sequencer (which has priority) is using it, the CPU is put into a wait state until the RAM is available.

5.7. Gate-array Block

The gate array block consists of a custom VLSI chip (gate-array) and a PAL. The actual gate array is used in both the coder and decoder and has an input pin to determine whether it is used to compress (coder) or expand (decoder) the input data. In the decoder the Gate-Array expands 10-bit samples into 14-bit samples and checks the parity. The PARITY DISPENSER PAL (U39), is used to convert parity words from the parallel format (the way they are stored in the system RAM) to serial (as required by the gate array).

The sequencer loads a parity word (first parity word is p1-p7, then p8-p14 etc. - see DSK21831A2) into the DISPENSER PAL at the correct slot so that the word is loaded by the time the gate-array requires a parity bit contained in that word. The PARITY DISPENSER PAL monitors the gate array commands issued by the sequencer and loads the word from the lower-byte of the system data bus when the sequencer issues an ARS (assess range of sample) gate-array command.

The ARS command does not affect the decompressing sequence of the gate-array (it is normally a command used for 14 to 10 bit encoding). The DISPENSER PAL will then supply a parity bit at the time when the gate-array executes the WPAR (initialise parity bit) command by monitoring the gate-array commands.

PARITY DISPENSER PAL (U39)

The PARITY DISPENSER PAL is a parallel to serial converter. It monitors the gate array commands issued by the sequencer and parallel loads from the system bus when the sequencer issues an ARS command. The gate array in decode mode ignores the ARS command but the PARITY DISPENSER PAL gets loaded with the next parity word. (The sequencer instructs the RAM to output the next parity word at the same time as it issues the ARS command). The PAL then monitors the gate array commands for WPAR. During this command the gate-array expects a parity bit for the next three samples to be present on its parity bus (pin 34) and the PARITY DISPENSER PAL provides that parity bit and then shifts in preparation for the next WPAR.

5.8. CPU Block

The CPU block is resident on UN26/99 with some I/O hardware on UN26/100. The main components are:

Z80 CPU (U40), 6116 RAM (U37), 27128 PROM (U41).

The CPU is responsible for the processing not done by the sequencer. The various roles it performs can be described:

- Calculation of error rates.
- Fixing delay of decoder.
- Controlling muting.
- Forcing channel relocks.
- Providing system diagnostics with fault reporting.
- Extraction of signalling bits

A reset is forced by the sequencer every 3 ms to prevent lock-up, and as a further protection the CPU must reset a monostable (U26 on the UN26/100) every 3 ms otherwise it will 'time-out' forcing all fault outputs bad. The CPU running program is stored in U41 and the private RAM for the CPU is U37 (both on the UN26/100). The system RAM U15, 30 (UN26/99) is shared by both the CPU and the sequencer and although the sequencer has priority if there is any contention, the CPU has certain slots where it can make use of this resource.

The CPU works independently of the rest of the hardware except when it accesses the system RAM. The sequencer allocates slots to the CPU and when the CPU wishes to access system RAM it is put into a 'wait' state by the sequencer until the next CPU slot. This process is transparent to the CPU program - the only drawback is that a system RAM access may have some wait states inserted by the sequencer. To minimise the time CPU wastes in the 'wait' state, all the data that does not need to be shared with the rest of the hardware resides in the private RAM. The CPU's memory map is as follows:

0000 - 3FFFH CPU PROM (27128 occupies 16 kbytes)
4000H - 7FFFH CPU private RAM (6116 occupies only 2 kbytes)
8000H - FFFFH System RAM (occupies 16 kbytes)

The system RAM as seen by the CPU is as follows:

	page	channel	channel workspace	switch
bit:	13 12	11 10 9	8 7 6 5 4 3 2 1	0

Bits 1 to 13 correspond to bits 0 - 12 of the actual system RAM chips.

The word size for the system RAM is 16 bits. Apart from the CPU all the functional blocks transfer a word at a time. The CPU transfers 8 bits at a time.

For the CPU to access system RAM bit 15 of the address must be set; bit 14 is "don't care". Bit 0 enables access to the RAM by 8-bit wide words: if bit 0 is zero the lower portion of the 16-bit RAM word is accessed; if bit zero is 1 the high byte is accessed. This enables Z80's 16-bit load instructions to be executed on the system RAM.

I/O ALLOCATION

UN26/99 OUTPUTS		Z80 port address (HEX)
SIGX	SIGNALLING BITS OF CHAN. 1 AND 2 (U55)	00
SIGY	SIGNALLING BITS OF CHAN. 3 AND 4 (U46)	01
SIGZ	SIGNALLING BITS OF CHAN. 5 AND 6 (U47)	02
GEN_PORT1	STROBE,CLEAR ERROR PAL ERROR RATE BLANKING (U35)	03
GEN_PORT3	ERROR RATE DISPLAY CH.1 & 2 LSN, 3 & 4 MSN (ND3 and ND2)	05
GEN_PORT4	ERROR RATE DISPLAY CH.5 & 6 LSN (ND1)	06
OK_KICK	TRIGGER FOR GOOD SELF-TEST (U26)	07
MISC_OP1	COPY OF CH_FAIL ON FRONT PANEL LEDs (U42)	0B
MISC_OP2	COPY OF XS_ERROR ON FRONT PANEL LEDs (U36)	0A
UN26/100 OUTPUTS		
GEN_PORT2	MUTING, RELOCK AND DELAY FIX CONTROL (U6)	04
ERROR_XS	BIT 0 & 1 = CH1 OR CH2 XSERROR, BIT 2 & 3 = CH3 OR 4, BIT 4 & 5 = CH5 OR 6. BIT6 = ANY CH.FAIL, BIT 7 = ANY COMP. FAIL (U19)	08
CH_FAIL	BIT 0 = CH1 FAIL, 1 = CH2, etc, BIT 6 = ANY DIG FAULT, BIT 7 = /2048_LOCK (U17,18)	09
UN26/99 INPUTS SELECTABLE SWITCHES:		
CH_FL_1	LSN = ERROR RATE TO REPORT FAIL OF CH.1 (U54)	02
CH_FL_2	LSN = ERROR RATE TO REPORT FAIL OF CH.2 (U54)	03
CH_FL_3	LSN = ERROR RATE TO REPORT FAIL OF CH.3 (U53)	04
CH_FL_4	LSN = ERROR RATE TO REPORT FAIL OF CH.4 (U53)	05
CH_FL_5	LSN = ERROR RATE TO REPORT FAIL OF CH.5 (U50)	06
CH_FL_6	LSN = ERROR RATE TO REPORT FAIL OF CH.6 (U50)	07
XS_ERR_X	LSN = EXCESS ERROR ON CH.1 & 2 (U52)	08
XS_ERR_Y	LSN = EXCESS ERROR ON CH.3 & 4 (U52)	09
XS_ERR_Z	LSN = EXCESS ERROR ON CH.5 & 6 (U51)	0A
UN26/99 OTHER INPUTS		
LOCK_READ	BIT 0 = /2048 LOCK 1, 2, 3 = 676 LOCK (U51)	0B
COMP_READ	6 LSB'S = 6 INPUTS FROM COMPARATOR (U43)	0C/0D
JUSTREAD_PORT	JUSTIFICATION BITS READ FOR DELAY FIXING (U48)	00/01

5.9. Executive Outputs

There are 23 executive outputs from the crate, these appear on socket B which is a 25 way D type (see D62190A1). All the signals are output by the CPU except one (/HDB3_ok). They are all open collector outputs, where the open circuit condition indicates a fault.

The various fault indications are:

1) Individual channel fails: (CHnFAILA and CHnFAILB when 'n' is the channel number)

This error indication is set if any channel is not reliable. Each output is duplicated to ease equipment change-over switching when a fault is reported. If the system cannot lock onto a channel pair it is set as failed (failure at 2048 level results in all channels being flagged as bad). There are nine decimal switches on the front of the unit and the top six of these set the maximum permissible error rate that will be accepted for each channel (see below).

If this rate is exceeded the channel will be flagged as in error. Because error rates are only calculated between 1 in 10^2 and 1 in 10^8, the switch values outside this range are accounted for as follows: Values 0, 1 and 2 never cause an error to be flagged. Values 8 and 9 always flag an error. Each channel has a duplicated audio output with a comparator which monitors the two identical output halves and triggers a channel failure if a difference is found. Also, if the system testing finds an error, all channels will be failed. There is a 'watchdog' that the CPU must write to every 3 ms; if this doesn't happen all channels will be failed.

2) Channel pair bit error rate failures: (CHnBER where 'n' is the channel number)

There are six of these outputs, two for each channel pair. They are triggered if the error rate for a channel pair is higher than the threshold set on one of the bottom three decimal switches.

The allocation of the switches is as follows:

TOP:
CHAN.1 max error rate
CHAN.2 max error rate
CHAN.3 max error rate
CHAN.4 max error rate
CHAN.5 max error rate
CHAN.6 max error rate
X max error rate (CHAN.1/2)
Y max error rate (CHAN.3/4)
Z max error rate (CHAN.5/6)

3) Comparator failure

These signals are produced on the C09/13s and passed to the UN26/99. If any of the comparators are in error then there are LEDs on the C09/13 that signal this. When a comparator fails the relevant channel is flagged as faulty as indicated by a LED on the front of the UN26/99, (see below).

4) System testing failure

This output becomes active when the internal self-test procedure shows up a fault. The digital fault LEDs on the front panel of the UN26/99 indicate the fault and all channels are flagged as bad.

5) Bitstream failures

If lock is lost at 2048 level then all channels are flagged as bad. If lock is lost at the 676 level then the relevant channels are flagged as bad.

The information contained in the executive outputs is also displayed on the LEDs on the front panel of the UN26/99. The allocation looking from the front is:

2048_lock ⊙ ⊙ Any comp fail
Dig_fault ⊙ ⊙ Any channel fail
CH.1 fail ⊙ ⊙ X BER error
CH.2 fail ⊙ ⊙ X BER error
CH.3 fail ⊙ ⊙ Y BER error
CH.4 fail ⊙ ⊙ Y BER error
CH.5 fail ⊙ ⊙ Z BER error
CH.6 fail ⊙ ⊙ Z BER error

5.10. Error Counting System

The system must be capable of detecting errors in the bitstream. This is done by parity checking. The NICAM format states that each parity bit protects the five msb's of three samples. There are therefore 32 parity bits for each 3 ms frame (96 samples). If one of these parity bits is in error then three samples are flagged as bad.

The gate-array checks the parity bits of the incoming audio data. During the RSP command execution it outputs the parity good/bad flag together with the decompressed sample that the parity bit protects onto the system data bus. The ERRCOUNT PAL (U40 on the UN26/100) monitors the gate-array commands and increments an internal 8-bit counter when the RSP command produces a parity bad result. After processing each channel, the error count is written to system RAM.

At the end of each frame therefore the system RAM contains six cumulative values from which individual channel error counts can be calculated. The CPU must then perform some arithmetic to convert these values into error rates.

ERRCOUNT PAL (U40)

This PAL counts the number of parity errors as flagged by the gate-array during one frame of processing of the six channels. It is an 8-bit counter which is clocked when the gate array executes the RSP command (read stored parity and sample) and the parity flag indicates an error. The counter is cleared at the beginning of each 3 ms frame. The output of the counter is connected to the low byte of the system bus and is tri-state.

After processing the samples for each channel in the gate-array, the sequencer reads the state of the counter into the system RAM. (The PAL monitors the gate-array commands and enables its tri-state outputs when a WRAN gate-array command and RAM write are issued by the sequencer. The gate-array will not get upset by the WRAN command which loads the range code register with a value that will be overwritten before the next samples are processed). Thus at the end of the six channels worth of processing by the gate-array the system RAM will contain the six states of the error counter - the cumulative count after each channel.

These values are kept in page 3 of the system RAM and are actually 3 times the number of errors since the gate array executes an RSP instruction, once for each of the three samples covered by one parity bit. In other words, one bit in error causes the error counter to increment the count by 3. The CPU now has enough information to work out individual channel errors per frame:

(Say the cumulative counts are C1, C2, C3, C4, C5, C6 then :

E1 = C1/3
E2 = (C2-C1)/3
E3 = (C3-C2)/3
E4 = (C4-C3)/3
E5 = (C5-C4)/3
E6 = (C6-C5)/3

where En is number of parity errors, for channel n, detected during the 3ms frame). The CPU works out the errors detected during the previous frame at the beginning of a 3 ms frame using a software routine called ERRCOUNT. Division by 3 is done using an assembler generated table.

5.11. Signalling Bits

2048 LEVEL SIGNALLING

The RECEIVE REGISTER PAL has a latch which is used to capture the 2048 level signalling bit. This signalling bit occurs once every 1 ms and can therefore be used to send low data rate information. It is not utilised at present. The sequencer issues a pulse when the 2048 signalling bit is being received. The PAL latches it and makes it available on pin 14 until the next signalling bit arrives. This output is connected to PL1a 28 on the UN26/100. The trailing edge of a monostable pulse, triggered from the clock which latched the 2048 data bit, provides the associated strobe pulse (PL2c 26 on the UN26/99). Both signals appear on SKA (see D62190A1 for pinout).

676 LEVEL SIGNALLING

The NICAM bitstream has capacity for carrying signalling data together with the audio. With each channel there are four signalling bits sent every 3 ms. These bits are grouped into 8-bit bytes carrying the data for two channels with an associated strobe pulse indicating valid data. These bits are used for remote switching of transmitters and to convey RDS (Radio Data System) information. The CPU extracts these bits from the system RAM where the sequencer has placed them and sends them, together with the strobe pulse, to open collector output buffers. (U55, U46, U47, and Q7, Q6, and Q9 on the UN26/99). All signalling outputs are open collector type. All these signals and associated supply/common connections appear on SKA (see D62190A1 for pinout).

5.12. DAC Block

The DAC block is resident on UN26/100 with the actual DACs on the two CO9/13 cards. The DAC block consists of 18 XOR gates (U20, 21, 23, 24, 51, 52, 52, 54), 6 16-bit negative clock triggered parallel load shift registers (U25, 32, 42, 55, 66, 75), interface PALs (U41, 50), digital filters (U76, 77, 78, 84, 85, 86), serial I/O shift registers (U80, 81, 88,89), latches, (U79, 87) and buffers (U22, 82, 83, 90).

From here the data goes to the analogue cards for conversion. The DAC chipset used is the Phillips SAA7220/TDA1541 combination. These use I^2S as their data protocol which is a serial format consisting of four signals: data, data clock, word select and an error flag. These signals are generated by the DAC block. The data is converted from parallel to serial by a 74LS674 16 bit shift register which is loaded with a 14-bit sample word from the system bus under sequencer control. The XOR gates translate from NICAM sign and magnitude format to the two's complement format accepted by the filter.

The 16 bit shift registers convert from the parallel format of the sample word to the serial format expected by the filter chips. The INTERFACE PAL is used to provide the timing for the DAC block and to latch error flags. The error flag is stored in the system RAM together with the sample it refers to. The DAC interface PAL latches the state of the error flag for the duration of the sample output to the filter.

The latched flag is supplied to the filter on pin 4 (EFAB) and will cause interpolation if the current sample is in error. There is a muting facility so that when the CPU decides that the number of parity errors in a frame is too high (threshold is set in the software) it can smoothly switch the audio output off; see muting systems section. The data clock and word select are sequencer generated.

DAC INTERFACE PAL (U41,50)

This PAL provides DAC interface functions. It consists of two parts:

- o Serialiser control.
- o Error latching.

Serialiser control is according to the following table:

inputs				outputs				
So	S1	If0	If1	Ser 1	Ser 2	Ser 3	Mode	Action
1	0	0	0	0	1	1	1	load serialiser 1
1	0	1	0	1	0	1	1	load serialiser 2
1	0	0	1	1	1	0	1	load serialiser 3
1	1	x	x	1	1	1	0	idle
0	1	x	x	0	0	0	0	clock out data

The inputs in the above table are supplied by the sequencer. The error latching part of the PAL loads the ERR 'n' latch inside the PAL with the state of the PB input, (pin 4) when the serialiser 'n' is loaded with the next sample word. This bit is then used as the error flag to the interpolator.

COSITED/INTERLEAVED SAMPLING

The NICAM transmission specifies an interleaved sampling process which means corresponding left and right audio samples in the digital domain represent analogue values taken half a sample period apart in time. The digital filter and DAC in the CD3L/58 are designed for use in compact disc players employing co-sited sampling which produces no time difference.

It thus is necessary to delay the right channel audio data by half a sample period to achieve correct timing. The digital filter IC outputs a bitstream of serial left and right samples at four times the original sampling rate. Each sample is 16 bits long and there are two of them, so one half period of the original sample rate corresponds to (16 x 2 x 4)/2 = 64 bit periods at this 'over sampled' rate. The CD3L/58 can be selected to work with either interleaved or co-sited signals using links LK1 (main) and LK2 (reserve) on the UN26/100. This works as follows:

From the shift registers the data line passes through a selectable delay network that has the effect of delaying right channel samples by half a sampling period if alternate sampling is required; co-sited sampling passes the data straight through.

Describing channel 1:

The data (DABD) emerges from U76 and is passed to both the octal latch (U79) and dual 64-bit shift register (U80). If co-sited mode is selected, the /CLR line on the latch is held low which causes the three-state buffer (U82) to pass the DABD signal straight through.

When interleaved mode is selected, the /CLR line is held high. WSBD (which flags whether the next sample is for the left or right channel) is latched by U79. When this result is low, U82 is enabled and passes data through as for the co-sited case (left channel). When WSBD is latched high, U83 is enabled causing the delayed version of the data to be passed through (right channel).

5.13. Muting Systems

When the error rate exceeds on in 10^2, the CPU will mute the audio outputs. The oversampling digital filter ICs on the UN26/100 have a MUTE input pin (/MUSB pin 23) which the CPU takes low causing an exponential mute over about 30 msec. Because of the pipelining in the processing of the audio samples, (see section 5.4.), the CPU 'knows' it must mute almost 3 ms before the corrupt audio samples will reach the DAC. The digital muting is thus not fast enough and is augmented by analogue muting on the C09/13 cards.

The control logic is derived from an 'OR' of /2048_lock and /Mute_n (where 'n' is X, Y or Z); there is a time constant in this function to disallow multiple mute-unmute commands occurring in a short space of time.

This mute function is provided by the MUTE PAL which is resident on the C09/13. The attenuation is performed as a logarithmic function of time, so as not to cause objectionable 'thuds' or 'clicks'. The attenuation is provided by a complimentary pair of JFETs in shunt with the audio signal path.

When on, these provide a symmetrical resistance of about 25 Ω and have virtually infinite resistance when off. The complementary gate switching waveforms are provided by an operational amplifier with a gain of 2, in tandem with a unity gain inverter.

Thus, when the MUTE logic line is high (+5 V) the 'n' channel FET gate is at -10 V and the 'p' channel FET gate is at +10 V,and thus both FETs are off. When the MUTE line is active (low), both FET gates are at zero potential and both FETs are on, giving an attenuation of about 50 dB.

At the start and end of the mute period, the envelope of the audio signal follows exponential transitions with a time constant CR.≈1ms.

5.14. Analogue Outputs

Refer to diagram D63600A2 for the block diagram of the analogue stages used in the decoder. There are two identical cards. The input signals to each DAC are serial data (DABD), data clock (CLBD), Left/Right channel ident (WSBD) and system clock (XSYS). Each DAC package is a dual channel device. Those packages on the card in to the left-hand slot of the crate handle the six main channels in pairs; one pair per package. The uppermost chip (U703) handles channels 1-2; the middle one (U706) channels 3-4; and the bottom one (U709) channels 5-6.

Similarly, the card in the right-hand slot of the crate is associated with the six (identical) reference channels.

Comparison of the audio outputs from the main and reference signal paths forms the basis of DAC and analogue circuit fault indication: if there are no malfunctions, then the main and reference audio outputs are identical and the comparator outputs are zero.

The six comparators are split; three to each card. Links prepare the card for the particular crate slot. There are also six quality-check outputs, which are separately buffered versions of the main outputs. In the following circuit description, component references are given as, for example, UX01, where X refers to the channel number. See circuit D62640A1.

DC OFFSET INTEGERATOR

The DC offset is controlled by an auto-zero servo loop, comprising an integrator, (UX01 b), and a current source (QX01, QX04) which balances the current sink within the DAC. The non-inverting input of UX01 b is connected to zero-potential reference. Any difference in voltage between the reference and TPX03 creates an error output from the integrator, which modifies the current in the grounded-base current source QX04. This in turn influences the gate-source potential of QX01, and so controls the magnitude of the current source into the summing-junction UX01a, pin 2. The DC offset at TPX03 is thus dynamically controlled to zero, with limits of accuracy set by the input offset voltage of UX01 b (±3 mV).

A low offset voltage on the output is needed to prevent clicks during muting when the audio is shorted to 0 V.

J17 DE-EMPHASIS AND LOW PASS FILTER

The J17 network comprises RX03, RX04, CX01, CX02. The low-pass filter comprises RX05, the combination of RX06, RX07, RX08 and RX09, coils LX01, LX02 and capacitors CX03, CX04, CX05. The filter has a Gaussian response to the -6 dB point, so as to achieve a flat group-delay in the audio pass-band and a corresponding transient step response with very small overshoot. The -3 dB cut-off frequency is nominally 40 kHz, and the stop-band attenuation at four fold over sampling frequency, (128 kHz) exceeds 40 dB.

LINE DRIVERS

Each driver has a balanced output stage which provides a sending end source impedance equivalent to 45 Ω in series with 100 μH. This is optimum for driving un-terminated twisted pairs. The output stage can also drive into 600 Ω. LX03 is a common mode filter which prevents RF being fed back from the line.

Protection against accidental mis-connection or short circuits is provided by the positive temperature coefficient resistors (self re-setting fuses) RX14 and RX15 in conjunction with diode clamps and relatively low voltage shunt-regulated supplies.

DAC CHECKING

To enable checking of the DACs under dynamic conditions, the audio outputs are duplicated. A reference output is provided by full replication of the main audio chain: DAC, J17 de-emphasis, low-pass filter, and line driver. The comparators recognise a disparity between the main and reference outputs, indicative of a fault. Fault recognition outputs a flag to the monitoring system.

BALUNS AND PRECISION RECTIFICATION

The comparators require uni-directional signal inputs and these are obtained from precision full wave rectifiers fed with unbalanced audio signals. The unbalanced audio signals are derived by balance-to-unbalance converters which are fed from the balanced main and auxiliary output lines.

Refer to circuit D62640A1. The precision rectifier (UX63 and associated components) is fed from a balanced to unbalanced converter (UX61 or UX62). During negative half-cycles at TPX61/2, the first section of UX63 functions as a unity gain inverting amplifier. During positive half-cycles, the amplifier is disabled by reason of DX73/4, and the section of the waveform at TPX61/2 is fed directly to the voltage follower section of UX63 via RX65 and RX67.

5.15. Audio Comparators

The comparators are based on a self balancing bridge circuit, which monitors the main and auxiliary channel levels. The bridge is made up of four resistors; one of these is variable and comprises an Operational Transconductance Amplifier (OTA) configured as a current controlled resistor, whose resistance is determined by the current I_{abc} into pin 16 of the package (UX64).

The other half of the dual OTA package functions as a conventional differential amplifier used as a balance sensing amplifier, with its differential inputs (pins 2 and 4) connected to the output of the bridge. The balance error output of this amplifier is fed back to control the current controlled resistor, thereby forming a servo loop which maintains bridge balance.

The balance condition of the bridge (any bridge) is independent of the energising signal level. This is a crucial feature, because in this application, we have to make comparisons of dynamic programme material.

When the main and auxiliary programme channel levels are identical, the variable resistor arm of the bridge has a particular ohmic value for bridge balance in that condition. This resistor value corresponds to a particular control current I_{abc} which in turn corresponds to a particular (nominally zero) error voltage output from the balance sensing amplifier.

In the event that there is a disparity in the output levels of the main and auxiliary audio channels, the bridge automatically re-balances, but it will have a new and different ohmic value current controlled resistance. Hence, there will be a different control I_{abc} value, and a different (non zero) error voltage output from the balance sensing amplifier. This error voltage is fed to a window discriminator UX65. When the error voltage exceeds a pre-set threshold (1.36 V set by RX85-6-7-8 pins 4/10 of UX65) a "fail" logic flag is output from U712 and the green LED (DX78) is extinguished.

Testing and setting-up is facilitated by two links, LKX61 and LKX62. When LKX61 is in position B, the bridge is energised from one source (simulating identical main and auxiliary levels). When LKX62 is made, a controlled error (imbalance) is introduced, and this can be used to test the fail detection circuits.

5.16. AES/E8U Outputs

As well as providing six channels of analogue audio, the CD3L/58 also provides digital audio AES/EBU outputs at 32 kHz rate. The six XLR connectors on the back panel (PLA-PLF) carry two sets of three AES feeds (channels 1/2, 3/4 and 5/6). There are two sets to enable external comparator monitoring for checking system performance. If one of the feeds fails then an external automatic monitoring system should be used to switch to a spare decoder.

The Philips SAA 7220 ICs, (U76-78 and U84-86), provide an output on the DOBM line, (pin 14), which is close in format to an AES/EBU signal. Minor changes to the bitstream convert the channel status data from consumer to professional format. The circuit is based to do this around two PALs, a buffer and a transformer providing a balanced earth free output as required.

EBU 1 PAL

This PAL takes the digital output from the SAA7220 and detects framing patterns. Because they are a bi-phase violation this is fairly straightforward.

The preambles are:

B: 11101000 - left sample, block start
M: 11100010 - left sample
W: 11100100 - right sample

The PAL contains a counter that is incremented every time a left channel sub-frame is detected and reset when a block sync occurs (every 192 frames). There is a look-up table inside EBU_1 that equates frame number to channel status bit.

If the incoming bit is different to the 'computed' value then the channel status bit for that frame is inverted. This also means that the parity bit must be inverted also. This inversion is controlled by EBU_2.

The 'C' bits set are: bits 0, 2, 3, 4, 6, and 7 of byte 0.

All other bits are zero, except the checksum which is 03.

This pattern of 'C' bits corresponds to:

PROFESSIONAL FORMAT
NORMAL AUDIO MODE
J17 PRE-EMPHASIS APPLIED
SAMPLING FREQUENCY LOCKED
32 KHZ SAMPLING

EBU_2 PAL

This PAL inverts the 'C' and 'P' bits in the outgoing bi-phase encoded bitstream under control from the EBU_1 PAL. In bi-phase coding, transistions in the output waveform always occur at bit cell boundaries and, if the output bit cell represents a logic '1', there is an extra transistion in the centre of the bit cell. Inverting the output signal during either half (but not both) of a bit cell period will invert the sense of the bit carried within the cell by adding or removing a central transistion.

The PAL contains an half-bit cell counter that is incremented at 4096 kHz. The data rate is 2048 kHz and it is Bi-Phase encoded. An AES sub-frame contains 32 bits (4 framing, 24 audio data V, U, C, P bits) giving 64 half-bit cells (0 to 63). To invert the C and P bits half-bit cells 61 and 62 are inverted, corresponding to the last half of the 'C' bit and the first half of the 'P' bit.

6. MAINTAINANCE

ROUTINE MAINTAINANCE

No routine maintainance or line up procedures are required for this equipment.

FAULT FINDING

As detailed in Section 5., there are 16 main blocks in the MKII NICAM decoder circuitry. These are:

	Block	Sited On
1	Power Supply	PS4/51
2	Clock and Data Recovery	UN26/99
3	2048 Locking	UN26/99
4	Sequencer	UN26/100
5	676 Locking	UN26/100
6	System RAM	UN26/100
7	Gate Array Block	UN26/100
8	CPU Block	UN26/99
9	Executive Outputs	UN26/100 and UN26/100
10	Error Counting System	UN26/100
11	Signalling Bits	UN26/99 and UN26/100
12	DAC Block	UN26/100 and CO9/13
13	Muting Systems	CO9/13
14	Analogue Outputs	CO9/13
15	Audio Comparators	CO9/13
16	AES/EBU Outputs	UN26/99 and UN26/100

The above block numbers are the same as the subsection numbers in both this section and the CIRCUIT DESCRIPTION section. They are also used on the overall block diagram D63598A1.

Items required for maintainance are:

1. CH4/15 Extender board
2. Dual Trace Oscilloscope (50 Mhz or better)
3. Variable Frequency Oscillator (range 2048 kHz ± 1 kHz)
4. Frequency Counter (> 10 MHz)
5. GE5P/9 NICAM Test Signal Generator
6. HP5006A Signature Analyser
7. Low Distortion 1 kHz Oscillator and Distortion Measuring Equipment
8. Coder (for companding noise test only)
9. 14 kHz Notch Filter (for companding noise test only) (See Appendix 3)

For many of the tests, Network Bitstream can be used instead of the GE4P/9. For tests of the analogue parts of the equipment, the GE4P/9 must be fitted with EPROMs producing an output which corresponds to the 'new' line-up levels (+14.8 dBu at 2 kHz = maximum coding range).

The last two items of equipment should not be needed for any on site tests - suspect units should be returned to base maintainance centres.

In general, if a crate is not functioning, try to identify the area at fault by card replacement (remembering to de-power the crate before replacing sub-units).

The sequencer is responsible for most of the digital processing in the system and a fault in this part may manifest itself as a difficulty in any of the following sections. The CPU block can also produce 'widespread' faults by issuing erroneous relock signals or forcing mutes due to problems in the error counting system. There are several other minor dependencies but, in general, the blocks can be tested for correct operation in the order given above; eg, once the 2048 locking has been proved to work, the sequencer can be tested and so on.

The following sub sections give a brief description of tests which confirm correct operation of each block and Appendix 1 at the end of this document contains lists of expected signatures analysis results at various points in the circuit when using the GE4P/9 NICAM TEST SIGNAL GENERATOR.

6.1. Power Supply

If the supply rails within the equipment are incorrect, the power supply can be loaded on the bench with about 7 A at +5 V and 0.8 A at ±18 V. Under these conditions, the 5 V line should be somewhat above 5 V to allow for voltage drops across the motherboard but should not exceed 5.25 V. The ±18 V rails should be between 17.5 V and 19 V each. If the ±18 V rails are low then check R57 and R58 have been removed from the power supply board. Faulty switch mode supplies should not be repaired but sent back to the manufacturer for repair.

6.2. Clock and Data Recovery

HDB3 DATA INPUTS

With the UN26/99 on an extender and all other cards in the rack, check the HDB3 data input stage level comparator as follows:

Apply a standard level (4.74 V) HDB3 signal to the input via a 75 Ω variable attenuator. Monitor the output of U9 pin 7 and check it goes high (> 3 V) when 10 dB of attenuation is put in the signal path. Then increase the input level and check the comparator output has gone low again by the time only 3 dB attenuation is present. There should be at least 1 dB of hysteresis in the switching level.

DATA SLICING

With the same setup as above, use a dual trace oscilloscope to monitor the DC level at pin 10 of U8 on one trace and the signal at pin 9 on the other. The DC level should be half the pulse amplitude. Check also for the other polarity pulses at pins 4 and 5 of U8. Pins 7 and 12 should pulse with data at TTL levels.

CLOCK RECOVERY

Again as above, look at the 2 MHz signal at TP1 (connect the earth of the oscilloscope probe directly to the earthy end of R47). A low amplitude sinewave should be present - check L4 is set to maximise the level. Check also the recovered clock at pin 12 of U9. This should be a TTL level 2 MHz square wave (1:1 ratio) with little data dependant jitter.

To check the locking range of the decoder needs a variable frequency oscillator and a frequency counter. Set the oscillator to produce a nominal 2048 kHz square wave at 4.7 V pk → pk and connect to the HDB3 input. (The /HDB3 ok output should fail indicating a rogue non HDB3 signal). Use the 2 channel oscilloscope, view U9 pin 12 on one trace (recovered clock) and U1 pin 10 on the other (de-jittered clock). Measure the input frequency range over which the traces stay in lock - it should be at least ±100 Hz but not greater than ±200 Hz referred to exactly 2D48 kHz. The crystal may be faulty if this range cannot be achieved by adjustment of VC1 (if fitted).

6.3. 2048 Locking

With no HDB3 connected to the crate, an 8 MHz clock should be at U29 pin 11 and U27, U30 pin 1. These should also be 2 MHz at U31 pin 10 and 4 MHz at U31 pin 9. At this stage, the top LED (D1) on the UN26/100 should be out and U32 pin 10 (on the UN26/99) should pulse with 3 ms mark and 1 ms space. U31 pin 8 should have a 2048 kHz signal with a 3:1 mark/space ratio. If all these are correct, check there is a stable negative going pulse train on U28 pin 9; if this is not present the sequencer is not working properly - see next section.

The /SDET line (U27 pin 3) should only have activity on it when an input is connected. /DDET (U27 pin 7) should be high. With an input present, check that a relock pulse from U32 pin 10 causes a later pulse on U27 pin 7; if not, then Frame Alignment Words are not being detected and the shift register circuitry should be checked. The MONITOR PROM (U32) or the PALs (U27, U3D) could also be faulty - check their Redcodes. Check also the 2048 lock LED driver - U8 pin 9 (UN26/100) is low to light the LED.

6.4. Sequencer

With the UN26/1D0 on an extender and no input signal to the crate, look at the outputs of the four counter chips U2, 3, 4 and 5. Depending on the 'weighting' of the bit, the outputs on pins 11 - 14 should be square waves at a sub multiple of the input clock frequency (pins 12, 13 of U2 will not have a 1:1 mark/space ratio). Pin 1 on U2 - 5 should pulse low every 3 ms. The /EOC signal fed back to the 2048 locking signal comes from PROM U43 and latch U44.

A reset pulse for the Z80A CPU is generated every 3 ms (active low) by U34 and U36. An unstable sequencer count can be caused by the CPU randomly changing the address lines of the Delay Fixing PROM (U10) - if necessary, remove the CPU to confirm this is the problem.

SIGNATURE ANALYSIS

Signature analysis can be used to test the sequencer action. The addressing sequence of the PROMs U11, 26, 34, 43 and 57 will always be the same after a CPU reset if the delay fixing does not affect the count. Use an HP5006A signature analyser set and connect as follows:

ANALYSER LINE	CONNECT TO	NOTE
GND	PL1 32c	-
CLK	PL2 19c	(-ve edge)
START	PL2 16c	(-ve edge)
STOP	PL2 16c	(-ve edge)
QUAL	-	Not Used

The open circuit signature should be OP7C. The signatures expected at the inputs and outputs of the sequencer PROMs and associated latches can be found in Appendix 1.

6.5. 676 Locking

Before checking this part of the circuitry, both the 2048 locking system and the sequencer must be working properly.

First, check the RECEIVE REGISTER PAL (U68 on UN26/100). Connect a GE4P/9 to the input of the crate, selecting the high frequency sweep as 'main' waveform and 'all 1's' as the 'secondary'. With all channels selected to 'main', pins 20 (CH1), 15 (CH2), 16 (CH3), 17 (CH4), 18 (CH5) and 19 (CH6) of U68 should show activity. Then, for each channel in turn, select the 'secondary' waveform and confirm that the corresponding output goes and stays logic high while the other outputs are unaffected.

Next check that the deserialisers (U69 - U74) are being correctly selected by connecting the signature analyser as above and verifying the signatures, listed in Appendix 1, at the inputs and outputs of U62. To confirm that the 676 frame alignment words are being detected correctly, select 'silence' on all six channels and check pins 6 and 7 of the deserialisers both have six positive going pulse per 3 ms.

These pins should become permanently high if 'all 1's' is selected on all channels. The CPU should be issuing relock pulses for any channels not in lock on pins 2 (X channel pair), 3 (Y channel pair and/or 4(Z channel pair). Other signals to check are:

A	The START pulse from the sequencer	(U67 pin 5 pulse low for every 3 ms)
B	Pin 1 of U69 - 74	(8 MHz clock)
C	Pin 1 of U47, 48, 60 and 61	(~ 340 kHz pulses)
D	Pin 7 of U68	(2048 kHz squarewave)
E	Pin 5 of U68	(2048 kHz 3:1 mark/space ratio)

For a channel pair that is not locked, Pin 2 of U47 (X channel pair), U48 (7 channel pair) and/or U61 (Z channel pair) should pulse when a FAW is detected.

Check also the Redcodes of the PALs (see Appendix 2).

6.6. System RAM

Check that on U15 and U30 pins 27 (/WE), 20 (/CE) and 22 (/OE) have activity. These signals are derived from the BUS CONTROL PAL (U37) which should have activity on pins 2 - 7 and an 8 MHz clock on pin 1. check the page switching operation by confirming that U35 (MISC PAL) pins 17 and 16 count in sequence 10, 01, 11 repeating every 9 ms. This cycle is clocked by a signal on pin 4 which pulses low every 3 ms. The address latches (U14, U29) and U37 can be checked by signature analysis. Connect the analyser as in 6.4. above, but also select QUAL active high going and connect it to U28 pin 1. The open circuit signature should be 77AH. The required signatures are listed in Appendix 1.

6.7. Gate Array Block

This block is tested using signature analysis. Connect the analyser as in section 6.4. above and feed the crate with an HDB3 signal from a GE4P/9 set to 333.33 Hz at +12.8 dBu. Confirm the system is locked (D1 - D4 on the UN26/100 are all on) and then check the signatures for U38 and U39 agree with those in Appendix 1.

6.8. CPU Block

LOCAL EPROM/RAM

The CPU performs a quick self test on power up. If an error in the EPROM or local RAM is found, the displays will read XF0 where X = A for the EPROM (U41 on UN26/99) or X = B for the RAM (U37 on UN26/99). Check these by substitution if necessary.

MUTE/RELOCK

With no bitstream present, the CPU should be producing positive going relock pulses at about 18 ms intervals and the audio should be muted. Check the correct signals appear on the output pins of U6 on the UN26/100 (pins 15, 6, 16 pulsing high and pins 5, 19 and 2 static low level). The strobe pulse for U6 comes from U44 pin 11 (low pulse every 3 ms).

SIGNALLING/DISPLAY STROBES

The signalling bit drivers and the alpha numeric displays are strobed by signals from U44 on the UN26/99 (some via inverters in U38). Check there are no short circuits on the inputs or outputs of U44 if invalid signalling display activity happens. The 16 front panel green LEDs on the UN26/99 and the executive fault outputs are strobed by signals from U45 on the UN26/99.

OTHER I/O STROBES

UN26/99

U35	:	pin 12	:strobe pulse, pulses when new 676 level signalling bits are output. (3 ms time period)
	:	pin 19	:clears the error counting PAL. (3 ms time period)
	:	pin 9	:blanks X display
	:	pin 15	:blanks Y display
	:	pin 6	:blanks Z display (these signals should become active when the channel has not received any errors for 2.5 min.)
U36	:	pin 11	:outputs LED values
U42	:	pin 11	:outputs LED values
U52	:	pins 1, 15	:inputs switch values
U54	:	pins 1, 15	:inputs switch values
U51	:	pins 1, 15	:inputs switch values
U53	:	pins 1, 15	:inputs switch values
U50	:	pins 1, 15	:inputs switch values
U48	:	pin 8	:inputs justification bits
U43	:	pins 1, 19	:inputs comparator fail inputs

UN26/100

U17	:	pin 2	:strobe for executive outputs
U18	:	pin 2	:strobe for executive outputs
U19	:	pin 2	:strobe for warning outputs

The time-out for the system is enabled if monostable U26 is not 'kicked' every 3 ms. Check that U44 pin 7 has negative going pulses and that these reach U26 pin 9. If the CPU has 'crashed', these pulses will not appear.

6.9. Executive Outputs

The green LEDs on the UN26/99 should mimic the state of the executive outputs according to the map in section 5.9. (LED on = fault output low ie, no fault). Set all the UN26/99 switches to '6' and confirm the 2048 and 676 lock indications are on when a bitstream is connected.

The error rate displays should read '7' or be blanked. (If the error counting circuitry is not working properly, the CPU will be issuing 676 relocks and mutes (the 676 lock LEDs will be flickering but too fast to see). Under these conditions, it will be impossible to test the channel fail outputs, though the BER outputs can still be checked).

Vary the settings of the lowest three switches on the UN26/99 and check the corresponding BER outputs and UN26/99 LEDs switch correctly (eg, switch set to 0, 1, 2 or 3 should not fail if display reads '4'). Use the GE4P/9 error rate control to vary the point at which the switches activate the outputs to check all the switch bits are active.

If there is a problem here, check the CPU is correctly reading the switches by looking at the contents of the 4 LSBs of the data bus when U51 or U52 are gating data onto it (pin 15 low). The CPU also must re-trigger monostable U26 b regularly or the CLR line on the BER/FAULT output drives (U17, 18 and 19 on the UN26/100) will be activated.

The fault outputs can be checked as above if the error counting circuitry (section 6.10.), the 676 locking circuitry (section 6.5.) and the audio outputs/comparators (sections 6.14.and 6.15.) are all working. In this case the CPU reads the switch data via U50, U53, or U54 as appropriate. To check the fault reporting tests the audio comparators outputs correctly, switch off and remove one of the audio cards. When the crate is re-powered, all six channels should report failure.

6.10. Error Counting System

Check the ERRCOUNT PAL is being correctly accessed by signature analysis. Set up the analyser as per section 6.4. and confirm the signatures given in Appendix 1 are correct. If the alpha numeric displays indicate invalid data but the signatures are correct, the CPU is not reading the ERRCOUNT PAL correctly - see CPU and the System Ram sections (6.8. and 6.6. respectively).

6.11. Signalling Bits

The quickest way to check the signalling bits are working correctly is to connect a RDS DATA SPLITTER (CD4S/18) and Network bitstream to the crate and check for readable RDS messages. If this method is not possible, check with an oscilloscope that the CPU is loading the signalling bit drivers (U55, U46 and U47) - strobe pulses (active high) should appear on pin 2. If the alpha numeric displays on the UN26/99 are working correctly, there is unlikely to be any fault on the CPU data bus - U55, U46, or U47 may be at fault. It is also possible (though the background self test would find a fault) that the system RAM has an error.

6.12. DAC Block

DAC INTERFACE PALS

Check the DAC INTERFACE PALS (U41, 50 on UN26/100) are being correctly accessed by signature analysis. Set up the analyser as per section 6.4. and confirm the signatures given in Appendix 1 are correct. Any errors here should be traced back to the sequencer or a faulty PAL.

SERIALISERS

Confirm the serialiser are working correctly by connecting the GE4P/9 set to 'going' waveform for all channels to the HDB3 input. With an oscilloscope, examine the waveform on pin 6 of the 74LS674s (U25, 32, 42, 55 and 75). It should have a 16 µs time period and the first half should clearly show the bit activity of the 'going' signal. Remove the bitstream and check the activity disappears on all the 74LS674s.

COSITED/INTERLEAVED SELECTIONS

It will not be possible to do this test if the audio outputs are not present. With the GE4P/9 plugged in and set to produce 10 kHz at +5 dBu, monitor two relevant audio outputs (ie, CH1, 2 or CH3, 4 etc). With the links (LK1, LK2 on UN26/100) set to the cosited position (upper), the two audio outputs should be in phase.

Moving the links to the lower position should delay the right channel audio output by 15 µs. A fault here should be traced to the delay circuitry, U79 - 83 (main) or U87 - 90 and U22 (reserve).

INTERPOLATORS

The following signals should be present on the Interpolator ICs (U76, 77, 78, 85 and 86):

Pin 1	(WSAB)	32 kHz square wave
Pin 11	(XIN)	8 MHz square wave
Pin 2	(CLAB)	2 MHz square wave
Pin 18	(WSBD)	128 kHz square wave
Pin 9	(X575)	4 MHz square wave
Pin 16	(CLBD)	2 Mhz square wave
Pin 22, 23	(/ATSB, /MUSB)	Active Low mute signal

A suspect Interpolator should be checked by substitution.

6.13. Muting Systems

The CPU block issues the mute commands to the MUTE PAL (U717) on the CO9/13 and also to the Interpolators as above. The MUTE PAL will also turn off the audio outputs if 2048 lock is lost. If the CO9/13 appears to be muting incorrectly check the signals from the CPU and 2048 LOCKING sections are reaching the MUTE PAL correctly as follows:

Pin 1	8192 kHz	8 MHz squarewave clock
Pin 23	MUTE X	Active low mute signal from CPU block
Pin 14	MUTE Y	Active low mute signal from CPU block
Pin 11	MUTE Z	Active low mute signal from CPU block
Pin 2	/2048 lock	Active low lock indicator
Pin 13	/RESET	CPU RESET line from the sequencer

(Note the /RESET signal is only used to count 3 ms intervals - not to reset the PAL). If these signals are correct and the mute outputs (pins 6, 7, and 8) are low, the PAL is faulty.

To check the analogue muting circuitry, proceed as follows:

De-power the crate and unplug the CO9/13s. Check the source - drain resistance of each FET pair (QXO2, QXO3 where X is the channel number) with an Ohm-meter - it should be less than 50 Ohms.

Unplug the MUTE PAL (U717) from the suspect card and put the card (on an extender) back into the rack. Check that with the GE4P/9 connected (set to 1 kHz tone at +8 dBu) that audio appears at the outputs - if not, see the next section. Apply a TTL level square wave at about 100 Hz to pin 6, 7 or 8 of U717's socket and check the resulting waveform at pins 1 and 7 of U714 (if using pin 6 U717), U715 (pin 7 U717) or U716 (pin 8 U717) as appropriate. This should be a 10 V pk → pk square wave with a rise or fall time to the 63% point of about 1 ms.

Check that the audio output envelope is a similar waveform with an attenuation of at least 40 dB in the 'on' periods. With digital silence selected on the GE4P/9 and the TTL square wave removed, use a digital voltmeter to check the DC offset at TPXO3 (X = channel number). This should be less than ±3 mV - if more, the DC auto zero integrator (UXO1 b, QXO4, QXO1 and associated components) or the DAC chip itself is suspect.

6.14. Analogue Outputs

DC OFFSET INTEGRATOR

This is checked by the method at the end of section 6.13. above.

J17 DE-EMPHASIS AND LOW PASS FILTER

The J17 de-emphasis network is best checked by injecting a variable frequency sinewave into TPX01 (X = channel number) via a J17 emphasis network. (30 kΩ resistor, 1200 pF and 10 nF capacitors all in parallel - connect network between source and TPX01). With the crate locked to digital silence from a GE4P/9 (and the offset within limits as per the section above), measure the frequency response at TPX03 into high impedance - this should be within ±0.1 dB from 100 Hz to 5 kHz and between -0.15 and -0.3 dB at 10 kHz. Any error is probably due to wrong value components.

LINE DRIVERS

These are fairly simple buffers which have line driving capability. RX12 sets the DC line-to-line voltage which should be less than 1 mV. The distortion can be checked by injecting a 1 kHz low distortion sinewave into TPX01 via a J17 emphasis network as above. At +8 dBm across the output the distortion should be less than 0.01% (80 dB separation).

BALUNS AND PRECISION RECTIFIERS

These checks can be performed on the cards in the crate or separately on the bench. For in crate tests, the audio gain will need to have been set correctly - see later. For on bench tests, apply power and +8 dBu tone to the card as follows:

+5 V	PL1 29c
0 V	PL1 30c
+18 V	PL1 2c
-18 V	PL1 4c
0 V	PL1 5c
Tone	PL2 22a/c (CH1), 24a/c (CH2) or 26a/c (CH3)

(For on bench tests, couple the centre pins of LKX63 and LKX64 to the 'B' pins of LKX42 and LKX41 respectively).

Check the level at the output of the bal-uns (UX61 or UX62) is 8 ±0.3 dBu. Check also with a DVM the mean DC potential at TPX63 and TPX64 - it should be 1.75 V ±100 mV.

GAIN

To set the gain, connect the GE4P/9 NICAM TEST SIGNAL GENERATOR to the crate and set its output to '416.66 Hz at +8 dB'. (The PROMs in the generator should be for the revised line-up level - maximum coding range = +14.8 dBu at 2 kHz).

Set each of the gain-set potentiometers RX07 on the left hand C09/13 so that, when terminated in 600 ohms, the main audio outputs are at +8 dBm. The gains on the right hand card can be set similarly, but a better method is first to check the alignment of the audio comparators (see next section) and then to set the gains on the right hand C09/13 so that the corresponding comparator outputs are 0 ±200 mV.

FREQUENCY RESPONSE

Use the GE4P/9 to check that the audio outputs when loaded with 600 Ω have a frequency response which is accurate to ±0.1 dB (up to 10 kHz) and is within the range +0.3, -0.5 dB above 10 kHz.

If the response is outside these limits, check the J17 de-emphasis network as above.

COMPANDING AND QUANTISATION NOISE

Unless audible distortion on the 'gong' tone from the GE4P/9 is present, this check is not needed. The test requires a coder and a 14 kHz source and notch filter. (The standard method of using a 40 Hz tone and a high pass filter cannot exercise all the data bits at the low frequency due to J17 emphasis). A circuit for a simple notch filter is given in DSK27215A1 and setting up instructions for this filter are given in Appendix 3.

Using a 6 channel NICAM coder (2 channel equipment may not have a good enough performance), feed a 14 kHz tone at +8 dBu into the coder and measure the weighted noise level at the output of the decoder.

The theoretical weighted noise levels are:

Input tone level (dBu)	Noise out (dB4w)
+8	38
+1	44
-5	50
-11	56
-17	62

The measured figures should be within 3 dB of these figures.

A suspect DAC can be checked by substitution.

6.15. Audio Comparators

Set LKX61 to position 'B' and leave LKX61 open circuit. With no audio present, adjust RX73 for zero DC at TPX65. Using the GE4P/9 by injecting a tone into TPX01, (as described in the J17 DE-EMPHASIS subsection above), produce +10 - +13 dBu at 1 - 2 kHz from all outputs.

Use RX81 to set the voltage at TPX65 to zero again. Drop the tone level by 20 dB or so and check TPX65 is still at zero volts. Minor sequential adjustments to RX73 and RX81 can be made until TPX65 remains at 0 ±200 mV for all signal levels (including no signal).

Alternatively, with a DC coupled oscilloscope connected to TPX65, adjust RX73 for no DC and RX81 for minimum response to audio content.

To check the other half of the circuit, temporarily couple the centre pins of LKX63 and LKX64 to both the 'A' and 'B' pins of LKX41 and LKX42 respectively (this connects the two balanced inputs in parallel). With LKX61 in the 'A' position, check that TPX65 remains at 0 ±300 mV for all signal levels (including no signal). The green LED DX78 should be on. Set the tone level to +4 - +6 dBu at any frequency and check that DX78 goes out when LKX61 is made. (LKX61 made simulates a 1 dB imbalance in comparator input levels). Remember to remove LKX61 again.

6.16. AES/EBU Outputs

These are best checked by using an MN8/12 Digital Audio Monitor (DAM). The DAM should lock to the signal and produce the same audio as is present at the analogue outputs. If the digital outputs do not work (and the analogue ones do), then the EBU PALs and output drivers are suspect (U11 - 25, U56 on UN26/99).

7. APPENDICES

APPENDIX 1

This is a List of expected signatures at various points in the circuits. The section number given refers to the associated part of the MAINTAINANCE section in the handbook.

6.4. Sequencer

The signatures expected are:

INPUT PINS	U11	U26	U34	U43	U57
2	U4P0	U4P0	U4P0	U4P0	U4P0
23	U03F	U03F	U03F	U03F	U03F
21	4671	4671	4671	4671	4671
24	A9H9	A9H9	A9H9	A9H9	A9H9
25	H68A	H68A	H68A	H68A	H68A
3	38A2	38A2	38A2	38A2	38A2
4	53CA	53CA	53CA	53CA	53CA
5	0920	0920	0920	0920	0920
6	42C6	42C6	42C6	42C6	42C6
7	U4P8	U4P8	U4P8	U4P8	U4P8
8	CA69	CA69	CA69	CA69	CA69
9	53FP	53FP	53FP	53FP	53FP
10	U452	U452	U452	U452	U452
OUTPUT PINS					
19	P9F7	38PF	4U78	PF80	9957
18	A0P9	9097	41U2	F04P	832A
17	U785	48P6	690F	8P18	8C17
16	3PPA	4PC3	3P33	U625	AHFU
15	6820	8725	80C3	AF4A	9P2A
13	89C4	601U	485F	86CF	836C
12	H41A	HA32	873F	C791	9H67
11	11H0	0U36	H9U7	7HAU	F04P

OUTPUT PINS	U58	U44	U36
2	45PH	U640	APUA
19	F8H3	6961	A9CU
5	4FFH	F70F	3HF0
16	5UA1	U254	965U
6	4653	5U63	491U
15	48U3	4A18	2H68
9	47U5	528P	F39P
12	6961	C791	XXXX

XXXX = UNSTABLE

6.5. 676 Locking

Expected Signatures for U62:

OUTPUT PINS	signature
14	A001
13	4A18
12	AF4A
11	5U63
10	C791
9	528P
INPUT PINS	
1	47U5
2	48U3
3	4653

6.6. System RAM

The following signatures should be present:

device	pin no.	signature
U14	3	3268
U14	18	3P63
U14	4	568U
U14	17	8UCH
U14	7	P49C
U14	14	5A49
U14	8	P174
U14	13	3793
U29	3	1255
U29	18	P69F
U29	4	5080
U29	17	XXXX
U29	7	XXXX
U29	14	294A
U29	8	002U
U29	13	H5FC
U37	4	U7C7
U37	6	H259
U37	12	UA6U
U37	15	4P01
U37	16	39AF
U37	17	0HH8
U37	18	8HF2
U37	19	7A75

6.7. Gate Array

The signatures taken should be:

U38	PIN	SIGNATURE
	23	A9CU
	24	APUA
	25	3HF0
	27	AH35
	28	F10H
	29	1530
U39		
	9	AH35
	10	F10H
	11	1530

6.10. Error Counting System

Expected Signatures at U40:

pin	signature
2	AH35
3	F10H
4	1530
6	3HF0
9	A244
10	2HP3
11	2H68
13, 14	243P

6.12. DAC Interface PALs

Signatures expected on U41, U50

pin	signature
2	AH35
3	F10H
6	491U
7	4FFH
12	4764
13	C379
18	868H
19	3P5H

APPENDIX 2

A List of programmable devices and their REDCODES

UN26/99

IC No.	Type	Name	Redcode (*16 bit checksum)	P/F No.
U14	EP600	EBU_1_PAL	B234 *	F1041A
U15	EP600	EBU_2_PAL	8071 *	F1042A
U16	EP600	EBU_1_PAL	B234 *	F1041A
U17	EP600	EBU_2_PAL	8071 *	F1042A
U18	EP600	EBU_1_PAL	B234 *	F1041A
U19	EP600	EBU_2_PAL	8071 *	F1042A
U20	EP600	EBU_1_PAL	B234 *	F1041A
U21	EP600	EBU_2_PAL	8071 *	F1042A
U22	EP600	EBU_1_PAL	B234 *	F1041A
U23	EP600	EBU_2_PAL	8071 *	F1042A
U24	EP600	EBU_2_PAL	8071 *	F1042A
U25	EP600	EBU_1_PAL	B234 *	F1041A
U27	PAL 20X10	MONITOR_PAL	6ED0 *	F1048A
U30	PAL 20X10	DETECTOR_PAL	6934 *	F1047A
U32	2716	MONITOR_PAL	A469	P5313A
U41	27128	CPU_PROM	A984	P5326A

UN26/100

IC No.	Type	Name	Redcode (*16 bit checksum)	P/F No.
U10	TBP18S030	DELAY_FIX_PROM	2CC7	P5314A
U11	2764	SEQ1_PROM	5DFF	P5319A
U26	2764	SEQ2_PROM	9D0C	P5318A
U34	2764	SEQ3_PROM	6C5E	P5317A
U35	PAL 16R4	MISC_PAL	4A7A *	F1049A
U37	PAL 16R6	BUS_CONTROL_PAL	5BDC *	F1051A
U39	PAL 20X8	PARITY_DISP_PAL	74D6 *	F1057A
U40	PAL 20X8	ERR_COUNT_PAL	83C8 *	F1058A
U41	PAL 16R4	DAC_INTERFACE_PAL	5546 *	F1059A
U43	2764	SEQ4 PROM	B288	P5316A
U47	PAL 20X10	COUNTER_PAL	9D8A *	F1054A
U48	PAL 20X10	COUNTER_PAL	9D8A *	F1054A
U50	PAL 16R4	DAC_INTERFACE_PAL	5546 *	F1059A
U57	2764	SEQ5 PROM	9E17	P5315A
U60	PAL 20X10	COUNTER_PAL	9D8A *	F1054A
U61	PAL 20X10	COUNTER_PAL	9D8A *	F1054A
U67	PAL 20X10	SUB_CONTROLLER_PAL	8488 *	F1050A
U68	PAL 20X8	RECEIVE_REG_PAL	5468 *	F1052A
U69	PAL 20X10	DE-SERIALISER_PAL	6F19 *	F1053A
U70	PAL 20X10	DE-SERIALISER_PAL	6F19 *	F1053A
U71	PAL 20X10	DE-SERIALISER_PAL	6F19 *	F1053A
U72	PAL 20X10	DE-SERIALISER_PAL	6F19 *	F1053A
U73	PAL 20X10	DE-SERIALISER-PAL	6F19 *	F1053A
U74	PAL 20X10	DE-SERIALISER_PAL	6F19 *	F1053A

C09/13

IC No.	Type	Name	Redcode (*16 bit checksum)	P/F No.
U717	EP600	MUTE_PAL	4F9B *	F1060A

APPENDIX 3

NOTCH FILTER

(CIRCUIT - DSK27215A1)

Setting Up

The tone source should have a good short-term stability, eg. ±1 Hz at a nominal 14 kHz.

Absolute frequency is not critical, and may have a tolerance of ±100 Hz.

A spectrum analyser is useful for measuring the 14 kHz level at the output of the notch filter.

1 Set C1 and R1 mid-range.

2 Adjust L1 adjuster and R2 for best null of 14 kHz.

3 Adjust C1 and R1 for best null at 14 kHz, which should be at least -65 dB relative to the incoming tone level.

C1 and R1 may require re-adjustment at the different tone levels to achieve this. In general, if the companding noise specification is met, there is no need to re-trim C1 and R1. If, however, the noise level appears higher than it should be, then re-check the notch tuning.

TO POWER SUPPLY

+16V
+12V
0V
+5V
0V

678 locked(0:2)
COMPARATOR(0:5)
MUTESIGS(0:2)
CLOCKS(0:3)
CONTROL(0:7)
DATA(0:7)
ADDRESS(0:15)

BD1 UN26/99
BD2 UN26/100
BD3 C09/13
BD4 C09/13

PL1 PL2 SKG SKH SKI SKJ SKM SKN SKO SKP

CHASSIS
/204B lock
+16V
-16V
0V (A)
COMP FAIL 1
COMP FAIL 2
COMP FAIL 3
COMP FAIL 4
COMP FAIL 5
COMP FAIL 6
/CDBS
678 locked 12
678 locked 34
678 locked 56
CH1 STR1
CH1 STR2
CH1 STR0
CH2 STR3
CH2 STR2
CH2 STR1
CH2 STR0
CH3 STR3
CH3 STR2
CH3 STR1
CH3 STR0
CH4 STR3
CH4 STR2
CH4 STR1
CH4 STR0
CH5 STR3
CH5 STR2
CH5 STR1
CH5 STR0
CH6 STR3
CH6 STR2
CH6 STR1
CH6 STR0
A(15)..A(0)
D(7)..D(0)
/BD
/WR
/IORQ
/MREQ
/REFH
/INT
/WAIT
/RESET
/ROFT
/EOC
BLOCK CLOCK
FRAMES CLOCK
CLOCKS GROUND
2048kHz
4096kHz
8192kHz
FAILS CLOCK
CLEAR ERRORS
RETRIG MONO O/P
GRAB JUST BITS
DOBM128
DOBM348
DOBM568
DOBM128
DOBM348
DOBM568
/STGEN
2048 STR
1/128-
1/128+
3/48-
3/48+
5/68-
5/68+
CH1FAIL A
CH2FAIL A
CH3FAIL A
CH4FAIL A
CH5FAIL A
CH6FAIL A
/STGEN
N/U
XSYS128
D880128
CLBD128
USB0128
XSYS348
D880348
CLBD348
USB0348
XSYS568
D880568
CLBD568
USB0568
XSYS128
D880128
CLBD128
USB0128
XSYS348
D880348
CLBD348
USB0348
XSYS568
D880568
CLBD568
USB0568
DOBM128
DOBM348
DOBM568
DOBM128
DOBM348
DOBM568
CH1FAIL A
CH1BER
CH1FAIL B
CH2BER
CH2FAIL A
CH2BER
CH3FAIL A
CH3BER
CH3FAIL B
CH4BER
CH4FAIL A
CH4BER
CH4FAIL B
CH5BER
CH5FAIL A
CH5BER
CH5FAIL B
CH6BER
CH6FAIL A
CH6BER
/MUTE X
/MUTE Y
/MUTE Z
BERCOMB
COMPCOMB
/MUTE Z
N/U
CH1 A+
CH1 A-
CH1 ASCN
CH2 A+
CH2 A-
CH2 ASCN
CH3 A+
CH3 A-
CH3 ASCN
CH4 A+
CH4 A-
CH4 ASCN
CH5 A+
CH5 A-
CH5 ASCN
CH6 A+
CH6 A-
CH6 ASCN
6192kHz
/RESET
CH1 CMP+
CH1 CMP-
CH1 ASCN
CH2 CMP+
CH2 CMP-
CH2 ASCN
CH3 CMP+
CH3 CMP-
CH3 ASCN
CH4 CMP+
CH4 CMP-
CH4 ASCN
CH5 CMP+
CH5 CMP-
CH5 ASCN
CH6 CMP+
CH6 CMP-
CH6 ASCN
CH1 MONSCN
CH1 MON+
CH1 MON-
CH2 MONSCN
CH2 MON+
CH2 MON-
CH3 MONSCN
CH3 MON+
CH3 MON-
CH4 MONSCN
CH4 MON+
CH4 MON-
CH5 MONSCN
CH5 MON+
CH5 MON-
CH6 MONSCN
CH6 MON+
CH6 MON-

CH1 MAIN TO OPERATOR ON BOARD 4
CH5 MAIN TO OPERATOR ON BOARD 4
CH6 MAIN TO OPERATOR ON BOARD 4
CH2 REF TO OPERATOR FROM BOARD 4
CH5 REF TO OPERATOR FROM BOARD 4
CH1 REF TO OPERATOR ON BOARD 3
CH2 REF TO OPERATOR ON BOARD 3
CH5 REF TO OPERATOR ON BOARD 3
CH6 MAIN TO OPERATOR FROM BOARD 3

AUDIO OUT(0:35)
COMP TO(0:17)

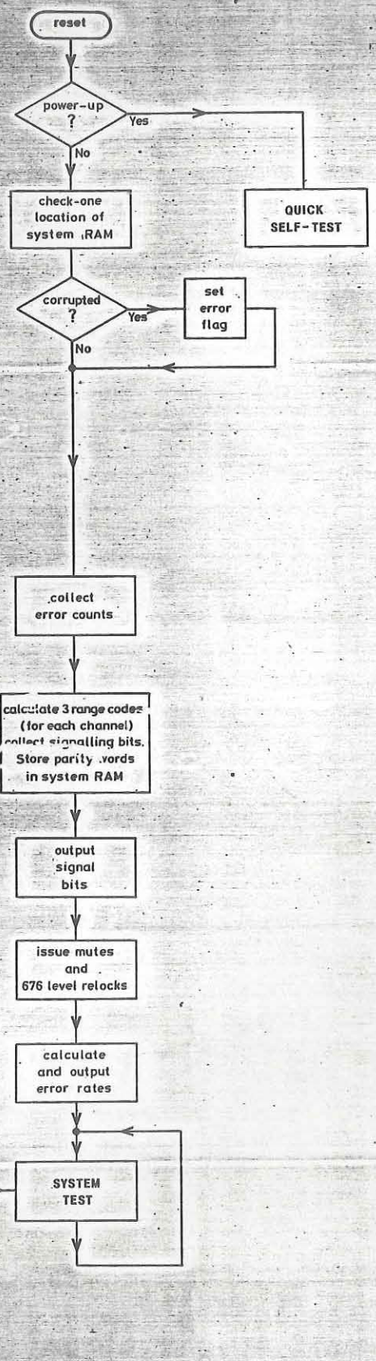
56 WAY VARICON SKD

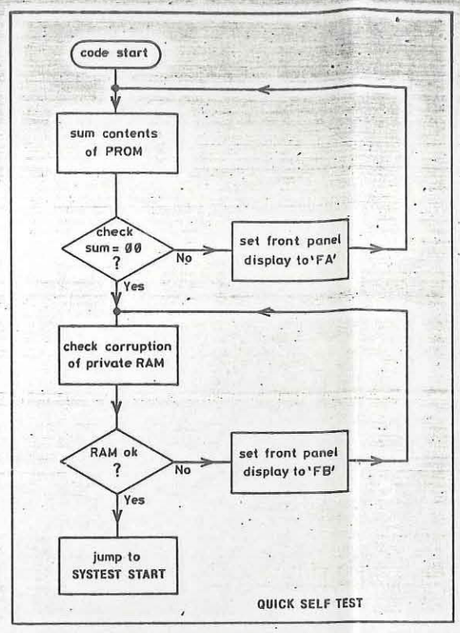
SKA 37WAY D TYPE
SKB 25WAY D TYPE
SKC
SKE
PLA PLB PLC PLD PLE PLF
STGBITS(0:26)
CH12 STR
CH34 STR
CH56 STR
/204B lock
clock earth
DIG 0V
DIG +5V
204B RST
DSIGS(0:23)
PHILIPS DIG(0:5)
EBOUT(0:11)
CHANBER(0:5)
CHANFAIL A(0:5)
MISCFAIL(0:3)
CHANFAIL B(0:5)
CHASSIS

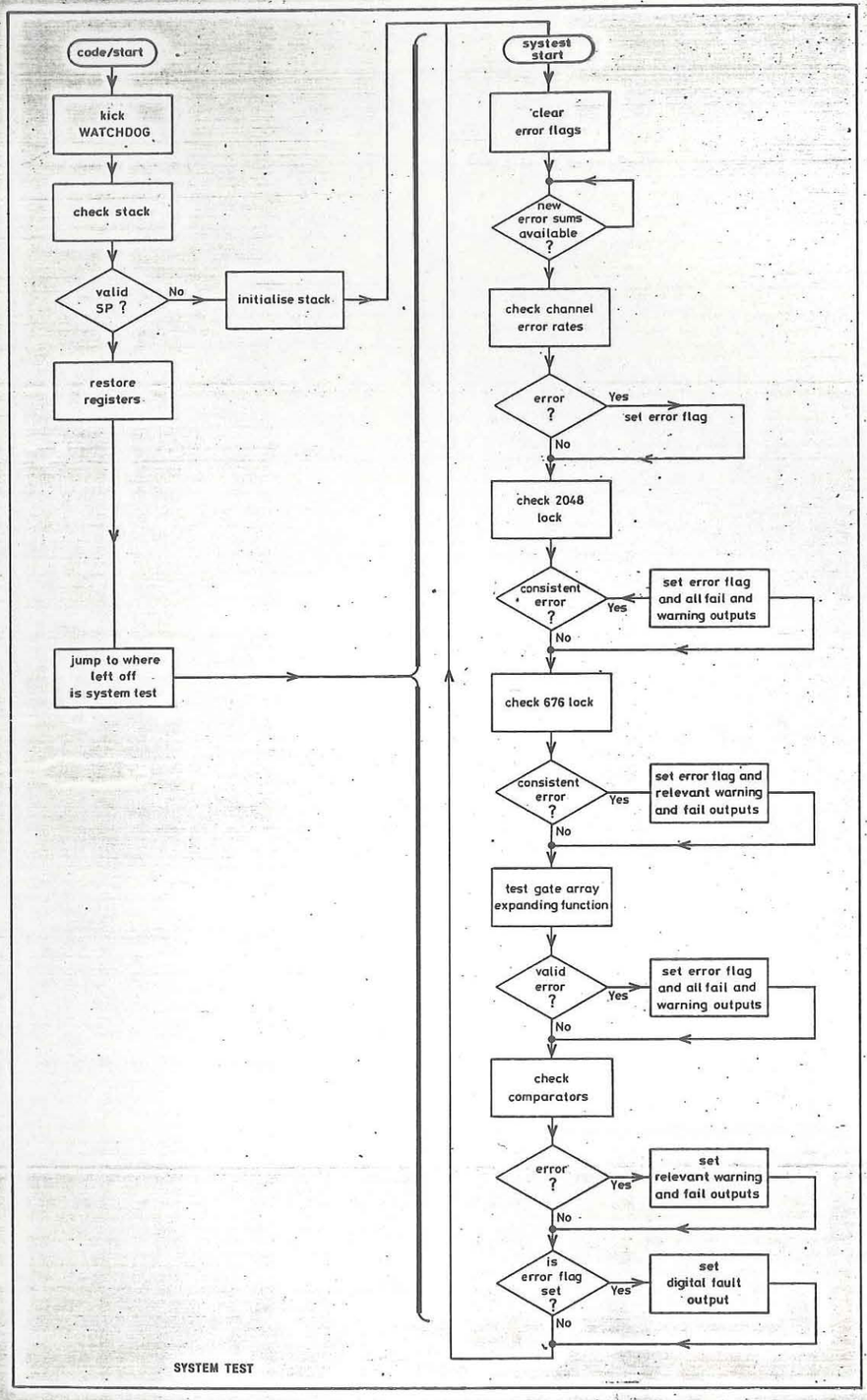
ORIGINAL FRAME SIZE 570mm x 821mm
ISS CHANGE 1/2/85

CD3L/58 MK II NICAM BLOCK DIAGRAM

DRN CCC
TCD
DF







D63567A1

SCALE:— 0

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE 574mm x 821mm

CHANGE A 15.1.88

NICAM II DECODER SOFTWARE

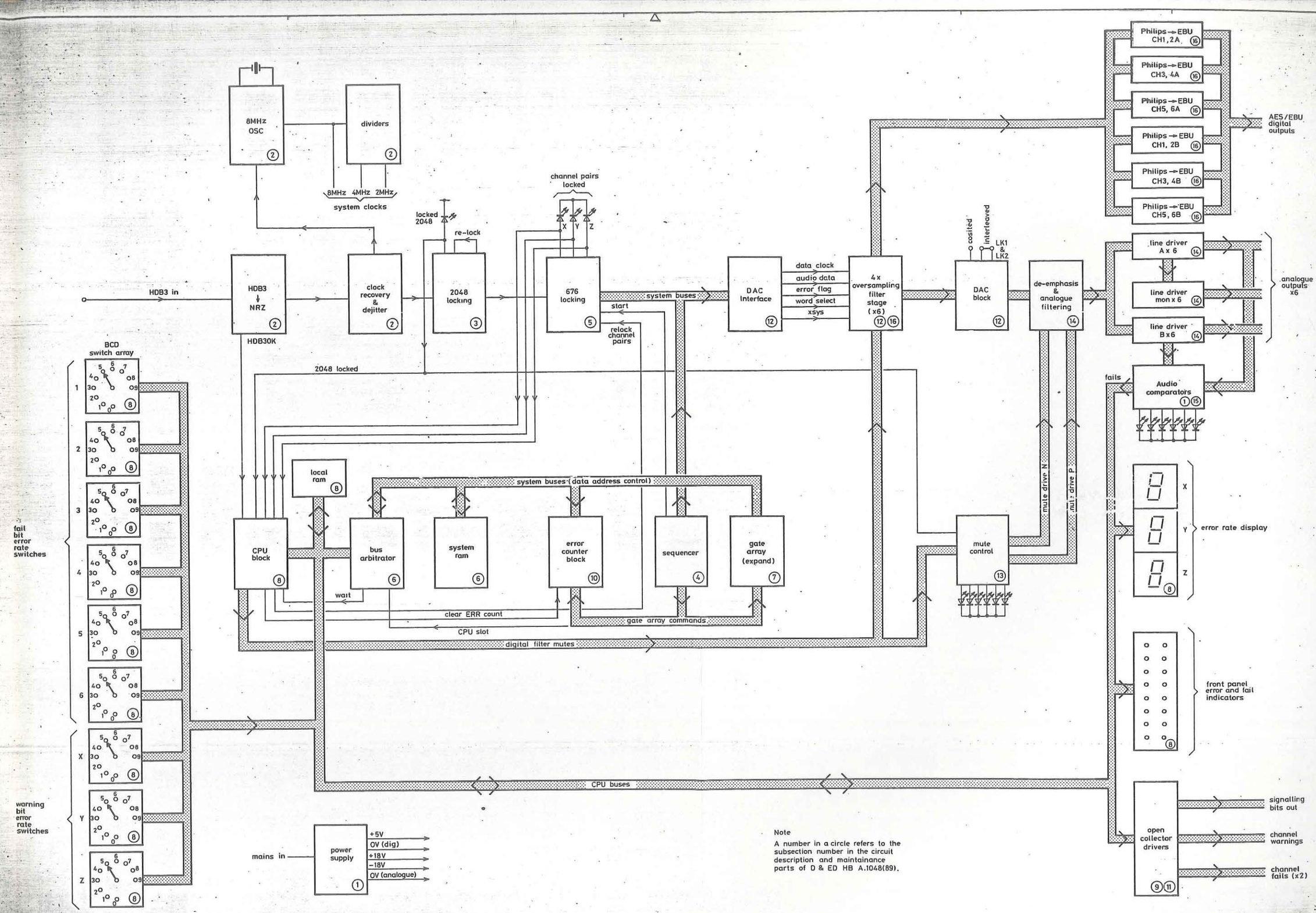
CD3L/58 SYSTEMS DIAGRAM

All dimensions in millimetres unless otherwise stated. Normal tolerances: no decimal places ± 1mm unless; one decimal place ± 0.5 mm otherwise; two decimal places ± 0.1 mm stated

DRN. P.P. TCD. CKD. APPD. C.C.C.

DESIGN & EQUIPMENT DEPARTMENT

D63567A1



Note

A number in a circle refers to the subsection number in the circuit description and maintainance parts of D & ED HB A.1048(89).

SCALE:– 0

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE 574mm x 821mm

CHANGE		
DR	DATE	
1	13/4/89	
2	4/5/89	
3	3/6/89	
4	6/7/89	
5	7/8/89	

NICAM MK II SIX CHANNEL DECODER

CD3L/58 BLOCK DIAGRAM

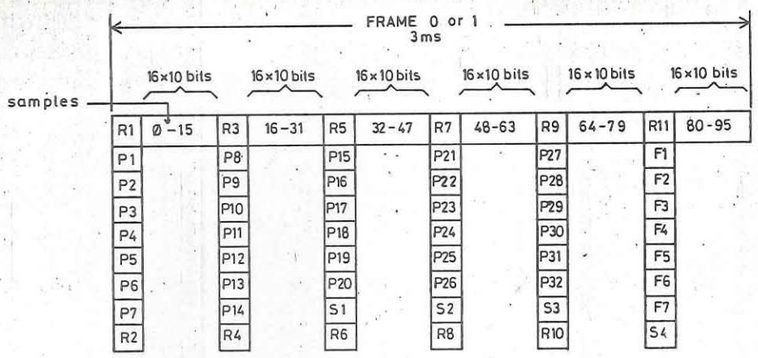
All dimensions in millimetres unless otherwise stated: Normal tolerances: no decimal place ± 1 mm unless, one decimal place ± 0.3 mm otherwise, two decimal places ± 0.1 mm stated

DRN.	J DB
TCD.	
CKD.	
APPD.	

DESIGN & EQUIPMENT DEPARTMENT

D63598A1

DSK 21831A2



NOTES:-

Single channel framing is contained in a multiframe - Frame 0 and 1.
Framing bits are different for each frame although their positions in the bitstream sequence are identical.

The single channel bit-rate is 338kbit/s. A two channel format (channels A and B) is comprised of two single channel formats with the bits interleaved, so that channel B bits follow corresponding channel A bits. The two channel bit-rate is 676kbit/s

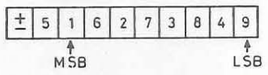
A six channel format includes additional framing and signalling bits (see Fig 2).

On channel 'B' F1 in frame 0 is inverted with respect to F1 on channel 'A'.

For compactness, the housekeeping bits are shown vertically
The occur in groups sequentially with groups of samples. In this diagram time is increasing from left to right, and from top to bottom.

The sample bits are shown as groups of 16×10 bits, with the bits in each sample arranged as shown below.

The sign bit(±) occurs first, and LSB(9) occurs last.



	Frame 0	Frame 1
F1	0(A), 1(B)	0
F2	0	0
F3	1	0
F4	1	1
F5	0	1
F6	0	0
F7	0	1

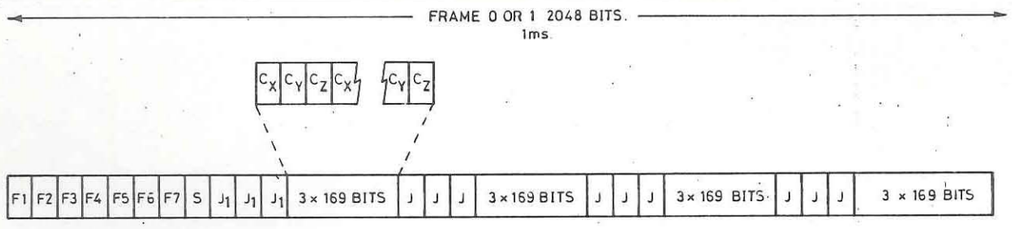
Parity Bit	Protects Samples	Parity Bit	Protects Samples
1	3, 35, 66	17	14, 47, 78
2	8, 39, 71	18	18, 52, 83
3	12, 44, 75	19	23, 58, 89
4	17, 48, 79	20	27, 63, 95
5	21, 53, 84	21	15, 50, 80
6	26, 57, 88	22	22, 56, 85
7	31, 62, 92	23	29, 61, 91
8	19, 51, 82	24	0, 34, 65
9	24, 55, 86	25	5, 40, 70
10	28, 60, 90	26	10, 45, 74
11	32, 64, 94	27	7, 33, 68
12	2, 37, 69	28	13, 38, 76
13	6, 42, 73	29	16, 43, 81
14	11, 46, 77	30	20, 49, 87
15	4, 36, 67	31	25, 54, 93
16	9, 41, 72	32	1, 30, 59

This order has been chosen:

(a) to spread each group of 3 protected samples as widely as possible

(b) To spread the 18 or 21 samples protected by each housekeeping word, with the maximum number of other samples between them.

Fig. 1 NICAM 3. SINGLE CHANNEL FORMAT.



NOTES.

Six channel multiplex framing is contained in a multiframe - Frame 0 and 1. Framing bits are different for each frame although their positions in the bitstream sequence are identical. Time is increasing from left to right

F = Framing Bit.
S = Signal Bit
J = Spare bit

$C_{X(Y,Z)}$ = Channel Bit From Coder Pair X (Y, Z).

Alternately $C_{X(Y,Z)}$ is a channel A and a channel B bit. Channel B bits follow corresponding channel A bits

$3 \times J_1$ = Frame lock bits
= 111 Every third frame
= 000 Otherwise
(Lock occurs on '111' frames)

Bit Rates:

3 Coder Pairs	= 3×676	=	2028 kbit/s
Framing		=	7 kbit/s
Spare	= 3×4	=	12 kbit/s
Signalling		=	1 kbit/s
			2048 kbit/s

	Frame 0	Frame 1
F1	1	0
F2	0	0
F3	1	0
F4	1	1
F5	0	1
F6	0	0
F7	0	1

Fig. 2 NICAM 3. SIX CHANNEL MULTIPLEX FORMAT.

DSK 21831A2 ISS. 6

BBC

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THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE 400mm x 574mm

SCALE - 0

ISS	CHANGE
1	26·3·80 RB.
2	7·8·81 S.T.
3	17·8·81 S.T.
4	24·6·82 S.T.
5	24·2·83 S.T.
6	6·6·83 DGE. (Similar to DSK2408A2)
8	8-1-88

All dimensions in millimetres unless otherwise stated
Normal tolerances
no decimal place = ± 1 mm unless
one decimal place = ± 0·3 mm otherwise
two decimal places = ± 0·1 mm stated

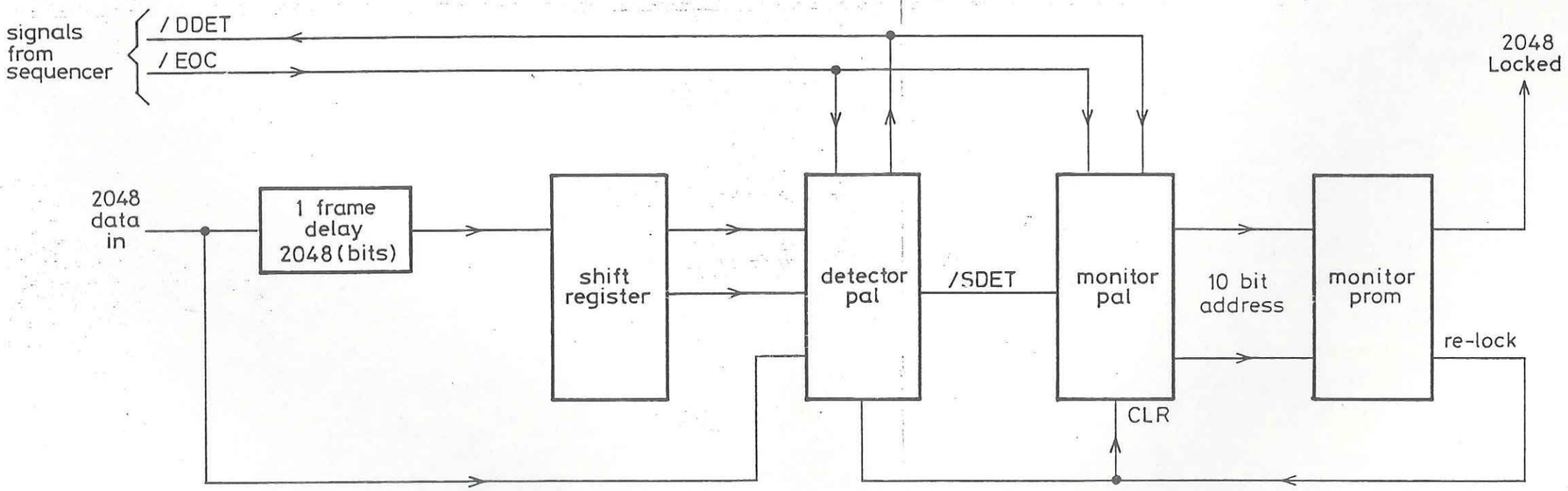
DRN	
TCD	RB
CKD	
APPD	

NICAM 3 BITSTREAM DIAGRAMS

DESIGNS DEPT.

DSK 21831A2

S&H LTD 15591



SCALE: – 0

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE
277mm x 400mm

DS/A3/1

ISS	CHANGE
1	14/4/89
2	5/5/89

2048 LOCKING

CD3L/58
BLOCK DIAGRAM

All dimensions in millimetres unless otherwise stated: Normal tolerances:
no decimal place – ± 1 mm unless
one decimal place – ± 0.3 mm otherwise
two decimal places – ± 0.1 mm stated

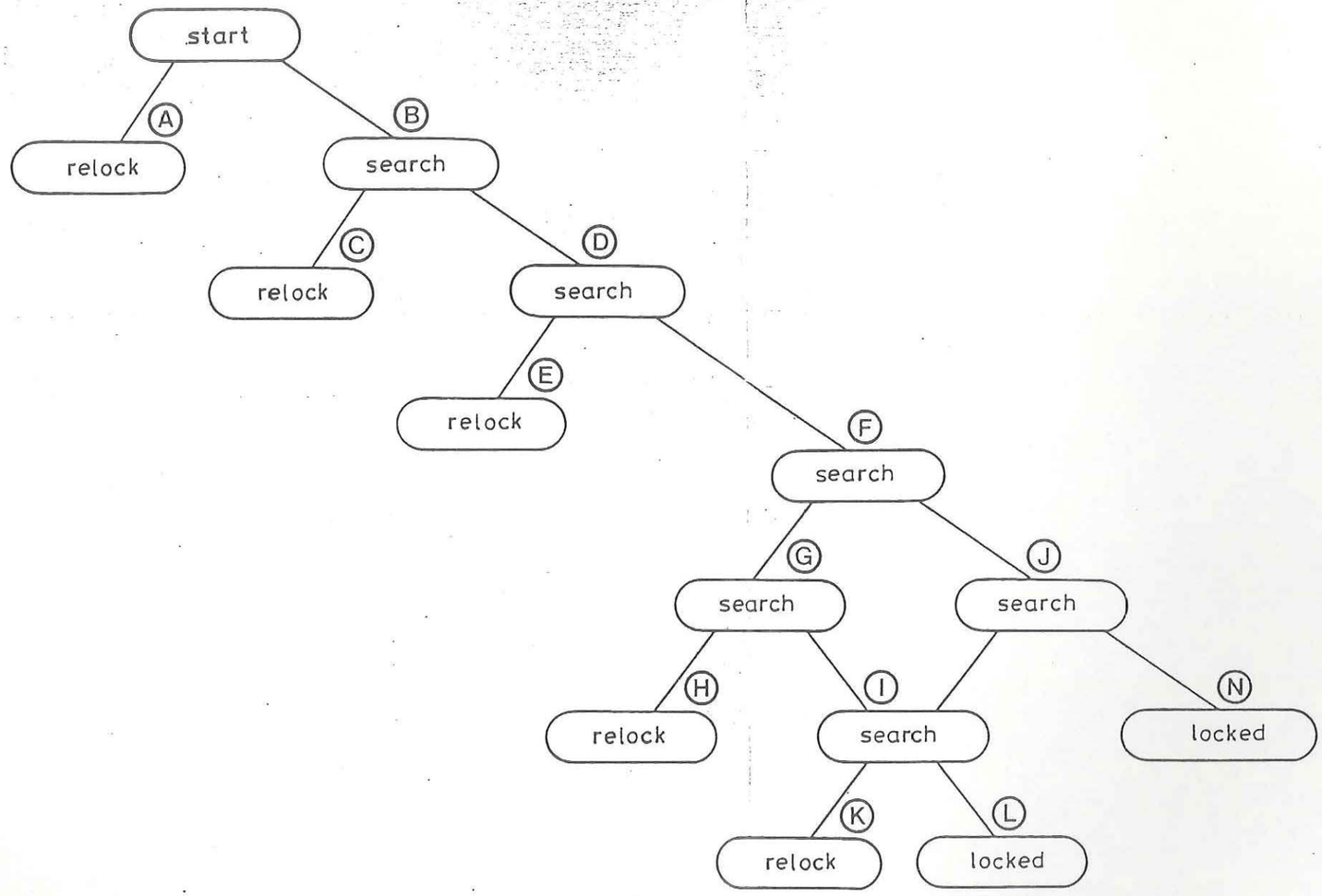
DRN.	J DB
TCD.	
CKD.	
APPD.	R.B.D

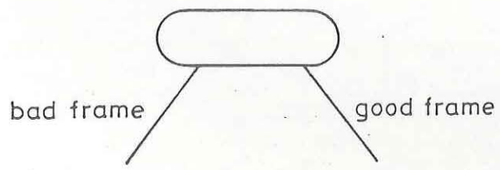
DESIGN & EQUIPMENT DEPARTMENT

D63602A3

R294

D63590A3





SCALE:– 0

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE
277mm x 400mm

ISS	CHANGE	
1	4.5.89	

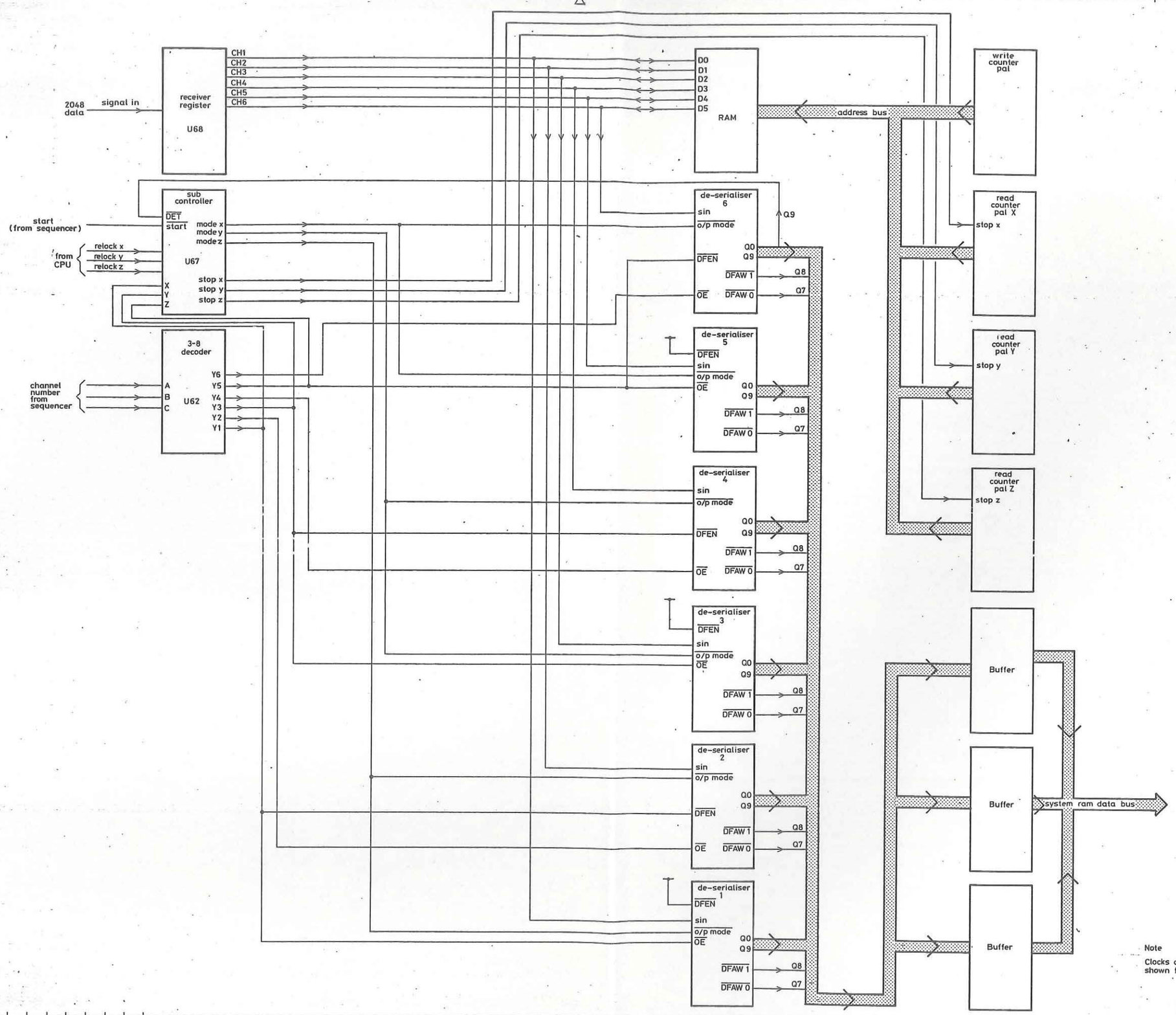
2048 LOCKING SEQUENCE

CD3L/58
SYSTEMS DIAGRAM

All dimensions in millimetres unless otherwise stated: Normal tolerances:
no decimal place – ± 1 mm unless
one decimal place – ± 0.3 mm otherwise
two decimal places – ± 0.1 mm stated

DRN.	P.P.	DESIGN & EQUIPMENT DEPARTMENT
TCD.		
CKD.		D63590A3
APPD.	C.C.C.	

R294



SCALE:– 0

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE 574mm x 821mm

CHANGE		
1	20/4/89	
2	6/7/89	

676 LOCKING SYSTEM

CD3L/58
BLOCK DIAGRAM

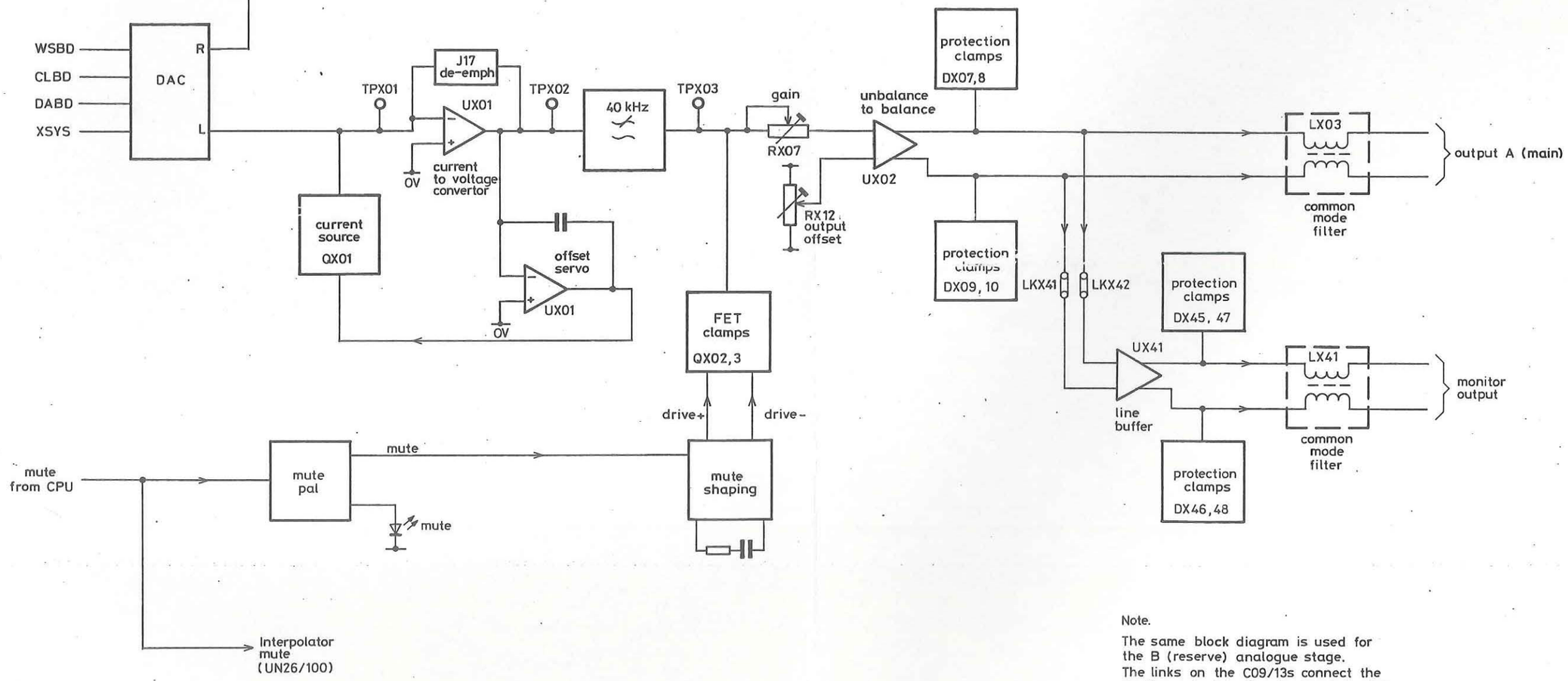
All dimensions in millimetres unless otherwise stated. Normal tolerances:
no decimal place – ±1 mm unless
one decimal place – ±0.3 mm otherwise
two decimal places – ±0.1 mm stated

DRN.	JDB
TCD.	
CKD.	
APPD.	

DESIGN & EQUIPMENT DEPARTMENT

D63599A1

Right channel as left channel



Note.

The same block diagram is used for the B (reserve) analogue stage.
The links on the C09/13s connect the monitor output buffers to the A (main) outputs - there are no monitor outputs on the B signals.

SCALE:- 0

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE
400mm x 574mm

ISS	CHANGE	
1	13/4/89	
2	6/7/89	

R293

ANALOGUE STAGE
BREAK DOWN
DECODER

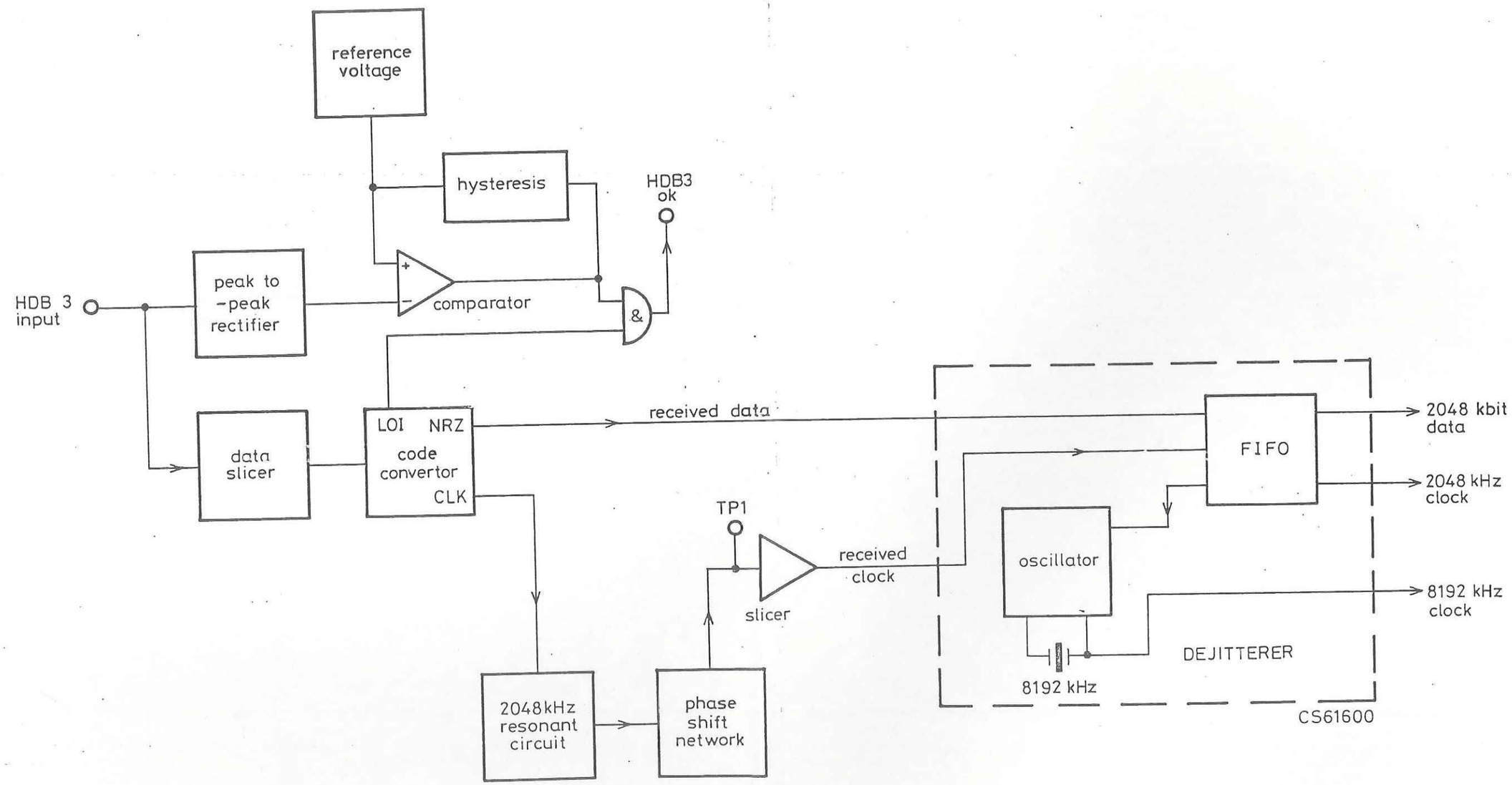
CD3L/58
BLOCK DIAGRAM

All dimensions in millimetres unless otherwise stated: Normal tolerances:
no decimal place - ±1 mm unless
one decimal place - ±0.3 mm otherwise
two decimal places - ±0.1 mm stated

DRN.	J DB
TCD.	
CKD.	
APPD	R.B.D

DESIGN & EQUIPMENT DEPARTMENT

D63600A2



SCALE: – 0

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE
277mm x 400mm

ISS	CHANGE
1	13/4/89
2	5/5/89
3	4/7/89

DS/A3/1

CLOCK RECOVERY AND HDB-NRZ CONVERSION

CD3L/58
BLOCK DIAGRAM

All dimensions in millimetres unless otherwise stated: Normal tolerances:
no decimal place – ± 1 mm unless
one decimal place – ± 0.3 mm otherwise
two decimal places – ± 0.1 mm stated

DRN.	J D B
TCD.	
CKD.	
APPD.	

DESIGN & EQUIPMENT DEPARTMENT

D63603A3

D62191A4

ISS.	CHANGE
1	1/2/89
2	12/5/89

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
			DRAWING LIST		
			BLOCK DIAGRAM D62190A1		
			PARTS LIST D62191A4		
			ASSEMBLY AND WIRING (2 SHTS) D62192A1		
			DETAIL 1 - FRONT PANEL D62193A2		
			DETAIL 2 - LACING BAR D62194A4		
			PBd MASTERS D62196A3s		
			PBd DRILLING D62197A2		
			WIRING SCHEDULE D62198A4		
			FRONT PANEL LEGEND D62199A1		
			FURTHER INFORMATION REQUIRED FOR MANUFACTURE		
			WIRING SPEC ED 122.		
			UNIT WIRING (VIDEO) EA10139		
			UNIT WIRING (PBd) EA10140		
			UNIT ASSEMBLY EA10484		
			UNIT SPEC ED/CD3L/58		
			SPEC ED 3002 INSULATING TUBING & SLEEVING		
			REAR PANEL DETAIL (REF, ONLY IF REQD). DSK 27306A1		
1	1	*	PRINTED BOARD TO SPEC ED/PB/CD3L/58/PTH		0624721
			MANUFACTURED TO :-		D62196A3s, D62197A2
2					
3	1		FRONT PANEL		
			MADE BY CONTRACTOR TO :-		D62193A2 - DET 1
			SCREEN PRINTED BY CONTRACTOR TO :-		D62199A1
4					
5	1		REAR PANEL LACING BAR		
			MADE BY CONTRACTOR TO :-		D62194A4 - DET 2
6	1	*	POLARISING SCREEN 100mm x 125mm HNCP 37 STD 0.76		- 0628684
7	1	*	FUSE HOLDER, MAINS, PANEL MOUNTING		S22229 - 0614124
			(1) FS1		
8	1	*	FUSE, QUICK ACTING, 5 x 20, 3.15A		S22444 - 0369439
9	1	*	FUSE INSULATING COVER, RED		S22332 - 0483808

BBC /PLA4

CD3L/58
6 CHANNEL NICAM II DECODER
PARTS LIST

DRN.	DSI
TPD	
CKD	
APPD.	CCC

D & ED
D62191A4
SHT 1 OF 6

ISS.	CHANGE
1	1/2/89
2	11/5/89

ITEM No.	No. OFF		DESCRIPTION	CCT REF	BBC REF. OR DRG. No.
10	1	9H	UN26/99		
11	1	9H	UN26/100		
12	1	9H	C09/13 - CUSTOMISED TO DSK 27219A4		
13	1	9H	C09/13 - CUSTOMISED TO DSK 27195A4		
14	1	9H	PS4/51		
15	1	*	EUROCONNECTOR BLANKING KIT (PIN 23)		-0632267
16	1	*	CODING BAR, PLASTIC		-0628144
17	12	*	PBD RUNNERS, PLASTIC		-0625457
18	6	*	PBd MOUNTING BLADE, VERTICAL, RS533-689		
19	6	*	CRIMP CONNECTOR, INSULATED, RS533-005		
			PLUGS & SOCKETS		
20	8	*	SOCKET, FIXED, 64 POLE, PBd MOUNTING (8) SKG, SKH, SKI, SKJ, SKK, SKL, SKM, SKN		S27890 - 0610089
21	1	*	SOCKET, FIXED, 11 POLE, PBd MOUNTING (1) SKS		S27892 - 0383320
22	1	*	SOCKET, FIXED, 56 POLE VARICON (1) SKD		S27953 - 0206311
23	1	*	SOCKET, FIXED, 37 POLE D TYPE (1) SKA		S27819 - 0454627
24	1	*	SOCKET, FIXED, 25 POLE, D TYPE (1) SKB		S27819 - 0351294
25	1	*	SOCKET FIXED, 15 POLE D TYPE (1) SKF		S27819 - 0351286
26	2	*	SOCKET FIXED, BNC, OPEN CABLE ENTRY (2) SKC, SKE		S27502 - 0236524
27	1	*	SOCKET FIXED, 11 POLE, PBd MNTG, MAINS (1) SKT		-0383320
28	1	*	SPADE CONNECTOR, CRIMP, FEMALE		-0629192
29					

BBC

S/PLA4

CD3L/58

PARTS LIST

DRN.	DSI
TPD.	
CKD.	
APPD	CCP

D & ED

D62191A4

ISS.	CHANGE
1	1/2/89

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
30	6	*	PLUG, FIXED, 3POLE XLR		S24933 - 0091829
			(6) PLA, PLB, PLC, PLD, PLE, PLF		
31	1	*	SOCKET, FIXED, 3 POLE MAINS, XLR		S27700 - 0023036
			(1) PLG		
32	11	*	SOCKET TERMINAL, STRAIGHT ENTRY, FREE		S27893 - 0379539
33	11	*	INSULATOR, SOCKET TERMINAL		S27893 - 0379555
34					
35	56	*	SOLDER CONTACT, VARICON		S25124 - 0210276
36	1	*	INSULATING COVER, RED, XLR		S25131 - 04C3844
37	25	*+	TY-RAP FOR 1.5 - 44.0 DIA		S19100 - 0250641
38					
			CABLE		
40	1m	*	PSF 1/7		S17355 - 038219X
41	A/R	*+	PUF 1/3M BLACK		S14708 - 0201540
42	A/R	*+	PUF 1/3M PINK		S14708 - 0375860
43	A/R	*+	PUF 1/3M BROWN		S14708 - 0201508
44	A/R	*+	PUF 1/3M RED		S14708 - 0201532
45	A/R	*+	PUF 1/3M ORANGE		S14708 - 0201488
46	A/R	*+	PUF 1/3M YELLOW		S14708 - 0201559
47	A/R	*+	PUF 1/3M GREEN		S14708 - 0201496
48	A/R	*+	PUF 1/3M BLUE		S14708 - 020147X
49	A/R	*+	PUF 1/3M VIOLET		S14708 - 0201567
50	A/R	*+	PUF 1/3M RED/WHITE		S14708 - 0406180
51	A/R	*+	PUF 1/3M SLATE		S14708 - 0201516

BBC

S/PLA-1

CD3L/58

PARTS LIST

DRN.	DSI
TPD	
CKD.	
APPD	CCC

D & ED

D62191A4

SHT 3 OF 6

D6219A4

ISS.	CHANGE
1	1/2/89

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
52	A/R	*+	PUF1/3M ORANGE/WHITE		S14708 - 0406093
53	A/R	*+	PUF1/3M SLATE/WHITE		S14708 - 0406121
54	A/R	*+	PUF1/3M BROWN/WHITE		S14708 - 0406113
55	A/R	*+	PUF1/3M GREEN/WHITE		S14708 - 0406105
56					
57					
58	A/R	*+	PSN2/4M BLUE/WHITE		S12403 - 0216919
59	A/R	*+	PSN2/4M ORANGE/WHITE		S12403 - 0216927
60	A/R	*+	PSN2/4M GREEN/WHITE		S12403 - 0216935
61	A/R	*+	PSN2/4M BROWN/WHITE		S12403 - 0216943
62	A/R	*+	PSN2/4M SLATE/WHITE		S12403 - 0216951
63	A/R	*+	PSN2/4M BROWN/RED		S12403 - 0216994
64	A/R	*+	PSN2/4M GREEN/RED		S12403 - 0216986
65					
66	A/R	*+	PUN1/1M BLACK		S14626 - 0216568
67					
68	A/R	*+	PUF1/5M BLUE		S14739 - 020253X
69	A/R	*+	PUF1/5M ORANGE		S14739 - 0202505
70	A/R	*+	PUF1/5M GREEN		S14739 - 0202521
71	A/R	*+	PUF1/5M BROWN		S14739 - 0202485
72	A/R	*+	PUF1/5M SLATE		S14739 - 0216769
73	A/R	*+	PUF1/5M WHITE		S14739 - 0216777
74	A/R	*+	PUF1/5M GREEN/YELLOW		S14739 - 0216785
75					
76					
77					

BBC

JS/PLA4

CD3L/58

PARTS LIST

DRN.	DSI
TPD.	
CKD.	
APPD	C.C.A.

D & ED

D62191A4

SHT 4 OF 6

D62191A4

ISS.	CHANGE	
1	1/2/89	
2	11/5/89	

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
78	A/R	*+	SLEEVING, SYMEL, 1·5 mm BORE, WHITE		0254100
79	50	*	BINDING, WHITE, 25·4 x 3·0 BORE		S19768-0052059
80	A/R	*+	PUF1/6M ORANGE		S14708 - 0201488
81	A/R	*+	PUF1/6M GREEN		S14708 - 0201496
82	A/R	*+	PUF1/6M BROWN		S14708 - 0201508
83	A/R	*+	PUF1/6M SLATE		S14708 - 0201516
84	A/R	*+	PUF1/6M WHITE		S14708 - 0201524
85					
86					
87	0·5m	*+	MAINS CABLE, 6AMP, 3CORE		- 0602874
			FIXINGS		
100	4	*	M3x16 LG. VARICON MOUNTING SCREWS		S25135 - 0384151
101	3	*	JACK POST ASSEMBLIES, D TYPE		S25150 - 0377384
102					
103	2	*	THUMBSCREW KIT (PAIR OFF)		- 0626769
104	4		M2·5 x 8 LG, INST HD, M.S., CHR. PL.		FOR FIXING ITEMS 14
105	10		M2·5 x 6 LG, M.S. Zn PL, PAN HD		1
106	25		M2·5 x 10 LG, Ms, Zn PL, PAN HD		16, 21, 20
107	1		M2·5 x 12 LG, Ms. Zn PL, PAN HD		21, 38
108	15		M3 x 8 LG, CH PL, Ms INST HD		30, 31, 123
109	2		M3 x 8 LG, Ms, Zn PL, PAN HD		5
110	1		M3 x 10, M.S, Zn PL, PAN HD		126
112	24		NUT, FULL, HEX, M2·5		

BBC S/PLA4

CD3L/58
PARTS LIST

DRN.	DSI
TPD.	
CKD.	
APPD	CCC

D&ED
D62191A4
SHT 5 OF 7

ISS.	CHANGE
1	1/2/89
2	11/5/89

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
113	20		NUT, FULL, HEX, M3		
114	2	*	NUT, LOCKING, M3, BINX BX213		0629393
115	36		WASHER, PLAIN, M2·5		
116	16		WASHER, PLAIN, M3		
117					
118					
119	1	*	P CLIP, 6·4 Ø, FIXED.		S19095-0052513
120	1	*+	MAINS WARNING LABEL 25x80, SELF ADHESIVE		S54977-0256984
121	6		SOLDER TAG. SINGLE ENDED, M3		
122	1	*	EARTH TAG, DOUBLE ENDED		-0629176
123					
124					
125					
126	1	*	SPACER, M3 x 5mm TAPPED		-0211352
140	1		CARTON CARDBOARD TO SPEC ED/CD3L/58		

Notes

* Denotes items supplied to the contractor on embodiment loan

*+ Denotes items supplied to the contractor on embodiment loan, requiring special costing or supply action by B.B.C.

θ* Denotes components supplied and fitted by B.B.C. on test.

θ+ Denotes coded plug in units supplied and fitted by B.B.C. on test.

Ø Denotes items supplied and fitted by B.B.C. on installation.

BBC

PLA4

CD3L/58 PARTS LIST

DRN.	DSI
TPD.	
CKD.	
APPD	C.C.

D&ED

D62191A4

SHT.	ISS.	DETAILS OF CHANGE
2	2	ITEM 15 ADDED. ITEM 27 WAS 5 POLE.
5	2	ITEM 105 WAS 8 OFF.
6	2	ITEM 115 WAS 34 OFF. ITEM 123, SINGLE ENDED SOLDER TAG, DELETED. DMS 1446(A) DSI 11/5/89

SHT.	ISS.	DETAILS OF CHANGE

ORIGINAL FRAME SIZE 190mm x 277mm

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED

BBC

VH 418/A4

DESIGNS DEPARTMENT

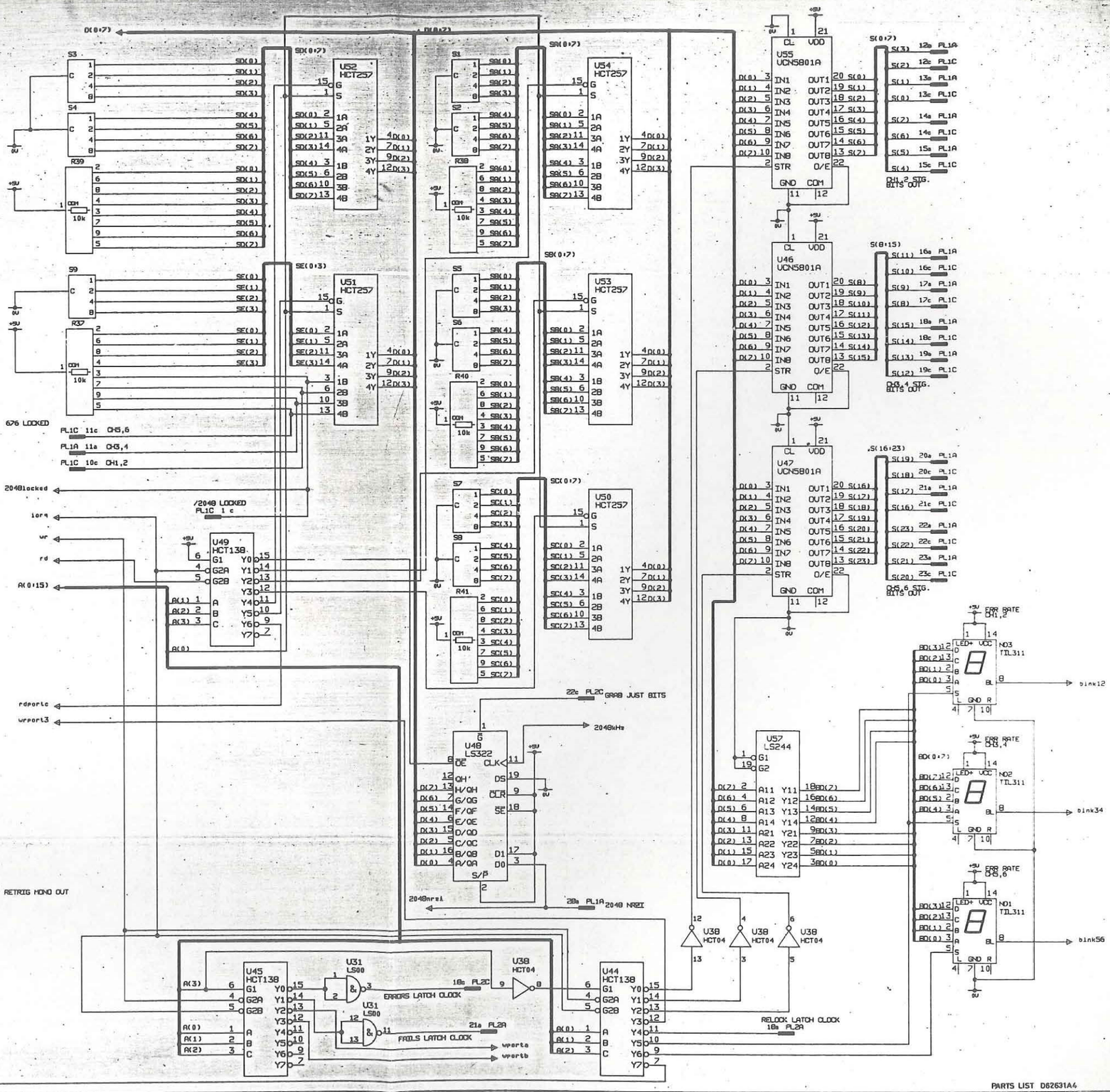
CODE:- CD3L/58 11/5/89

PARTS LIST CHANGE RECORD, ISSUE:- 2

D62191 A4

SHEET 7

D62630A1



PARTS LIST D62631A4

SCALE: - 0

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE 574mm x 821mm

CHANGE 18/6/98

NICAM MKII DIGITAL BOARD 1 . UN26/99 CIRCUIT

All dimensions in millimetres unless otherwise stated Normal tolerances.
no decimal place - ±1 mm unless
one decimal place - ±0.3 mm otherwise
two decimal places - ±0.1 mm stated

DRN.	DT	DESIGN & EQUIPMENT DEPARTMENT
TCD.		
CKD.		D62630A1
APPD.	CCC	

SHEET 1 OF 5 SHEETS

D62630A1

D15 LT63HRG
D14 LT63HRG
D13 LT63HRG
D12 LT63HRG
D11 LT63HRG
D10 LT63HRG
D9 LT63HRG
D8 LT63HRG

ADDRESS BUS CONNECTIONS

U40 Z80A

U39 HCT32
U38 HCT04
U28 HCT32
U37 6116
PGM U41 27128

DATA BUS CONNECTIONS

U36 HCT377
U42 HCT377
U43 LS244
U35 HCT377

4x470 R27
4x470 R26
4x470 R29
4x470 R28

R34 470
R30 2k7
R31 1k
R32 1k
R33 1k
Q8 2N3904
Q7 2N3904
Q6 2N3904
Q9 2N3904
R35 15 w/w

U38 HCT04
D25 1N4148
D24 1N4148
U39 HCT32
U31 LS00
C22-61 10n

PROBE EARTH

SIG BITS STROBES
+5V COMMON
CLEAR ERRPAL
REPEAT=40

SCALE: - 0

PARTS LIST D62631A4

THIRD ANGLE PROJECTION
ORIGINAL FRAME SIZE 574mm x 821mm
CHANGE 18/6/89

NICAM MKII DIGITAL
UN26/99
CIRCUIT

All dimensions in millimetres unless otherwise stated. Normal tolerances: no decimal place ± 1 mm unless, one decimal place ± 0.3 mm otherwise, two decimal places ± 0.1 mm stated.

DRN. DI
TCD.
CKD.
APPD.

DESIGN & EQUIPMENT DEPARTMENT
D62630A1
SHEET 2 OF 5 SHEETS

D62630A1

U22 EP600 — 4096kHz — PL3A 23a DQBH12A — EBU_1 PAL — EBU_2 PAL — EBUOUT12A
U23 EP600
U20 EP600 — PL2C 23c DQBH34A — EBU_1 PAL — EBU_2 PAL — EBUOUT34A
U21 EP600
U16 EP600 — PL2A 24a DQBH56A — EBU_1 PAL — EBU_2 PAL — EBUOUT56A
U17 EP600
U25 EP600 — PL2C 24c DQBH12B — EBU_1 PAL — EBU_2 PAL — EBUOUT12B
U24 EP600
U18 EP600 — PL2A 25a DQBH34B — EBU_1 PAL — EBU_2 PAL — EBUOUT34B
U19 EP600
U14 EP600 — PL2C 25c DQBH56B — EBU_1 PAL — EBU_2 PAL — EBUOUT56B
U15 EP600

U12 9638 — U56 9638

U13 9638 — L18 220n — L10 L/12235 — 27a PL2A — EBU OUTPUT 9 CHANNELS 1&2 — 27c PL2C
U13 9638 — C17 220n — L9 L/12235 — 28a PL2A — EBU OUTPUT A CHANNELS 3&4 — 28c PL2C
U12 9638 — C16 220n — L8 L/12235 — 29a PL2A — EBU OUTPUT A CHANNELS 5&6 — 29c PL2C
U56 9638 — C15 220n — L7 L/12235 — 30a PL2A — EBU OUTPUT B CHANNELS 1&2 — 30c PL2C
U11 9638 — C14 220n — L6 L/12235 — 31a PL2A — EBU OUTPUT B CHANNELS 3&4 — 31c PL2C
U11 9638 — C13 220n — L5 L/12235 — 32a PL2A — EBU OUTPUT B CHANNELS 5&6 — 32c PL2C

U29 HCT327 — L(0:6) — 8192kHz — 2048data — 2048nrzi
U28 HCT32 — L(1) — L(5)
U30 20X10 — SDET — CLR
U27 20X10
U32 2716 — RELOCK
U28 HCT32 — PL2C 17c /EDC — PL2A 17a /DDET — 2048blocked
U31 LS00 — 2048kHz — 4096kHz — PL1A 10a /CDR3 — /CDR1
U34 AM2833 — U33 AM2833 — -12V

R24 33k — C19 1n — U26 HCT123 R/C C CLR — R25 3k3 — Q5 BFY50 — 2048strobe — 26c PL2C — PL2A 26a /STROBE

PL1A 1a — IMPLICIT VCC +5V — PL1C 29c — PL1A 29a — PL1C 30c — PL1A 30a — PL1C 31c — PL1A 31a — PL1C 32c — PL1A 32a — IMPLICIT END

SCALE: - 0

PARTS LIST D62631A4

THIRD ANGLE PROJECTION | ORIGINAL FRAME SIZE 574mm x 821mm | CHANGE 18/6/98 SS 2

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NICAM MKII DIGITAL — UN26/99 CIRCUIT

All dimensions in millimetres unless otherwise stated. Normal tolerances: no decimal place ± 1.0 mm unless; one decimal place ± 0.5 mm otherwise; two decimal places ± 0.05 mm stated

DRN | DT | DESIGN & EQUIPMENT DEPARTMENT
TCD
CKD
APPD

D62630A1

SHEET 3 OF 5 SHEETS

D62630A1

/HDB3ok FL1A 27a

+12V

R21 68k

R7 10k

R14 2k2

Q2 BFY50

U9 LM319

R12 100k

R20 10k

R15 1k8

R8 2k

D6 1N4148

R16 68k

-12V

L4 15uH

C11 390p

R18 10k

C10 1n

R51 3k

R22 22k

D64 20p

Q4 2N3904

Q3 2N3904

R13 2k7

C8 1n

R17 2k

R47 1k8

C9 1n

R19 24k

+9V

R23 560

U9 LM319

recd_clock

TP1

RECOVERED CLOCK

R5 10k

U6 HC4049

D3 10V

D1 BAV10

D4 10V

D2 BAV10

PL1A 9 a

HDB3 INPUT

PL1C 9 c

R2 75

C3 1n

D5 1N4148

D7 1N4148

C7 1n

C4 100n

R4 3k3

C5 1n

R6 33k

R9 3k3

C6 1n

R10 33k

Q1 CA3096

SUBS 16

R11 33k

+12V

U8 LM319

R45 560

R46 560

-12V

R3 33k

U8 LM319

U7 78L12

+1BV ANALOGUE

PL1C 2 c

PL1A 2 a

L2 22u

R44 100

C2 100n

C12 100n

+12V

U2 79L12

-1BV ANALOGUE

PL1C 3 c

PL1A 3 a

L1 22u

R43 100

C1 100n

C20 100n

-12V

PL1C 4 c

PL1A 4 a

PL1C 5 c

PL1A 5 a

0V ANALOGUE

R42 100

U10 MJ1440

IN

ENCK

B IN

A IN

DECK

RESAIS

LTE

OUT

ERR

O2

O1

CK

AIS

LOI

recd_data

0V

SCALE:- 0

PARTS LIST D62631A4

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE 574mm x 821mm

CHANGE 16/6/00

NICAM MKII DIGITÁL

UN26/99

CIRCUIT

All dimensions in millimetres unless otherwise stated Normal tolerances

no decimal place ± 1 mm unless

one dec. pl. place ± 0.1 mm otherwise

two decimal places ± 0.1 mm stated

DRN. DJ

TCD.

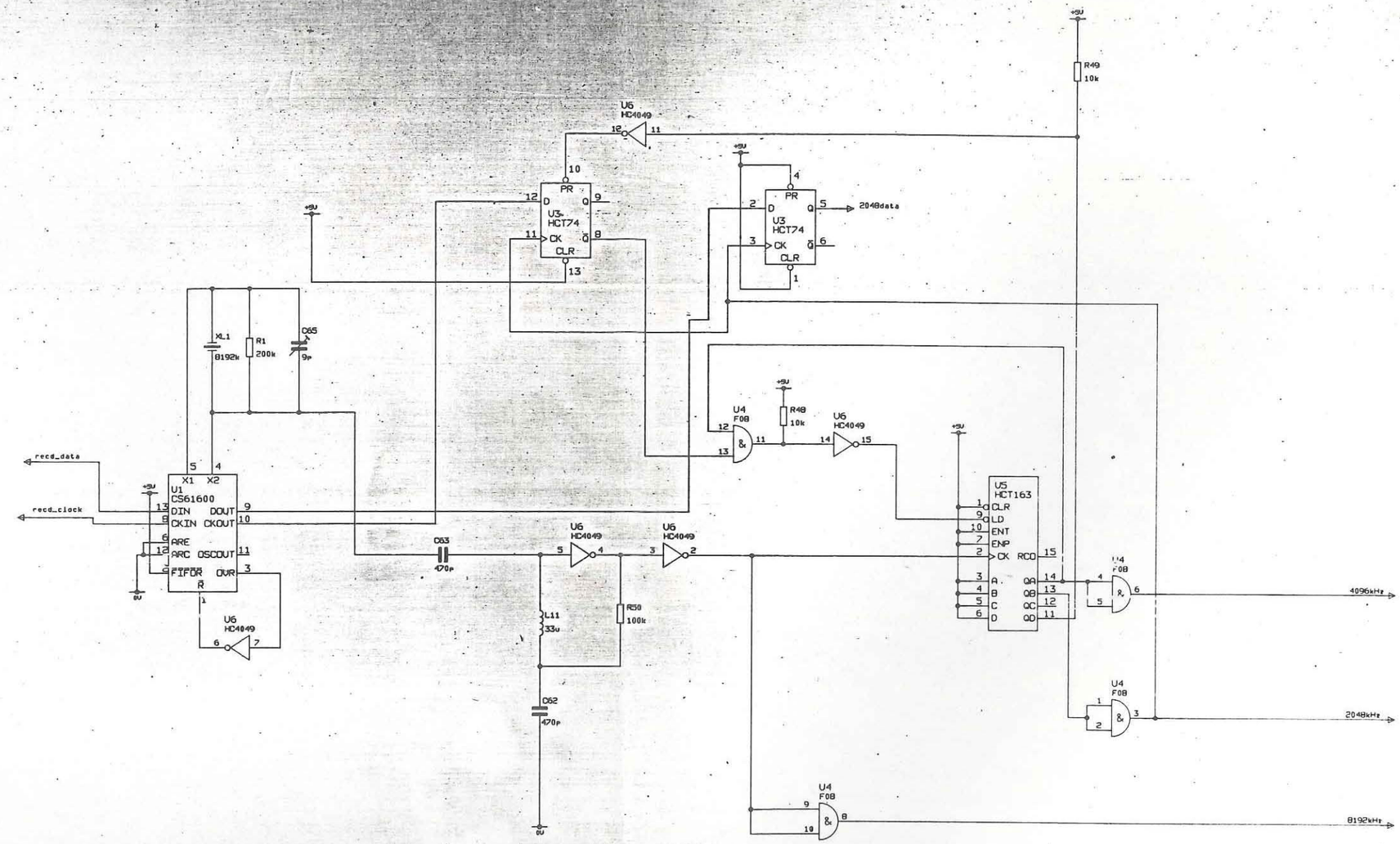
CKD.

APPD CAC

DESIGN & EQUIPTMENT DEPARTMENT

D62630A1

SHEET 4 OF 5 SHEETS



D62630A1

SCALE: – 0

PARTS LIST D62631A4

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE 574mm x 821mm

CHANGE 18/6/99

NICAM MKII DIGITAL

UN26/99

CIRCUIT

All dimensions in millimetres unless otherwise stated. Normal tolerances: no decimal place ± 1 mm unless; one decimal place ± 0.3 mm otherwise; two decimal places ± 0.1 mm stated

DRN. DI

TCD.

CKD.

APPD. CCC

DESIGN & EQUIPMENT DEPARTMENT

D62630A1

SHEET 5 OF 5 SHEETS

ISS.	CHANGE
7	1/2/89

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF	BBC REF. OR DRG. No.
			DRAWING LIST		
			CIRCUIT D62630A1 (5 SHTS)		
			PARTS LIST D62631A4		
			ASSEMBLY & WIRING D62632A2		
			DETAIL D62633A4		
			P.B. MASTERS (P. PLOTS) D62634A2s		
			P.B. ENHANCED COMP LOC DSK27046A2		
			P.B. DRILLING D62635A2		
			FURTHER INFORMATION REQUIRED FOR MANUFACTURE		
			EA10140 UNIT WIRING INFO		
			EA10484 UNIT ASSEMBLY INFO		
			UNIT SPEC ED/UN26/99		
			P5313A, P5326A		
			F1041A, F1042A, F1047A, F1048A		
1	1	*	PRINTED BOARD MANUFACTURED TO:- TO SPEC ED/P.B/UN26/99/PTH		-0626919 D62634A2s, D62635A2
2	1	*	PBd HANDLE, PLASTIC, WHITE ENGRAVED BY CONTRACTOR TO:-		S53922-0388150 D62633A4
3	1	*	6U SCREEN PLATE (UNCODED), 280mm		-0628483
4					
5					
6	1	*	I.C. HOLDER, LOW PROFILE, 0.6", 40 PIN. (1) U40		S27860-0445488
7	1	*	I.C. HOLDER, LOW PROFILE, 0.6", 28 PIN. (1) U41		S27860-0445043
8	2	*	I.C. HOLDER, LOW PROFILE, 0.6", 24 PIN. (2) U32, U37		S27860-044547X
9	3	*	I.C. HOLDER, LOW PROFILE, 0.4", 22 PIN. (3) U46, U47, U55		S27860-0445035
10	14	*	I.C. HOLDER, LOW PROFILE, 0.3", 24 PIN (14) U14, U15, U16, U17, U18, U19, U20, U21, U22, U23, U24, U25, U27, U30		-0619218

BBC

UN26/99

6 CHANNEL NICAM II PROCESSING

DRN.	DSI
TPD	
CKD	

D&ED

D62631A4

SHT 1 OF 10

CHANGE 1/2/89 TISS. 1

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
11	2	*	I.C. HOLDER, LOW PROFILE, 0.3" 20 PIN (2) U43, U48		S27860-0439423
12	4	*	I.C. HOLDER, LOW PROFILE, 0.3" 16 PIN (4) U10, U26, U44, U45		S27860-040704X
13	3	*	I.C. HOLDER, LOW PROFILE, 0.3" 14 PIN (3) U1, U4, U31		S27860-0445461
14	6	*	I.C. HOLDER, LOW PROFILE, 0.3" 8 PIN (6) U11, U12, U13, U33, U34, U56		S27860-0445453
15	3	*	LED DISPLAY SOCKET, 90° MNTG. (3) ND1, ND2, ND3		-0488508
16					
17					
18	9	*	SWITCH, BCD, VERTICAL DEC, PCB MTG., RS 334-937 (9) S1, S2, S3, S4, S5, S6, S7, S8, S9		-0626927
19					
20	2	*	PLUG, FIXED, 40°, 64 POLE, G06 (2) PL1, PL2		S25090-0610062
21					
22	1	*	TEST POINT (1) TP1		S28650-039229X
23					
24					
			RESISTORS		
30	1	*	15Ω, 2.5W, ±5% WIRE WOUND. (1) R35		S27051-023201X
31	1	*	75Ω, 0.4W, ±2% METAL FILM (1) R2		S26877-0098992
32	3	*	100Ω, 0.4W, ±2% METAL FILM (3) R42, R43, R44		S26877-0099007
33	1	*	470Ω, 0.4W, ±2% METAL FILM (1) R34		S26877-009904X

BBC

UN26/99
PARTS LIST

DRN.	DSI
TPD	
CKD	
APPD	

D&ED
D62631A4
SHT 2 OF 10

ISS.	1	2
CHANGE	1/2/89	22/5/89

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
34	3	*	560Ω, 0·4W, ± 2% METAL FILM (3) R23, R45, R46		S26877-0227953
35	3	*	1KΩ, 0·4W, ± 2% METAL FILM (3) R31, R32, R33		S26877-0099082
36	2	*	1·8KΩ, 0·4W, ± 2% METAL FILM (2) R15, R47		S26877-0099484
37	2	*	2KΩ, 0·4W, ± 2% METAL FILM (2) R8, R17		S26877-0099137
38	1	*	2·2KΩ, 0·4W, ± 2% METAL FILM (1) R14		S26877-0099145
39	2	*	2·7KΩ, 0·4W, ± 2% METAL FILM (2) R30, R13		S26877-0099492
40	3	*	3·3KΩ, 0·4W, ± 2% METAL FILM (3) R4, R9, R25		S26877-0099161
41	6	*	10KΩ, 0·4W, ± 2% METAL FILM (6) R5, R7, R18, R20, R48, R49		S26877-0099224
42	1	*	22KΩ, 0·4W, ± 2% METAL FILM (1) R22		S26877-0228078
43	1	*	24KΩ, 0·4W, ± 2% METAL FILM (1) R19		S26877-0228086
44	5	*	33KΩ, 0·4W, ± 2% METAL FILM (5) R3, R6, R10, R11, R24		S26877-0099259
45	2	*	68KΩ, 0·4W, ± 2% METAL FILM (2) R16, R21		S26877-0099520
46	1	*	82KΩ, 0·4W, ± 2% METAL FILM (1) R36		S26877-0228165
47	2	*	100KΩ, 0·4W, ± 2% METAL FILM (2) R12, R50		S26877-0228181
48	1	*	200KΩ, 0·4W, ± 2% METAL FILM (1) R1		S26877-0099275
49					
50	1	*	3KΩ, 0·4W, ± 2%, METAL FILM (1) R51		S26877-0099362

BBC

UN26/99
PARTS LIST

DRN.	DSI
TPD.	
CKD.	
APPD	PCC

D & ED
D62631A4
SHT 3 OF 10

ISS. 1

CHANGE REF. 1/2/89

ITEM No.	No. OFF		DESCRIPTION	C'CT REF	BBC REF. OR DRG. No.
51					
52	4	*	4x 470Ω, NETWORK, 8PIN, ± 2%		S27076-042815X
			(4) R26, R27, R28, R29		
53	5	*	8x 10KΩ NETWORK, 9 PIN, ± 5%		S27075-0428038
			(5) R37, R38, R39, R40, R41		
54					
55					
			I.C.'s		
60	1	*	SSD/DIC 74LS00N		-0177590
			(1) U31		
			WARNING - SSD's. TO AVOID DAMAGE FROM STATIC CHARGES GREAT CARE SHOULD BE TAKEN WHEN HANDLING THESE DEVICES.		
61	2	*	LM319N		-0187213
			(2) U8, U9		
62	1	*	SSD/DIC2716N		-0193219
			(1) U32 - PROGRAMMED TO P5313A		-07000026
63	1	*	LM78L12ACZ		-0194626
			(1) U7		
64	1	*	SSD/Z80A		-0503824
			(1) U40		
65	4	*	9638RC		-0505695
			(4) U11, U12, U13, U56		
66	1	*	SSD/DIC74F08N		-0507551
			(1) U4		
67	2	*	AM2833PC		-0508654
			(2) U33, U34		
68	1	*	SSD/DIC2712BN-250NS		-0514049
			(1) U41 - PROGRAMMED TO P5326A		-07000034
69	3	*	UCN6801A		-051621X
			(3) U46, U47, U55		
70	1	*	SSD/DIC6116LP-150nS		-051885X
			(1) U37		

BBC

UN26/99

PARTS LIST

DRN.	DSI
TPD.	
CKD.	
APPD	CCC

D & ED

D62631A4

SHT 4 OF 10

S/PLA4

ISS. 7

CHANGE E: 1/2/89

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF	BBC REF. OR DRG. No.
51					
52	4	*	4x 470Ω, NETWORK, 8PIN, ± 2%		S27076-042815X
			(4) R26, R27, R28, R29.		
53	5	*	8x 10KΩ NETWORK, 9 PIN, ± 5%		S27075-0428038
			(5) R37, R38, R39, R40, R41		
54					
55					
			I.C.'s		
60	1	*	SSD/DIC 74LS00N		-0177590
			(1) U31		
			WARNING - SSD's. TO AVOID DAMAGE FROM STATIC CHARGES GREAT CARE SHOULD BE TAKEN WHEN HANDLING THESE DEVICES.		
61	2	*	LM319N		-0187213
			(2) U8, U9		
62	1	*	SSD/DIC 2716N		-0193219
			(1) U32 - PROGRAMMED TO P5313A		-07000026
63	1	*	LM78L12ACZ		-0194626
			(1) U7		
64	1	*	SSD/Z80A		-0503824
			(1) U40		
65	4	*	9638RC		-0505695
			(4) U11, U12, U13, U56		
66	1	*	SSD/DIC74F08N		-0507551
			(1) U4		
67	2	*	AM2833PC		-0508654
			(2) U33, U34		
68	1	*	SSD/DIC2712BN-250NS		-0514049
			(1) U41 - PROGRAMMED TO P5326A		-07000034
69	3	*	UCN6801A		-057621X
			(3) U46, U47, U55		
70	1	*	SSD/DIC6116LP-150nS		-051885X
			(1) U37		

BBC /S/PLA4

UN26/99
PARTS LIST

DRN.	DSI
TPD.	
CKD.	
APPD	CCC

D&ED
D62631A4
SHT 4 OF 10

D62631A4

ISS.	CHANGE
7	1/2/89

ITEM No.	No. OFF		DESCRIPTION	CCT REF	BBC REF. OR DRG. No.
71	2	*	DMPAL 20X10NC		- 0530187
			(1) U27 - PROGRAMMED TO - F1048A		- 07000042
			(1) U30 - PROGRAMMED TO - F1047A		- 07000050
72	1	*	SSD/DIC 74HCT04N		- 052685X
			(1) U38		
73	1	*	SSD/DIC74HCT123N		- 0525722
			(1) U26		
74	3	*	SSD/DIC 74HCT138N		- 052603X
			(3) U44, U45, U49		
75	1	*	SSD/DIC 74HCT 163N		- 05284 28
			(1) U5		
76	5	*	SSD/DIC 74HCT 257N		- 0530073
			(5) U50, U51, U52, U53, U54		
77	2	*	SSD/DIC 74 HCT 32N		- 0528444
			(2) U28, U39		
78	4	*	SSD/DIC 74HCT 377N		- 0522152
			(4) U29, U35, U36, U42		
79	1	*	SSD/DIC 74 HCT 74N		- 0522073
			(1) U3		
80	2	*	SSD/DIC 74LS244N		- 0199133
			(2) U43, U57		
81	1	*	SSD/DIC 74LS322N		- 0511623
			(1) U48		
82	1	*	LM79L12ACZ		- 0197348
			(1) U2		
83	1	*	CS61600-IP1		- 0530081
			(1) U1		
84	12	*	EP600DC		- 053009X
			(6) U14, U16, U18, U20, U22, U25 - PROG TO F1041A		- 0700000X
			(6) U16, U17, U19, U21, U23, U24 - PROG TO F1042A		- 07000018
85	1	*	SSD/DICHC4049N		- 0530101
			(1) U6		
86	1	*	MJ1440DP		- 053011X
			(1) U10		
87					

BBC

JS/PLA4

UN26/99

PARTS LIST

DRN	DSI
TPD	-
CKD	
APPD	CCC

D & ED

D62631A4

ISS.	CHANGE
1	1/2/89
2	22/5/89

ITEM No.	No. OFF		DESCRIPTION	CCT REF	BBC REF. OR DRG. No.
88					
89					
90					
			TRANSISTORS		
95	6	*	2N3904		-0122792
			(6) Q3, Q4, Q6, Q7, Q8, Q9		
96	1	*	CA3096AE		-0174828
			(1) Q1		
97	2	*	BFY50		-0173779
			(2) Q2, Q5		
98					
99					
			DIODES		
100	5	*	1N4148		-0102612
			(5) D5, D6, D7, D24, D25		
101	2	*	BAV10		-0162916
			(2) D1, D2		
102	2	*	VZ10M4		-0417258
			(2) D3, D4		
103					
104	3	*	TIL311, SEGMENTED DISPLAY, RED		-0174189
			(3) ND1, ND2, ND3		
105	8	*	DUAL GREEN LED, 90° PCB MNTG, LEDTECH LTB3H2G		-0531263
			(8) D8, D9, D10, D11, D12, D13, D14, D15		
106					
107					
			CAPACITORS		
108	1	*	1.8 - 9pF VARIABLE		S21287 - 0447080
			(1) C65		

BBC

UN26/99
PARTS LIST

DRN.	DSI
TPD	
CKD	
APPD	ACC

D & ED
D62631A4
SHT 6 OF 10

ISS.	1	2
CHANGE	1/2/89	22/5/89

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF	BBC REF. OR DRG. No.
110	40	*	10n, 100V, MULTILAYER (40) C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61.		S20647 - 0099669
111	8	*	1nF, 100V, MULTILAYER (8) C3, C5, C6, C7, C8, C9, C10, C19		S20647 - 0207737
112	5	*	100nF, 50V, MULTILAYER (5) C1, C2, C4, C12, C20		S20648 - 0204648
113	1	*	330nF, 50V, MULTILAYER (1) C21		S20648 - 038983X
114	1	*	390pF, 63V, RECTANGULAR, POLYSTYRENE (1) C11		S21005 - 0450104
115	6	*	220nF, 160V, RECTANGULAR, POLYCARBONATE (6) C13, C14, C15, C16, C17, C18		S21030 - 020896X
116	2	*	470pF, 63V, RECTANGULAR, POLYCARBONATE (2) C62, C63		S21005 - 0450120
117	1	*	20pF, 160V, POLYSTYRENE (1) C64		S21004 - 020827X
118					
			INDUCTORS		
120	2	*	22µH, CHOKE, R.F. SHIELDED. (2) L1, L2		S21472 - 0403915
121	1	*	15µH, TOKO 119ANA5873HM - PINK (1) L4		- 0481428
122	6	*	L/12235 (6) L5, L6, L7, L8, L9, L10		- 0499928
123	1	*	33µH, CHOKE, R.F SHIELDED (1) L11		S21471 - 0206571
124					
125	1	Θ*	8192kHz, XTAL, CATHODEON (1) XL1		- 0626880

BBC

UN26/99
PARTS LIST

DRN.	DSI
TPD	
CKD.	
APPD	CCC

D62631A4
SHT 7 OF 10

D62631A4/PL.A4

D62631A4

ISS.	CHANGE
1	1/2/89
2	22/5/89

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
130	1	*	ANTI STATIC PLASTIC BAG, 10" x 12"		-0613387
131	2	*+	SPACER, CERAMIC, 3·2 Ø x 4·0 LG		S58261-0255439
132					
133	A/R		B.T.C. 1·0 Ø		
144	A/R		B.T.C. 1·8 Ø		
145					
146					
147					
148					
			FIXINGS		FOR FIXING ITEMS
150	9		SCREW, PAN HD, M2·5 x 8 LG, M.S. Zn. PL, SLOTTED		1 & 3
151	4		SCREW, PAN HD, M2·5 x 10 LG, M.S. Zn PL, SLOTTED		20 & 1
152					
153					
154	4		NUT, FULL, HEX		20 & 1
155					
156	13		WASHER, PLAIN, M2·5		
157					
158	1		CARTON CARD BOARD TO SPEC ED/UN26/99		

Notes

*	Denotes items supplied to the contractor on embodiment loan
*+	Denotes items supplied to the contractor on embodiment loan, requiring special costing or supply action by B.B.C.
θ *	Denotes components supplied and fitted by B.B.C. on test.
θ +	Denotes coded plug in units supplied and fitted by B.B.C. on test.
Ø	Denotes items supplied and fitted by B.B.C. on installation.

BBC
S/PLA4

UN26/99
PARTS LIST

DRN.	DSI
TPD.	
CKD.	
APPD	ACC

D & ED
D62631A4
SHT 8 OF 10

CIRCUIT REFERENCES.....

CAPACITORS

C1	112
C2	112
C3	111
C4	112
C5	111
C6	111
C7	111
C8	111
C9	111
C10	111
C11	114
C12	112
C13	115
C14	115
C15	115
C16	115
C17	115
C18	115
C19	111
C20	112
C21	113
C22 - C61	110

DIODES

D1	101
D2	101
D3	102
D4	102
D5	100
D6	100
D7	100
D8 - D15	105
ND1	104
ND2	104
ND3	104
C62	116
C63	116
C64	117
C65	108
D24	100
D25	100

RESISTORS

R1	48
R2	31
R3	44
R4	40
R5	41
R6	44
R7	41
R8	37
R9	40
R10	44
R11	44
R12	47
R13	39
R14	38
R15	36
R16	41
R17	37
R18	41
R19	43
R20	41
R21	45
R22	42
R23	54
R24	44
R25	40
R26	52
R27	52
R28	52
R29	52
R30	39
R31	37
R32	37
R33	35
R34	33
R35	30
R36	46
R37	53
R38	53
R39	53
R40	53
R41	53
R42	32
R43	32
R44	32
R45	34
R46	34
R47	36
R48	41
R49	41
R50	47
R51	50

I.C.

U1	83
U2	82
U3	79
U4	66
U5	75
U6	81
U7	63
U8	61
U9	61
U10	86
U11	67
U12	67
U13	65
U14	84
U15	84
U16	84
U17	84
U18	84
U19	84
U20	84
U21	84
U22	84
U23	84
U24	84
U25	84
U26	73
U27	71
U28	77
U29	78
U30	71
U31	60
U32	62
U33	67
U34	67
U35	78
U36	78
U37	70
U38	72
U39	77
U40	64
U41	68
U42	78
U43	80
U44	74
U45	74
U46	69
U47	69
U48	81
U49	74
U50	76
U51	76
U52	76
U53	76
U54	76
U55	69
U56	65
U57	80

SWITCHES

S1	18
S2	18
S3	18
S4	18
S5	18
S6	18
S7	18
S8	18
S9	18

TRANSISTORS

Q1	96
Q2	97
Q3	95
Q4	95
Q5	97
Q6	95
Q7	95
Q8	95
Q9	95

INDUCTORS

L1	120
L2	120
L4	121
L5	122
L6	122
L7	122
L8	122
L9	122
L10	122
L11	123

CRYSTAL

XL1	125
TP1	22
PL1	20
PL2	20

ORIGINAL FRAME SIZE 190mm x 277mm

THIRD ANGLE PROJECTION

All dimensions in millimetres unless otherwise stated:
Normal tolerances:
no decimal place - ± 1 mm unless
one decimal place - ± 0.3 mm otherwise
two decimal places - ± 0.1 mm stated

SCALE: - 0

BBC

DS/A4

ISS	CHANGE
1	1/2/89
2	22/5/89

UN26/99
PARTS LIST

DRN.	DSH	D&ED
TCD.		D62631A4
CKD.		
APPD.	CCC	SHT 9 OF 10

R297

SHT.	ISS.	DETAILS OF CHANGE	SHT.	ISS.	DETAILS OF CHANGE
3	2	R47 WAS 1Kn R13 WAS 12Kn R19 & R22 WERE 15Kn R48 - R51 ADDED.			
6	2	C65 ADDED.			
7	2	C62 - 64 ADDED L11 ADDED. L3 DELETED (WAS 22µH)			
8	2	ITEM 144 ADDED. ITEM 145 DELETED (SYMEL SLEEVE)			
9	2	CHANGED TO ABOVE INFO.			

ORIGINAL
FRAME SIZE
190mm x 277mm

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED

BBC

VM418/A4

DESIGNS DEPARTMENT

CODE:- UN26/99 22/5/89

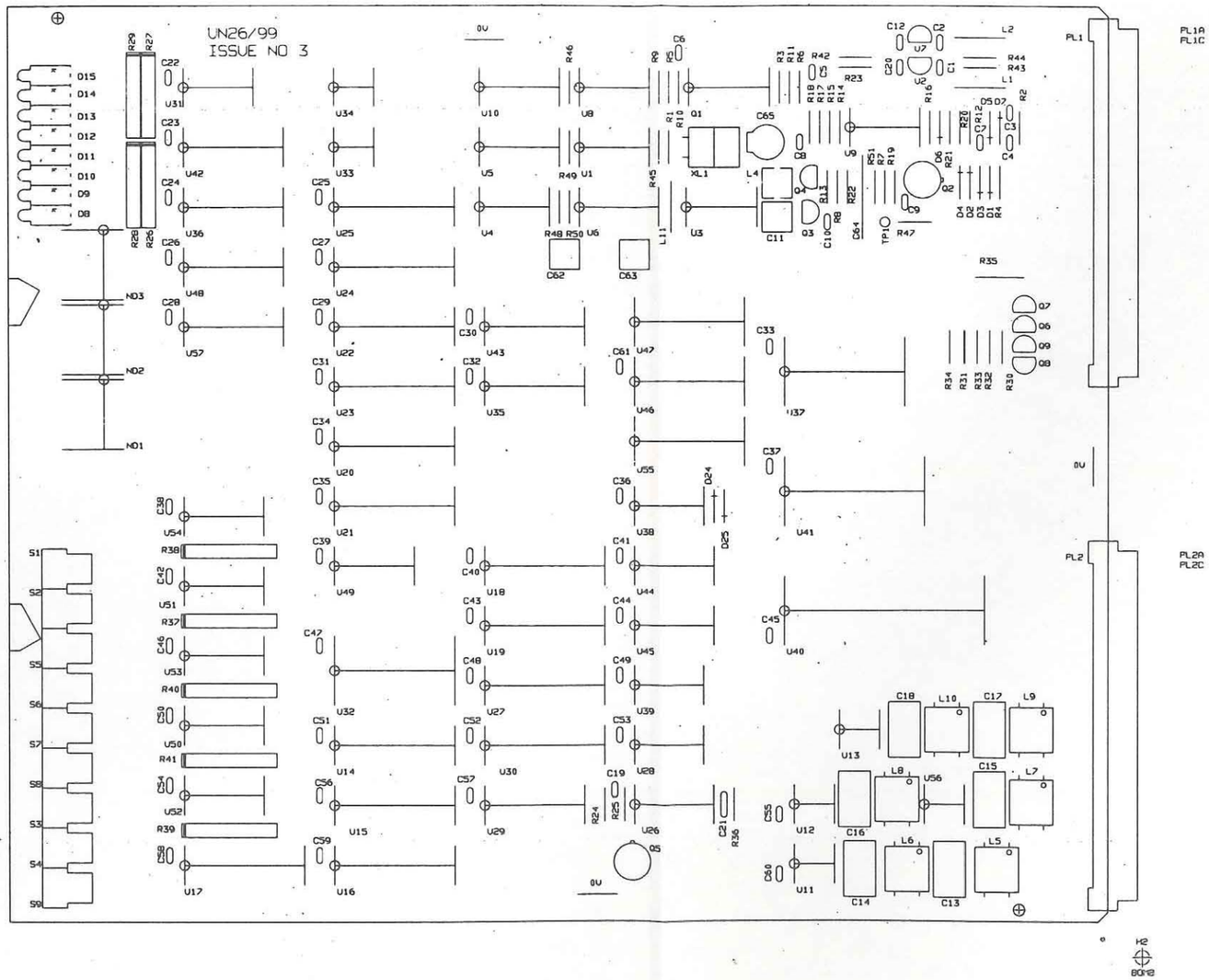
PARTS LIST CHANGE RECORD, ISSUE:- 2

D 62631 A4

SHEET 10

UN26/99

ISSUE NO 3
PTH BOARD



SCALE:- 0

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE
400mm x 574mm

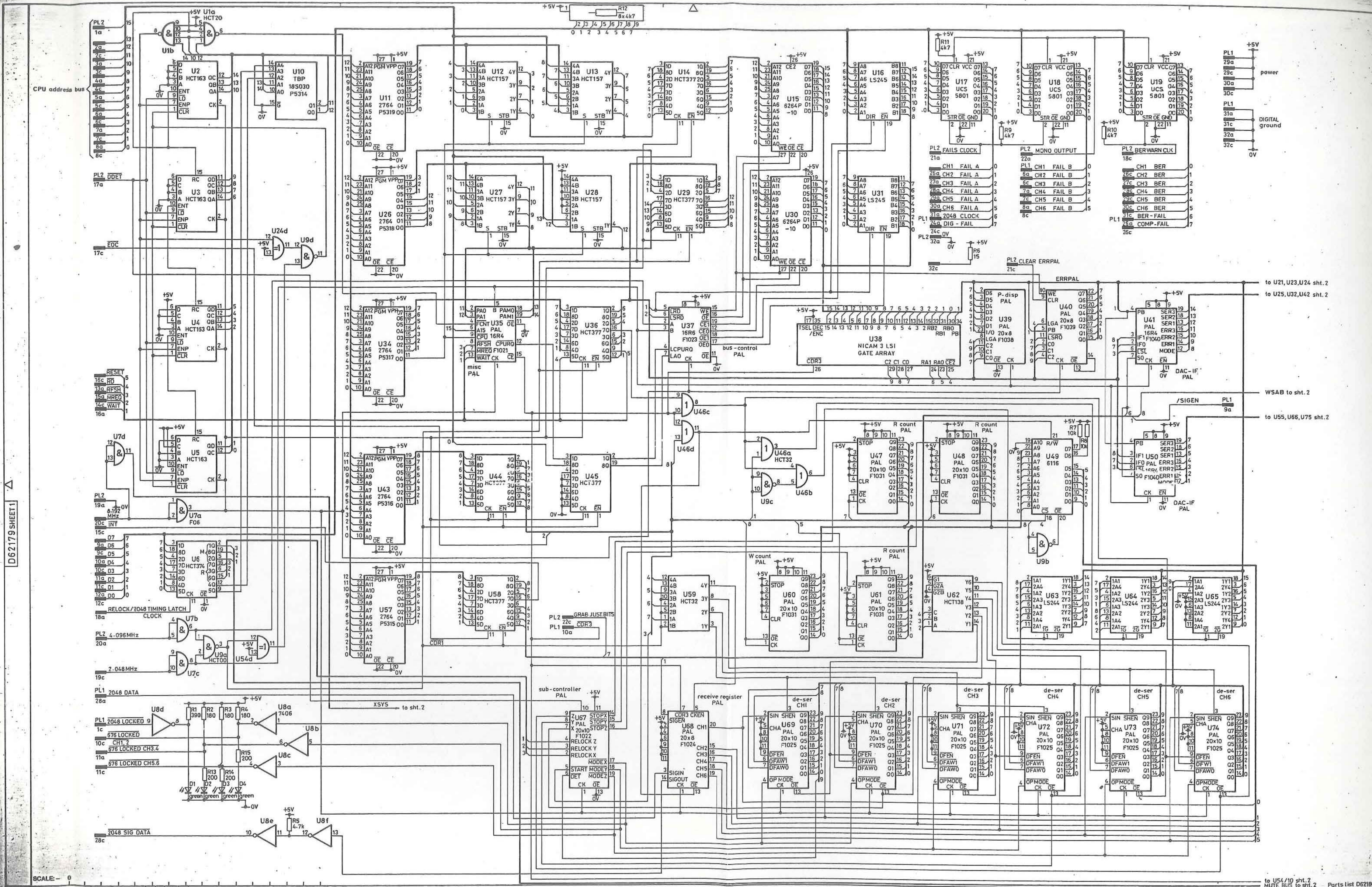
ISS	CHANGE
3	MODS TO ISS 3 OF PCB. DSK 23.5.89

UN26/99
ENHANCED
COMP. LOC.

All dimensions in millimetres unless otherwise stated: Normal tolerances:
no decimal place – ± 1 mm unless
one decimal place – ± 0.3 mm otherwise
two decimal places – ± 0.1 mm stated

DRN.	DSK	D&ED
TCD.		
CKD.		DSK 27046 A2
APPD	CCC	

DSK27046A2



THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE 574mm x 821mm

SCALE: - 0

CHANGE: 11-10-88; 1-3-89; 14-4-89

6 CHANNEL NICAM II PROCESSING UNIT

UN26/100

CIRCUIT

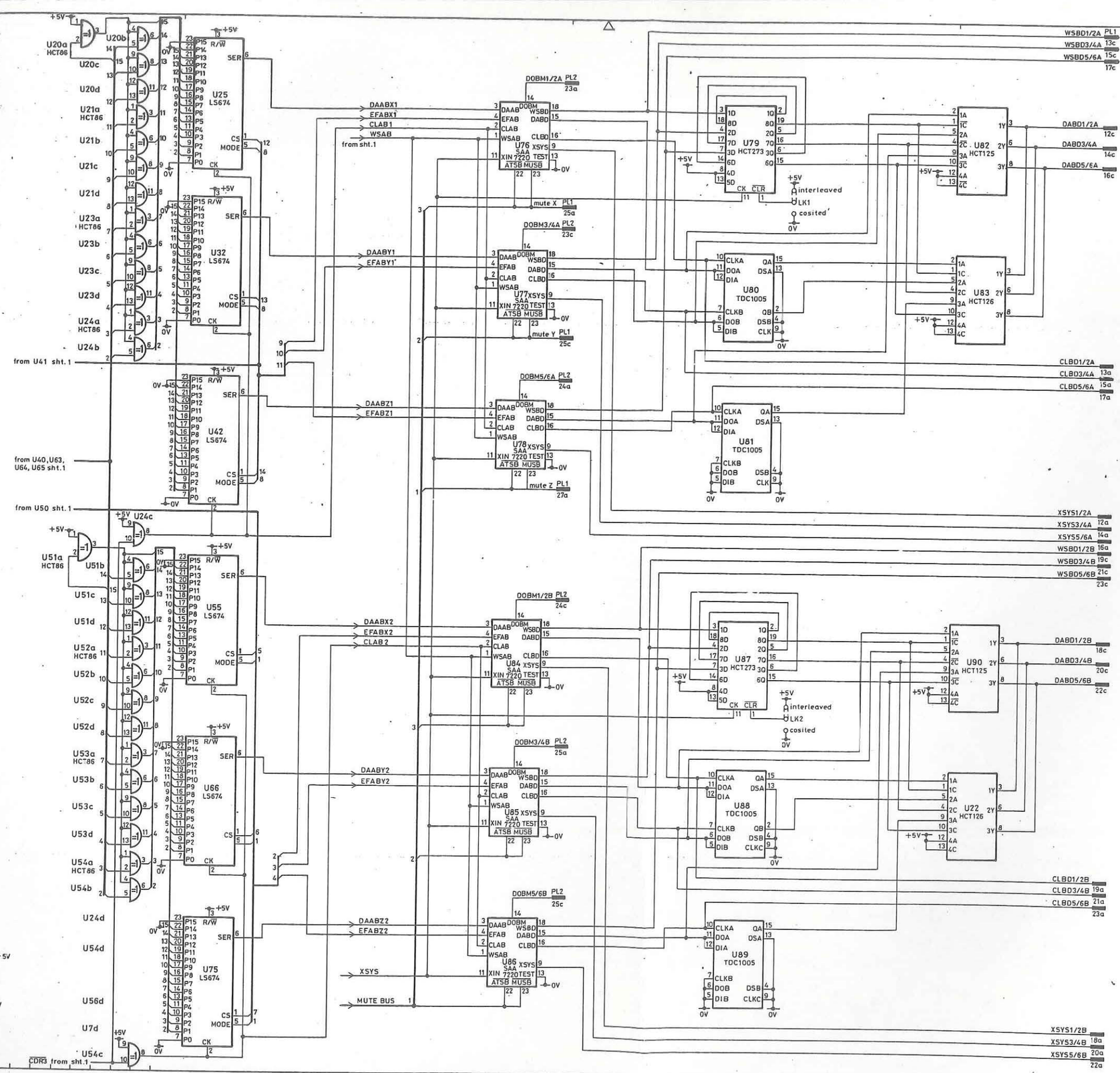
All dimensions in millimetres unless otherwise stated. Normal tolerances:
no decimal place — ± 1 mm unless
one decimal place — ± 0.3 mm otherwise
two decimal places — ± 0.1 mm stated

DRN. P.P.
TCD.
CKD.
APPD. C.C.C.

DESIGN & EQUIPMENT DEPARTMENT

D62179 A1

SHEET 1 OF 2 SHEETS



U CIRCUIT REFERENCE	TYPE	SUPPLY CONNECTIONS +5V	0V	-5V
U1	HCT20	14	7	
U2.U3.U4.U5	HCT163	16	8	
U6	HCT374	20	10	
U7.U9	HCT00	14	7	
U8	7406	14	7	
U10	TBP18S030	16	8	
U11.U26.U34.U43. U57	2764	28	14	
U12.U13.U27.U28	HCT157	16	8	
U14.U29.U36.U44. U45.U58	HCT377	20	10	
U15.U30	6264P-10	28	14	
U16	LS245	20	10	
U17.U18.U19	UCS5801	21	11	
U20.U21.U23.U24. U51.U52.U53.U54	HCT86	14	7	
U22.U83	HCT126	14	7	
U25.U32.U42.U55. U66.U75	LS674	24	12	
U31	LS245	20	10	
U35.U41.U50	PAL16R4	20	10	
U37	16R6	20	10	
U38	NICAM gate array	16.40	1.20	
U39.U40.U68	PAL 20x8	24	12	
U46.U59	HCT32	14	7	
U47.U48.U60.U61. U67.U69-U74	PAL 20x10	24	12	
U49	6116	24	12	
U62	HCT138	16	8	
U63.U64.U65	LS244	20	10	
U76.U77.U78. U84.U85.U86	SAA 7220	24	12	
U79	HCT273	20	10	
U80.U81.U87-U89	TDC1005	16	8	
U82.U90	HCT125	14	7	

D62179 SHEET 2

SCALE:- 0 1

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE 574mm x 821mm

CHANGE			
11-10-88	1-3-89	14-6-89	
0	1	2	3

6 CHANNEL NICAM II PROCESSING UNIT

UN26/100 CIRCUIT

All dimensions in millimetres unless otherwise stated: Normal tolerances: no decimal place ± 1 mm unless one decimal place ± 0.3 mm otherwise two decimal places ± 0.1 mm stated

DRN.	P.P.	DESIGN & EQUIPMENT DEPARTMENT
TCD.		
CKD.		D62179A1
APPD.	C.E.C.	SHEET 2 OF 2 SHEETS

D62180A4

ISS.	CHANGE
1	1/2/89
2	3/7/89

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF	BBC REF. OR DRG. No.
			DRAWINGS LIST		
			CIRCUIT D62179A1 (2 SHTS)		
			PARTS LIST D62180A4		
			ASSEMBLY & WIRING D62181A2		
			DETAIL D62182A4		
			PB. MASTERS (PHOTO PLOTS) D62183A2s		
			PB. ENHANCED COMP LOC DSK27045A2		
			DRILLING D62185A2		
			FURTHER INFORMATION REQUIRED FOR MANUFACTURE		
			EA10140 UNIT WIRING INFO		
			EA10484 UNIT ASSY INFO		
			UNIT SPEC ED/UN26/100		
			P5314A, P5315A, P5316A, P5317A, P5318A, P5319A		
			F1049A, F1050A, F1051A, F1052A, F51053A, F1054A, F1057A, F1058A, F1059A		
1	1	*	PRINTED BOARD MANUFACTURED TO TO SPEC ED/PB/UN26/100/PTH		0625343 D62183A2s, D62185A2
2	1	*+	PBd HANDLE ENGRAVED BY CONTRACTOR TO:-		S53922-0388150 D62182A4
3	1	*	6U SCREEN PLATE (UNCODED), 280mm		-0628483
4	1	*	RUBBER FOOT, SELF ADHESIVE		-0497371
5	2	Δ	HEADER, 3 WAY, MADE BY CONTRACTOR FROM ITEM 6 (2) LK1, LK2		
6	1	*+	HEADER, 36 WAY, BERG STICK 75160-101-36		-0457322
7	2	*	LINK, MINIJUMP, BERG 65474 (2) LK1, LK2		-0464325
8					
9	6	*	I.C. HOLDER, LOW PROFILE, 0·6", 24 PIN (6) U76, U77, U78, U84, U85, U86		S27860-044547X
10	5	*	I.C. HOLDER, LOW PROFILE, 0·6", 28 PIN (5) U11, U26, U34, U43, U57		S27860-0445043

BBC

UN26/100
6 CHANNEL NICAM II PROCESSING
UNIT 2. — PARTS LIST

DRN.	DSI
TPD.	
CKD.	
APPD	CAC

D&ED
D62180A4
SHT 1 OF 9

D62180DA4-

ISS.	CHANGE
1	1/2/89
2	3/7/89

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
11	1	*	IC HOLDER, LOW PROFILE, 0·6", 40 PIN		S27860 - 0445488
			(1) U38		
12	3	*	IC HOLDER, LOW PROFILE, 0·4", 22 PIN		S27860 - 0445035
			(3) U17, U18, U19		
13	6	*	IC HOLDER, LOW PROFILE, 0·3", 14 PIN		S27860 - 0445461
			(6) U7, U8, U22, U82, U83, U90		
14	13	*	IC HOLDER, LOW PROFILE, 0·3", 16 PIN		S27860 - 0407Q4X
			(13) U2, U3, U4, U5, U10, U12, U13, U27, U28, U80, U81, U88, U89		
15	11	*	IC HOLDER, LOW PROFILE, 0·3", 20 PIN		S27860 - 0439423
			(11) U6, U16, U31, U35, U36, U37, U41, U44, U50, U79, U87		
16	14	*	IC HOLDER, LOW PROFILE, 0·3", 24 PIN (FARNELL 170-718)		- 0619218
			(14) U39, U40, U47, U48, U60, U61, U67, U68, U69, U70, U71, U72, U73, U74		
17					
18					
19					
20	2	*	PLUG, FIXED, 90° MOUNTING, 64 POLE		S25090 - 0610062
			(2) PL1, PL2		
			RESISTORS		
30	3	*	180Ω, 0·4W, ±2%, METAL FILM		S26877 - 0227910
			(3) R2, R3, R4		
31	1	*	390Ω, 0·4W, ±2% METAL FILM		S26877 - 0099354
			(1) R1		
32	3	*	4·7KΩ, 0·4W, ±2% METAL FILM		S26877 - 0099425
			(3) R5, R9, R10, R11		

BBC

3/PLA4

UN26/100
PARTS LIST

DRN.	DSI
TPD.	
CKD.	
APPD	CCC

D&ED

D62180A4

SHT 2 OF 9

ISS.	1	2
CHANGE	1/2/89	3/7/89

ITEM No.	No. OFF		DESCRIPTION	CCT REF	BBC REF. OR DRG. No.
33	1	*	15Ω, 2·5W, ±5%, WIREWOUND		S26931-023201X
			(1) R6		
34	2	*	10KΩ, 0·4W, ±2%, METAL FILM		S26877-0099224
			(2) R7, R8		
35	1	*	4·7KΩ x 8, ±5%, NETWORK		S27075-042802X
			(1) R12		
36	3	*	200Ω, 0·4W, ±2%, METAL FILM		S26877-0099015
			(3) R13, R14, R15		
37					
38					
39					
			I.C.s		
			SSD's TO AVOID DAMAGE FROM STATIC CHARGES GREAT CARE SHOULD BE TAKEN WHEN HANDLING THESE DEVICES.		
40	1	*	SSD/1/DIC 74HCT20N		0529922
			(1) U1		
41	4	*	SSD/1/DIC 74HCT163N		0528428
			(4) U2, U3, U4, U5		
42	1	*	SSD/1/DIC 74HCT374N		0529930
			(1) U6		
43	1	*	SSD/1/DIC 74F08N		0507551
			(1) U7		
44	1	*	DIC 7406N		0153489
			(1) U8		
45	1	*	SSD/1/DIC 74HCT00N		0522081
			(1) U9		
46	1	*	TBP18S030N		0182162
			(1) U10 - PROGRAMMED TO P5314A		07000069
47	5	*	SSD/DIC 2764N		0513758
			(1) U11 PROGRAMMED TO P5319A		07000077
			(1) U26 " P5318A		07000085
			(1) U34 " P5317A		07000093
			(1) U43 " P5316A		07000105
			(1) U57 " P5315A		07000113

BBC

UN26/100
PARTS LIST

DRN.	DJI
TPD.	
CKD	
APPD	CCC

D & ED

D62180A4

SHT 3 OF 9

D62180A4

ISS.	CHANGE
1	1/2/89

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
48	4	*	SSD/1/DIC74HCT157N		-0529949
			(4) U12, U13, U27, U28		
49	6	*	SSD/1/DIC HCT377N		-0522152
			(6) U14, U29, U36, U44, U45, U58		
50	2	*	SSD/DIC6264		-0518431
			(2) U15, U30		
51	2	*	SSD/DIC74LS245N		-0196698
			(2) U16, U31		
52	8	*	SSD/1/DIC74HCT86N		-0528452
			(8) U20, U21, U23, U24, U51, U52, U53, U54		
53	6	*	SSD/DIC74LS674		-0530049
			(6) U25, U32, U42, U66, U75, U55		
54					
55	3	*	SSD/PAL16R4		-0525773
			(1) U35 - PROGRAMMED TO F1049A		-07000121
			(2) U41, U50 " F1059A		-07000138
56	1	*	SSD/PAL16R6		-0529973
			(1) U37 - PROGRAMMED TO F1051A		-07000148
57	1	*	LSI GATE ARRAY		-0524279
			(1) U38		
58	3	*	SSD/PAL20X8		-0523961
			(1) U39 - PROGRAMMED TO - F1057A		-07000156
			(1) U40 " F1058A		-07000164
			(1) U68 " F1052A		-07000172
59	2	*	SSD/1/DIC74HCT32N		-0528444
			(2) U46, U59		
60	11	*	SSD/PAL20X10		-0524035
			(4) U47, U48, U60, U61 - PROGRAMMED TO F1054A		-07000180
			(1) U67 " F1050A		-07000199
			(6) U69, U70, U71, U72, U73, U74 " F1053A		-07000200
61	1	*	SSD/DIC6116LP-150nS		-051885X
			(1) U49		
62	1	*	SSD/1/DIC74HCT138N		-052603X
			(1) U62		

BBC

S/PLA4

UN26/100 PARTS LIST

DRN	DJI
TPD.	
CKD.	
APPD	CCC

D&ED

D62180A4

SHT 4 OF 9

ISS.	1
CHANGE	1/2/89

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
48	4	*	SSD/1/DIC74HCT157N		-0529949
			(4) U12, U13, U27, U28		
49	6	*	SSD/1/DIC HCT377N		-0522152
			(6) U14, U29, U36, U44, U45, U58		
50	2	*	SSD/DIC6264		-0518431
			(2) U15, U30		
51	2	*	SSD/DIC74LS245N		-0196698
			(2) U16, U31		
52	8	*	SSD/1/DIC74HCT86N		-0528452
			(8) U20, U21, U23, U24, U51, U52, U53, U54		
53	6	*	SSD/DIC74LS674		-0530049
			(6) U25, U32, U42, U66, U75, U55		
54					
55	3	*	SSD/PAL16R4		-0525773
			(1) U35 - PROGRAMMED TO F1049A		-07000121
			(2) U41, U50 " F1059A		-0700013X
56	1	*	SSD/PAL16R6		-0529973
			(1) U37 - PROGRAMMED TO F1051A		-07000148
57	1	*	LSI GATE ARRAY		-052.4279
			(1) U38		
58	3	*	SSD/PAL20X8		-0523961
			(1) U39 - PROGRAMMED TO - F1057A		-07000156
			(1) U40 " F1058A		-07000164
			(1) U68 " F1052A		-07000172
59	2	*	SSD/1/DIC74HCT32N		-0528444
			(2) U46, U59		
60	11	*	SSD/PAL20X10		-0524035
			(4) U47, U48, U60, U61 - PROGRAMMED TO F1054A		-07000180
			(1) U67 " F1050A		-07000199
			(6) U69, U70, U71, U72, U73, U74 " F1053A		-07000200
61	1	*	SSD/DIC6116LP-150nS		-051885X
			(1) U49		
62	1	*	SSD/1/DIC74HCT138N		-052603X
			(1) U62		

BBC

S/PLA4

UN26/100 PARTS LIST

DRN	DSI
TPD.	
CKD.	
APPD	CCC

D & ED

D62180A4

SHT 4 OF 9

D62180A4

ISS.	CHANGE
1	1/2/89
2	3/7/89

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF	BBC REF. OR DRG. No.
63	3	*	SSD/DIC 74LS244N		-0199133
			(3) U63, U64, U65		
64	6	*	SSD/SAA 7220		-0529981
			(6) U76, U77, U78, U84, U85, U86		
65	2	*	SSD/1/DIC 74HCT 273		-0530057
			(2) U79, U87		
66	4	*	SSD/TDC 1005-J9C		-0530006
			(4) U80, U81, U88, U89		
67	2	*	SSD/1/DIC 74HCT 125		-0529957
			(2) U82, U90		
68	2	*	SSD/1/DIC 74HCT 126		-0529965
			(2) U22, U83		
69	3	*	UCN5801A		-051621X
			(3) U17, U18, U19		

BBC S/PLA4

UN26/100
PARTS LIST

DRN.	DSI.
TPD.	
CKD.	
APPD.	CCC

D & ED

D62180A4

SHT 5 OF 9

D62180A4

ISS.	CHANGE
1	1/2/89
2	1/3/89

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF	BBC REF. OR DRG. No.
			CAPACITORS		
70					
71	49	*	10nF, 100V, MULTILAYER, ±20% (49) C7 - C55		S20647 - 0099665
			DIODES		
75	4	*	LED, MINIATURE, GREEN, HLMP1503 (4) D1, D2, D3, D4		0178878
80	1	*	ANTI STATIC PLASTIC BAG, 10" x 12"		0613387
81					
82	2	*†	SPACER, CERAMIC, 3.2Ø x 4.0LG		S58261 - 0255439
83					
84	A/R	*†	SLEEVING, SYMEL, 0.5Ø, WHITE		- 0254249
85					

BBC

S/PLA4

UN26/100
PARTS LIST

DRN.	DSI
TPD.	
CKD.	
APPD	CCC

D&ED

D62180A4

SHT 6 OF 9

ISS.	CHANGE
1	1/2/89

ITEM No.	No. OFF		DESCRIPTION	CCT REF	BBC REF. OR DRG. No.
			FIXINGS		FOR FIXING ITEMS
90	9		SCREW, PANHD, M2.5x8 LG, M.S. Zn PL, SLOTTED		1 & 3
91	4		SCREW, PAN HD, M2.5 x 10 LG, M.S. Zn PL, SLOTTED		20 & 1
92					
93					
94	4		NUT FULL HEX, M2.5		20 & 1
95					
96					
97	13		WASHER PLAIN, M2.5		1, 3, & 20
98					
99					
100	1		CARTON CARDBOARD TO SPEC ED/UN26/100		
105	A/R	**	BTC 1·8 Ø		

Notes

*	Denotes items supplied to the contractor on embodiment loan
* +	Denotes items supplied to the contractor on embodiment loan, requiring special costing or supply action by B.B.C.
θ *	Denotes components supplied and fitted by B.B.C. on test.
θ +	Denotes coded plug in units supplied and fitted by B.B.C. on test.
Ø	Denotes items supplied and fitted by B.B.C. on installation.
Δ	DENOTES 6 OFF ITEM 5 CAN BE MADE FROM 1 OFF ITEM 6.

BBC

S/PLA4

UN26/100
PARTS LIST

DRN	DSI
TPD	
CKD	
APPD	

D&ED

D62180A4

SHT 7 OF 9

CIRCUIT REFERENCES.....

C7 - C55	71
D1	75
D2	75
D3	75
D4	75
PL1	20
PL2	20
R1	
R2	30
R3	30
R4	30
R5	32
R6	33
R7	34
R8	34
R9	32
R10	32
R11	32
R12	35
LK1	[illegible]
LK2	[illegible]
R13	36
R14	36
R15	36

U1	40
U2	41
U3	41
U4	41
U5	41
U6	42
U7	43
U8	44
U9	45
U10	46
U11	47
U12	48
U13	48
U14	49
U15	50
U16	51
U17	69
U18	69
U19	69
U20	52
U21	52
U22	68
U23	52
U24	52
U25	53
U26	47
U27	48
U28	48
U29	49
U30	50
U31	51
U32	53
U34	47
U35	53
U36	49
U37	56
U38	57
U39	58
U40	58
U41	[illegible]
U42	[illegible]
U43	47
U44	49
U45	49
U46	59
U47	60
U48	60
U49	61
U50	51
U51	52
U52	52

U53	52
U54	52
U55	53
U57	47
U58	49
U59	59
U60	60
U61	60
U62	62
U63	63
U64	63
U65	63
U66	53
U67	60
U68	58
U69	60
U70	60
U71	60
U72	60
U73	60
U74	60
U75	53
U76	64
U77	64
U78	64
U79	65
U80	66
U81	66
U82	67
U83	68
U84	64
U85	64
U86	64
U87	65
U88	66
U89	66
U90	67

END OF CIRCUIT REFERENCES.

ORIGINAL FRAME SIZE 190mm x 277mm

THIRD ANGLE PROJECTION

All dimensions in millimetres unless otherwise stated:
Normal tolerances:
no decimal place ± 1 mm unless
one decimal place ± 0.3 mm otherwise
two decimal places ± 0.1 mm stated

SCALE: - 0

ISS	CHANGE
1	1/2/89
2	1/3/89
3	3/7/89

BBC

DS/A4

UN26/100 PARTS LIST

DRN.	DSI	D & ED
TCD.		D62180A4
CKD.		
APPD.	CQ	SHT 8 OF 9

R297

SHT.	ISS.	DETAILS OF CHANGE	SHT.	ISS.	DETAILS OF CHANGE
6	2	C1-C6 DELETED. DSI 1/3/89.			
1	2	ITEM 3 NOTE DEL.			
2	2	R2, R3, R4 WERE 390Ω, R7, R8 WERE 4.7KΩ R13, R14, R15 ADDED. R6 WAS 0.4W			
5	2	ITEM 64 WAS 052999X DSI 3/7/89			

ORIGINAL
FRAME SIZE
190mm x 277 mm

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED

BBC

VM418/A4

DESIGNS DEPARTMENT

CODE:- UN26/100 3/7/89

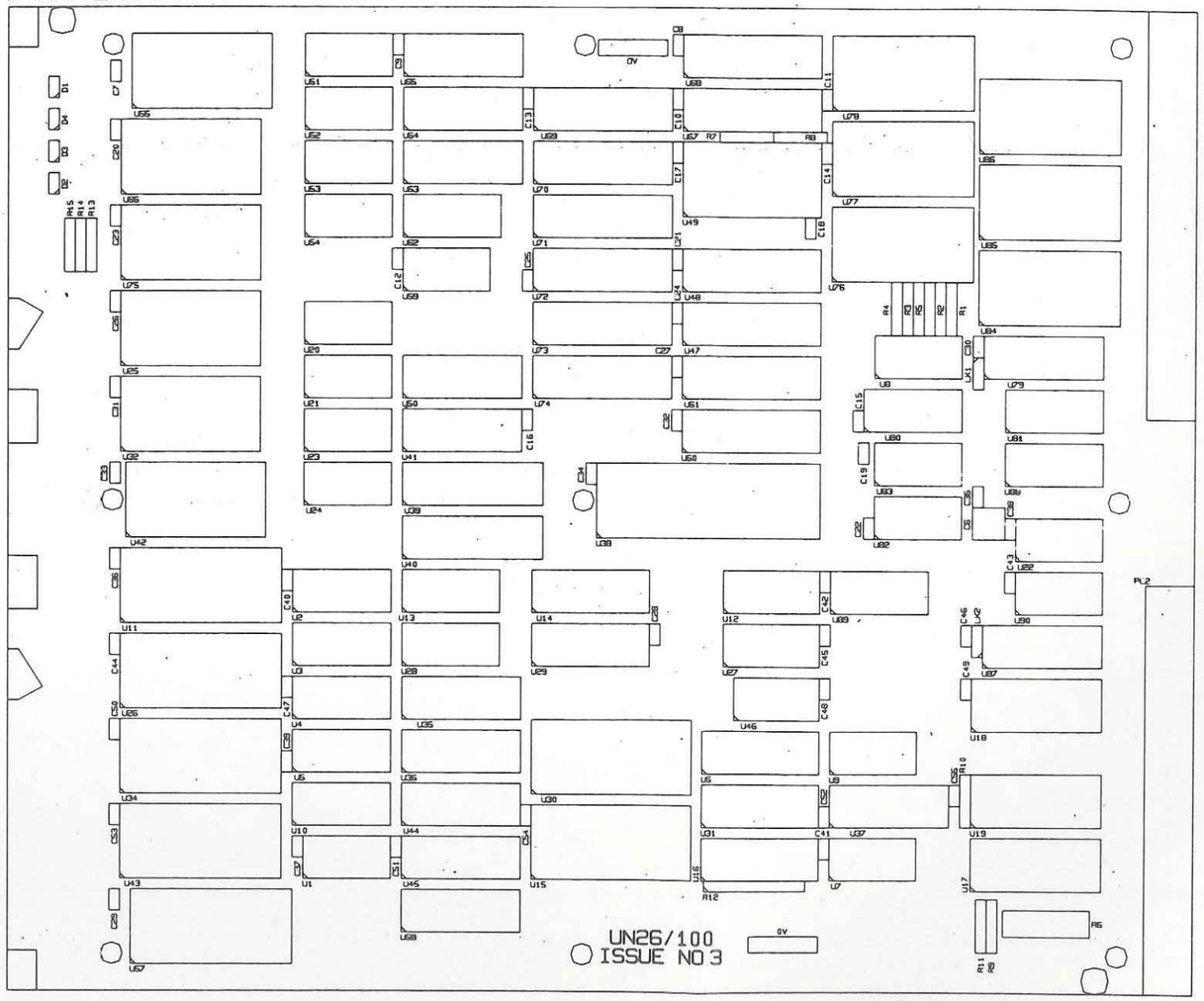
PARTS LIST CHANGE RECORD, ISSUE:- 3

D62180A4

SHEET 9

DSK27045A2

UN26/100
ISSUE NO3
PTH BOARD



SCALE: - 0

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE
400mm x 574mm

ISS 3 MODS TO ISS 3 OF B.L. DAT 23.5.89

UN26/100
ENHANCED
COMP. LOC.

All dimensions in millimetres unless otherwise stated: Normal tolerances:
no decimal place - ± 1 mm unless
one decimal place - ± 0.3 mm otherwise
two decimal places - ± 0.1 mm stated

DRN.	DSI	D & ED
TCD.		DSK27045A2
CKD.		
APPD	ecc	

D62640A2SHT1.

U701 79L15 I/P O/P REF -18V C701 100n 0VA C702 100n C775 10u
U702 79L05 D701 1N5347B C703 C704 C776
+15V -15V +10Va -10Va +10Vb -10Vb
TP101 TP102 TP103 TP201 TP202 TP203
R101 3k9 R103 18k R104 2k4 C101 10n C102 6n2 C778 100n
Q101 J175 R102 3k3 R119 2k2
U101 TL072 R105 10k L101 33m L102 39m C103 180p C104 430p C105 1n
MUTEDRIVEp12 MUTEDRIVEn12
Q102 J112 Q103 J175 R107 20k GAIN C106 2u2 R106 18k R108 100k
D101 1N4148 D102 1N4148
C109 220n R120 1M U101 TL072 C777 100n
Q104 BC183LC R121 2k2 D111 1N4148
R201 3k9 R203 18k R204 2k4 C201 10n C202 6n2 C780 100n
Q201 J175 R202 3k3 R219 2k2
U201 TL072 R205 10k L201 33m L202 39m C203 180p C204 430p C205 1n
Q202 J112 Q203 J175 R207 20k C206 2u2 R206 18k R208 100k
D201 1N4148 D202 1N4148
C209 220n R220 1M U201 TL072 C779 100n
Q204 BC183LC R221 2k2 D211 1N4148
R109 20k 0.1x U102 TL072 R110 33 R111 33k R112 20k R114 +t° R116 15 C108 10n R118 330 R117 15
D105 D106 D107 D108 VSK130 D109 D110 D103 D104
L103 RM6D/132 ch1+ ch1- CH1 OUTPUT 2 a PL 2 c PL 1 a PL 1 c PL
R209 20k 0.1x U202 TL072 R210 33 R211 33k R212 20k R214 +t° R216 15 C208 10n R218 330 R217 15
D205 D206 D207 D208 VSK130 D209 D210 D203 D204
L203 RM6D/132 ch2+ ch2- CH2 OUTPUT 5 a PL 5 c PL 4 a PL 4 c PL
R113 20k C107 100p R115 +t° R213 20k C207 100p R215 +t°
C705 C707 C709 C711 C712 C714 C716 C718 C706 C708 C710 C713 C715 C717 100n
U703 TDA1541 WSBD12A CLBD12A DABD12A XSYS12A PL1C 13c PL1A 13a PL1C 12c PL1A 12a
VDD VDD1 VDD2 WSBD CLBD DABD XSYS MODE DECOU DGND AGND C719 C720 470p
+5V D734 1N4148 D733 HUMP 1301 R718 560 MUTEDRIVEp12
OFFSET U714 TL072 R717 4x47k R716 100k X_MUTE C823 10n MUTEDRIVEn12
0VA -15V

CHANNEL 1/2

SCALE:- 0

Parts List D62641A4

THIRD ANGLE PROJECTION | ORIGINAL FRAME SIZE 400mm x 574mm | CHANGE ISS 3 17/7/89

NICAM MKII ANALOGUE BOARD

AUDIO OUTPUTS

C09/13 CIRCUIT

All dimensions in millimetres unless otherwise stated. Normal tolerances:
no decimal place – ± 1 mm unless
one decimal place – ± 0.3 mm otherwise
two decimal places – ± 0.1 mm stated

DRN. ccc TCD. CKD. APPD ccc

DESIGN & EQUIPMENT DEPARTMENT

D62640A2 SHEET 1 OF 7 SHEETS

D62640A2SHT2

+15V
-15V
+10Vc
-10Vc
0VA

ch1+
ch1-
ch4+
ch4-

LK142 A B
LK141 A B
LK163 A B
LK164 A B
LK161 A B
LK162

R141 20k
R142 12k
R143 2k
R144 12k
R145 1M
R146 20k
C141 2u2

D141 1N4148
D142 1N4148
D143 1N4148
D144 1N4148

U141 TL072
C142 100p
R147 20k
R148 +t°
C799 100n
C800 100n
R149 20k
C143 100p
R150 +t°

D145 VSK130
D146 VSK130
D147 VSK130
D148 VSK130

L141 RM6D/132
R151 15
C144 10n
R153 330
R152 15
28a PL2A
28c PL2C
CH1/4 MON OUTPUT

PL2A 22a
PL2C 22c
COMP A INPUT

R161 +t°
R162 +t°
R163 +t°
R164 +t°
D165 15V
D166 15V
D171 15V
D172 15V
D161 1N4148
D162 1N4148
D163 1N4148
D164 1N4148
D167 1N4148
D168 1N4148
D169 1N4148
D170 1N4148

U161 INA105
U162 INA105
25k 25k 25k 25k

C793 100n
C794 100n
C795 100n
C796 100n
C797 100n
C798 100n

R165 10k
R166 10k
R167 10k
R168 10k
TP161
TP162
TP163
TP164

U163 TL074
D173 1N4148
D174 1N4148

2.5V REF OFFSET
R173 250k
R174 220k
R175 220k
R169 330k
R170 39k
R171 39k
R172 4k7
R175 300
R176 300

U164 LM13700
BIAS AMP BIAS OUT BUF IN BUF OUT
C801 100n
C802 100n
C161 1u

R177 2k4
R178 15k
R179 56k
R180 56k
SET BALANCE
R181 50k
R182 51k
Q161 BC107
Q162 BCY72

TP165
R183 150k
R184 10k
R185 15k
R186 1k5
R187 1k5
R188 15k
D175 1N4148
D176 1N4148
D177 1N4148

U165 LM319
GND
R189 3k3
R190 620
D178 HUMP 1503

U712 LS05
CHAN A COMP FAIL
/railfail

CHANNEL 1 or 4

SCALE: - 0

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE
400mm x 574mm

CHANGE
ISS 3 17/7/89

NICAM MKII ANALOGUE BOARD
COMPARATOR AND MON. OUTPUT
C09/13 CIRCUIT

All dimensions in millimetres unless otherwise stated. Normal tolerances:
no decimal place – ± 1 mm unless
one decimal place – ± 0.3 mm otherwise
two decimal places – ± 0.1 mm stated

DRN. cee
TCD.
CKD.
APPD cee

DESIGN & EQUIPMENT DEPARTMENT
D62640A
SHEET 2 OF 7 SHEETS

D62640A2SHT3

U704 79L15 I/P O/P REF
U705 79L05 I/P O/P REF
D702 1N5347B
D732 1N4148
D731 HLMP 1301
-18V
+15V
-15V
+10Va
-10Va
+10Vb
-10Vb
+5V
0VA
0V
C721 100n
C722 100n
C781 10u
C723 100n
C724 100n
C782 10u
C725 C727 C729 C731 100n
C726 C728 C730 100n
C732 C734 C736 C738 100n
C733 C735 C737 100n
C824 10n
C739 C740 470p
R719 100k
R720 4x47k
R721 560
Y_MUTE
MUTEDRIVEp34
MUTEDRIVEn34
TP301
TP302
TP303
TP401
TP402
TP403
R303 18k
R304 2k4
R30i 3k9
C301 10n
C302 6n2
C784 100n
Q301 J175
R302 3k3
R319 2kz
U301 TL072
R305 10k
L301 33m
L302 39m
C303 180p
C304 430p
C305 1n
R306 18k
R308 100k
Q302 J112
Q303 J175
R307 20k
GAIN
C306 2u2
R403 18k
R404 2k4
C401 10n
C402 6n2
C786 100n
Q401 J175
R402 3k3
R419 2k2
U401 TL072
R405 10k
L401 33m
L402 39m
C403 180p
C404 430p
C405 1n
R406 18k
R408 100k
Q402 J112
Q403 J175
R407 20k
GAIN
C406 2u2
C309 220n
R320 1M
U301 TL072
Q304 BC183LC
R321 2k2
D311 1N4148
R401 3k9
C783 100n
C785 100n
C409 220n
R420 1M
U401 TL072
Q404 BC183LC
R421 2k2
D411 1N4148
U706 TDA1541
WSBD34A
CLBD34A
DABD34A
XSYS34A
PL1C 15c
PL1A 15a
PL1C 14c
PL1A 14a
VDD VDD1 VDD2
WSBD CLBD DABD XSYS MODE DECOU DGND AGND L R
D305 D306 D303 D304 1N4148
D309 20k 0.1%
R310 33
R311 33k
R312 20k
R313 20k
C307 100p
R314 +t°
R315 +t°
U302 TL072
D307 D308 D309 D310 VSK130
L303 RM6S/101
R316 15
R317 15
C308 10n
R318 330
CH3 OUTPUT
ch3+
ch3-
8a PL2A
8c PL2C
7a PL2A
7c PL2C
D405 D406 D403 D404 1N4148
R409 20k 0.1%
R410 33
R411 33k
R412 20k
R413 20k
C407 100p
R414 +t°
R415 +t°
U402 TL072
D407 D408 D409 D410 VSK130
L403 RM6S/101
R416 15
R417 15
C408 10n
R418 330
CH4 OUTPUT
ch4+
ch4-
11a PL2A
11c PL2C
10a PL2A
10c PL2C

CHANNEL 3/4

SCALE:- 0

THIRD ANGLE PROJECTION
ORIGINAL FRAME SIZE 400mm x 574mm
CHANGE 3 17/7/89

NICAM MKII ANALOGUE BOARD
AUDIO OUTPUTS
C09/13 CIRCUIT
All dimensions in millimetres unless otherwise stated. Normal tolerances
no decimal place ± 1 mm unless
one decimal place ± 0.3 mm otherwise
two decimal places ± 0.1 mm stated
DRN. CCC
T.C.D.
CK'D.
APP'D CCC
DESIGN & EQUIPMENT DEPARTMENT
D62640
SHEET 3 OF 7

D62640A2SHT4

+15V
-15V
+10Vc
-10Vc
0VA

ch2+
ch2-
LK242
LK241

R241 20k
R242 12k
R243 2k
R244 12k
R245 1M
R246 20k
C241 2v2

D241 1N4148
D242 1N4148
D243 1N4148
D244 1N4148

U241 TL072
C242 100p
R247 20k
R248 +t°
C809 100n
C810 100n
R249 20k
C243 100p
R250 +t°

D245 VSK130
D246 VSK130
D247 VSK130
D248 VSK130

L241 RM6D/132
R251 15
C244 10n
R253 330
R252 15
30a PL2A
CH2/5 MON OUTPUT
30c PL2C

PL2A 24a
COMP B INPUT
PL2C 24c

R261 +t°
D261 1N4148
D262 1N4148
R262 +t°
D263 1N4148
D264 1N4148
D265 15V
D266 15V

U261 INA105
25k 25k 25k 25k
TP261
R265 10k
C803 100n
C804 100n
C805 100n

U263 TL074
R267 10k
D273 1N4148
C807 100n
TP263

R269 330k
R270 39k
R271 39k
R272 4k7
R275 300
R276 300

LK262
2.5V REF
OFFSET
R273 250k
R274 220k
R279 220k

U264 LM13700
C811 100n
C812 100n
C261 1u
BIAS
AMP BIAS
OUT
BUF IN
BUF OUT

R277 2k4
R278 15k
SET BALANCE
R280 56k
R281 50k
R282 51k

Q261 BC107
Q262 BCY72

TP265
R283 150k
R284 10k
R285 15k
R286 1k5
R287 1k5
R288 15k
D275 1N4148
D276 1N4148
D277 1N4148

U265 LM319
R289 3k3
U712 LS05
R290 620
D278 HUMP 1503
6 c PL1C
CHAN B COMP FAIL
/railFail

ch2+
ch2-
LK263
ch5+
LK264
ch5-

R263 +t°
D267 1N4148
D268 1N4148
R264 +t°
D269 1N4148
D270 1N4148
D271 15V
D272 15V

U262 INA105
25k 25k 25k 25k
TP262
R266 10k
C806 100n
C808 100n

U263 TL074
R268 10k
D274 1N4148
TP264
LK261

CHANNEL 2 or 5

SCALE:- 0

THIRD ANGLE PROJECTION
ORIGINAL FRAME SIZE 400mm x 574mm

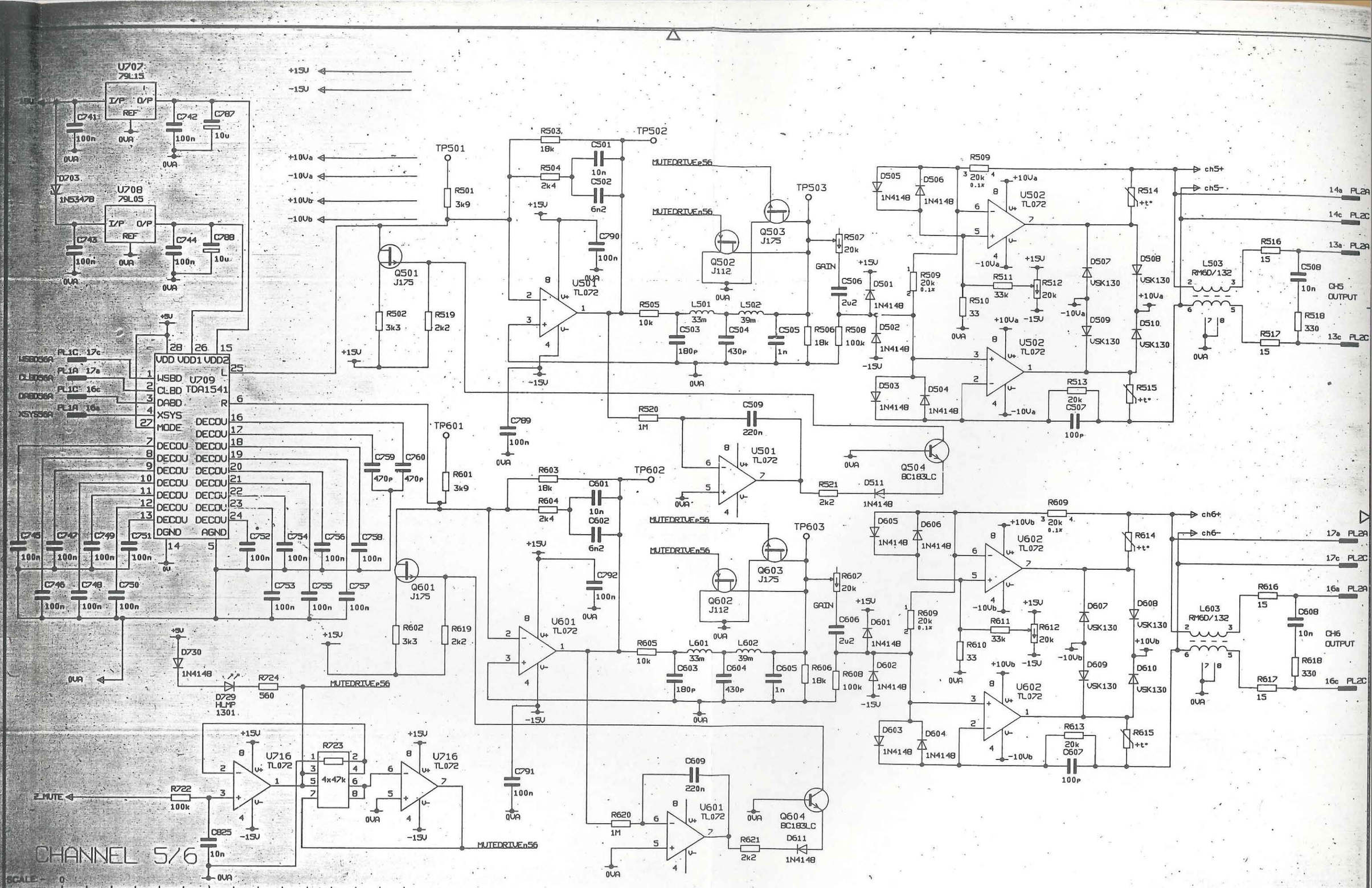
CHANGE
SS 17/7/89

NICAM MKII ANALOGUE BOARD
COMPARATOR AND MON. OUTPUT CIRCUIT
C09/13

All dimensions in millimetres unless otherwise stated. Normal tolerances:
no decimal place ± 1 mm unless
one decimal place ± 0.3 mm otherwise
two decimal places ± 0.1 mm stated

DAN. CLC
TCD.
CKD.
APPD

DESIGN & EQUIPMENT DEPARTMENT
D62640A2
SHEET 4 OF 7 SHEETS



THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE 400mm x 574mm

CHANGE	
17/7/99	

NICAM MKII ANALOGUE BOARD

AUDIO OUTPUTS

C09/13 CIRCUIT

All dimensions in millimetres unless otherwise stated. Normal tolerances:
no decimal place – ± 1 mm unless
one decimal place – ± 0.3 mm otherwise
two decimal places – ± 0.1 mm stated

DRN.	ccc
TCD.	
CKD.	
APPD	ccc

DESIGN & EQUIPMENT DEPARTMENT

D62640A2

SHEET 5 OF 7 SHEETS

D62640A2SHT6

+15V
-15V
+10Vc
-10Vc
0VA

ch3+
ch3-
LK341
LK342
ch6+
ch6-
LK363
LK364

PL2A 26a
COMP C INPUT
PL2C 26c

R361 +t°
R362 +t°
R363 +t°
R364 +t°

D361 1N4148
D362 1N4148
D363 1N4148
D364 1N4148
D365 15V
D366 15V
D367 1N4148
D368 1N4148
D369 1N4148
D370 1N4148
D371 15V
D372 15V

U361 INA105
U362 INA105
25k

C813 100n
C814 100n
C815 100n
C816 100n
C817 100n
C818 100n

R365 10k
R366 10k
R367 10k
R368 10k

U363 TL074
D373 1N4148
D374 1N4148

TP361
TP362
TP363
TP364

LK361
LK362

2.5V REF
OFFSET
R373 250k
R374 220k
R379 220k

R369 330k
R370 39k
R371 39k
R372 4k7
R375 300
R376 300

U364 LM13700
BIAS
AMP BIAS
OUT
BUF IN
BUF OUT
C821 100n
C822 100n

C361 1u
Q361 BC107
Q362 BCY72
SET BALANCE
R380 56k
R381 50k
R382 51k

R377 2k4
R378 15k
R383 150k
R384 10k
R385 15k
R386 1k5
R387 1k5
R388 15k

U365 LM319
R389 3k3
R390 620
D378 HLMP 1503
U712 LS05
D375 1N4148
D376 1N4148
D377 1N4148
/railfail

CHAN C COMP FAIL

D341 1N4148
D342 1N4148
D343 1N4148
D344 1N4148

R341 20k
R342 12k
R343 2k
R344 12k
R345 1M
R346 20k
C341 2u2

U341 TL072
C342 100p
R347 20k
R348 +t°
C819 100n
C820 100n
D345 VSK130
D346 VSK130
D347 VSK130
D348 VSK130
R349 20k
C343 100p
R350 +t°

L341 RM60V/132
R351 15
R352 15
C344 10n
R353 330
32a PL2A
32c PL2C
CH3/6 MON OUTPUT

CHANNEL 3 or 6

SCALE:- 0

THIRD ANGLE PROJECTION
ORIGINAL FRAME SIZE 400mm x 574mm

ISS 3 CHANGE 17/7/89

NICAM MKII ANALOGUE BOARD
COMPARATOR AND MON. OUTPUT CIRCUIT
C09/13

All dimensions in millimetres unless otherwise stated. General tolerances: no decimal place ± 1 mm unless; one decimal place ± 0.3 mm otherwise; two decimal places ± 0.1 mm stated

DRN. ccc
TCD.
CKD.
APPD ccc

DESIGN & EQUIPMENT DEPARTMENT
D62640A2
SHEET 6 OF 7 SHEETS

D62640A2SHT7

D726 1N4006
H10
U710 7815
+18V
I/P O/P
REF
+15V
D725 1N4006
C761 100n
C762 100n
C763 33u
0VA

+15V
D707 1N4148
R701 100
+10Va
D708 1N5347B
C769 100n
D709 1N5347B
C770 100n
-10Va
R702 100
D710 1N4148
-15V
0VA

+15V
D711 1N4148
R703 100
+10Vb
D712 1N5347B
C771 100n
D713 1N5347B
C772 100n
-10Vb
R704 100
D714 1N4148
-15V
0VA

+15V
D715 1N4148
R705 100
+10Vc
D716 1N5347B
C773 100n
D717 1N5347B
C774 100n
-10Vc
R706 100
D718 1N4148
-15V
0VA

+15V
D719 12V
D720 1N4148
R707 330
0VA
+5V
R708 47k
D721 1N4148
R709 47k
0VA
+5V
R710 10k
Q701 BC107
0VA

+5V
R711 1k
D723 1N4148
D722 13V
-15V
D724 1N4148
R712 33k
0VA
+5V
R713 3k3
/railfail
20c PL2C
Q702 BC107
0VA

PL1A 1 a
CHASSIS
0V

IMPLICIT VCC +5V
PL1A 29a
PL1C 29c
PL1A 30a
PL1C 30c

PL1A 31a
PL1C 31c
PL1A 32a
PL1C 32c
0V

D728 1N4006
H11
U711 7915
-18V
I/P O/P
REF
-15V
D727 1N4006
C764 100n
C765 100n
C766 33u
0VA

PL1A 2 a
PL1C 2 c
+18V
C767 10u
0VA
C768 10u
PL1A 3 a
PL1C 3 c
-18V

+15V
R715 3k3
2.5V_REF
U713 TL431 CLP
0VA

PL1A 4 a
PL1C 4 c
PL1A 5 a
PL1C 5 c
0VA
R714 100
0V
IMPLICIT GND

+5V
R725 4k7
R726 4k7
R727 4k7

U717 EP600 MUTE PAL
CLK1 IN
IN I/O
I/O I/O
I/O I/O
I/O I/O
I/O I/O
I/O I/O
I/O I/O
I/O IN
IN CLK2
0V

8192kHz PL2A 19a
/2048_LOCK PL1C 1 c
X_MUTE
Y_MUTE
Z_MUTE
/MUTE_Z PL1A 27a
/MUTE_Y PL1C 25c
/MUTE_X PL1A 25a
/CPU_RST PL2C 19c

+5V
U712 LS05
U712 LS05
U712 LS05

PROBE EARTH
PROBE EARTH
PROBE EARTH
PROBE EARTH
PROBE EARTH
0VA

20a PL2A
3 a PL2A
3 c PL2C
6 a PL2A
6 c PL2C
9 a PL2A
9 c PL2C
12a PL2A
12c PL2C
15a PL2A
15c PL2C
18a PL2A
18c PL2C
21a PL2A
21c PL2C
23a PL2A
23c PL2C
25a PL2A
25c PL2C
27a PL2A
27c PL2C
29a PL2A
29c PL2C
31a PL2A
31c PL2C
0VA

SCALE: – 0

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE 400mm x 574mm

BBC DS/A2/1

ISS 3 CHANGE 17/7/89

NICAM MKII ANALOGUE BOARD

POWER SUPPLIES

C09/13 CIRCUIT

All dimensions in millimetres unless otherwise stated. Normal tolerances: no decimal place ± 1 mm unless; one decimal place ± 0.3 mm otherwise; two decimal places ± 0.1 mm stated

DRN. CCC
TCD.
CKD.
MTD CCC

DESIGN & EQUIPMENT DEPARTMENT

D62640A2 SHEET 7 OF 7 SH

ISS.	CHANGE
1	1/2/89

ITEM No.	No. OFF		DESCRIPTION	C'CT REF.	BBC REF. OR DRG. No.
			DRAWING LIST		
			CIRCUIT D62640A2		
			PARTS LIST D62641A4		
			ASSY & WIRING D62642A2		
			DETAIL D62643A4		
			PBd. PHOTO PLOT MASTERS D62644A2		
			PBd. DRILLING D62645A2		
			ENHANCED COPY COMP. LOC. DSK 27171A2.		
			FURTHER INFORMATION REQUIRED FOR MANUFACTURE		
			EA10140 - UNIT WIRING INFO		
			EA10484 - UNIT ASSY INFO		
			UNIT SPEC ED/C09/13		
			CUSTOMISING SHEET VELO MASTER VM621A4		
			PROM DEFINITION SHEET F1660A		
1	1	*	PRINTED BOARD MANUFACTURED TO :-		-0627581
			AND TO SPEC ED/PB/C09/13/PTH		D62644A2, D62645A2 DSK 27171A2.
2	1	*+	PBd HANDLE, PLASTIC, WHITE.		S53922 - 0388150
			ENGRAVED BY CONTRACTOR TO :-		D62643A4
3	1	*	6U SCREEN PLATE (UNCODED) x 280 mm		-0629483
4					
5	2	*	PLUG, FIXED 90° PBd MOUNTING, 64 POLE, G06		S25090 - 0610062
			(2) PL1, PL2		
6	33	*	TEST POINT, VERO 1.0 Ø		S28650 - 039229X
			(33) TP101 - TP103, TP161 - TP165, TP201 - TP 203, TP261 - TP265, TP301 - TP303, TP361 - TP365, TP401 - TP403, TP501 - TP503, TP601 - TP603.		
7	1	*	I.C. HOLDER, LOW PROFILE, 14 PIN x 7.6mm (U712)		S27860 - 0445461
8	3	*	I.C. HOLDER, LOW PROFILE, 28 PIN x 0.6"		S27860 - 0445043
			U703, U706, U709		
9	1	*	I.C. HOLDER, LOW PROFILE, 0.3" x 24 PIN (FARNELL 170-718)		-0619218
			(U717)		

BBC

C09/13
6 CHANNEL NICAM II D.A.C.
PARTS LIST

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D62641A4
SHT 1 OF 16

CHANGE	ISS.
1/2/87	1
12/5/89	2

ITEM No.	No. OFF		DESCRIPTION	C'CT REF	BBC REF. OR DRG. No.
			RESISTORS		
10	18	*	15Ω, ±2%, 0·4W, METAL FILM (18) R116, R117, R151, R152, R216, R217, R251, R252, R316, R317, R351, R352, R416, R417, R516, R517 R616, R617.		S26877-0227760
11	6	*	33Ω, ±2%, 0·4W, METAL FILM (6) R110, R210, R310, R410, R510, R610		S26877-0099441
12	7	*	100Ω, ±2%, 0·4W, METAL FILM (7) R701, R702, R703, R704, R705, R706, R714		S26877-0099007
13	6	*	300Ω, ±2%, 0·4W, METAL FILM (6) R175, R176, R275, R276, R375, R376,		S26877-0099338
14	10	*	330Ω, ±2%, 0·4W, METAL FILM (10) R118, R153, R218, R253, R318, R353, R418, R518, R618, R707		S26877-0099031
15	3	*	620Ω, ±2%, 0·4W, METAL FILM (3) R190, R290, R390		S26877-0099058
16	1	*	1KΩ, ±2%, 0·4W, METAL FILM (1) R711		S26877-0099082
17	6	*	1·5KΩ, ±2%, 0·4W, METAL FILM (6) R186, R187, R286, R287, R386, R387		S26877-0099110
18	9	*	2·4KΩ, ±2%, 0·4W, METAL FILM (9) R104, R177, R204, R277, R304, R377, R404, R504, R604		S26877-0099153
19	11	*	3·3KΩ, ±2%, 0·4W, METAL FILM (11) R189, R289, R389, R713, R715 R102. R202. R302. R402, R502, R602		S26877-0099161
20	6	*	3·9KΩ, ±2%, 0·4W, METAL FILM (6) R101, R201, R301, R401, R501, R601		S26877-009917X
21	6	*	4·7KΩ, ±2%, 0·4W, METAL FILM (6) R172, R272, R372 R725, R726, R727		S26877-0099425
22	22	*	10KΩ, ±2%, 0·4W, METAL FILM (22) R105, R165, R166, R167, R168, R184, R205, R265, R266 R267 R268, R284, R305, R365, R366, R367, R368, R384, R405, R505, R605, R710.		S26877-0099224
23	6	*	12KΩ, ±2%, 0·4W, METAL FILM (6) R142, R144, R242, R244, R342, R344		S26877-0228043

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ISS	CHANGE
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ITEM No.	No. OFF		DESCRIPTION	C'CT REF.	BBC REF. OR DRG. No.
24	9	*	15KΩ, ± 2%, 0·4W, METAL FILM		S26877-0099370
			(9) R178, R185, R188, R278, R285, R288, R378, R385, R388		
25	12	*	18KΩ, ± 2%, 0·4W, METAL FILM		S26877-0099389
			(12) R103, R106, R203, R206, R303, R306, R403, R406, R503, R506, R603, R606		
26	18	*	20KΩ, ± 2%, 0·4W, METAL FILM		S26877-022806X
			(18) R113, R141, R146, R147, R149, R213, R241, R246, R247, R249, R313, R341, R346, R347, R349, R413, R513, R613.		
27	7	*	33KΩ, ± 2%, 0·4W, METAL FILM		S26877-0099259
			(7) R111, R211, R311, R411, R511, R611, R712		
28	6	*	39KΩ, ± 2%, 0·4W, METAL FILM		S26877-0099512
			(6) R170, R171, R270, R271, R370, R371		
29	2	*	47KΩ, ± 2%, 0·4W, METAL FILM		S26877-0099267
			(2) R708, R709		
30	3	*	51KΩ, ± 2%, 0·4W, METAL FILM		S26877-0228122
			(3) R182, R282, R382		
31	3	*	56KΩ, ± 2%, 0·4W, METAL FILM		S26877-0228130
			(3) R180, R280, R380		
32	9	*	100KΩ, ± 2%, 0·4W, METAL FILM		S26877-0228181
			(9) R108, R208, R308, R408, R508, R608 R716, R719, R720		
33	3	*	150KΩ, ± 2%, 0·4W, METAL FILM		S26877-0228228
			(3) R183, R283, R383		
34	3	*	330KΩ, ± 2%, 0·4W, METAL FILM		S26877-0099417
			(3) R169, R269, R369		
35	6	*	220K, ± 2%, 0·4W, METAL FILM		S26877-0228244
			(6) R174, R274, R374, R179, R279 R379		
36	9	*	1MΩ, ± 2%, 0·4W, METAL FILM		S26877-0099283
			(9) R145, R245, R345, R120, R220, R320, R420 R520, R620		
37					
38	3	*	560Ω, ± 2%, 0·4W, METAL FILM		S26877-0227953
			(3) R718, R721, R724		
39	12		2·2KΩ, ± 2%, 0·4W, METAL FILM		S26877-0099145
			(12) R119, R219, R319, R419, R519, R619 R121, R221, R321, R421, R521, R621		

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CHANGE	ISS.
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12/5/89	2

ITEM No.	No. OFF		DESCRIPTION	C'CT REF.	BBC REF. OR DRG. No.
40	3	*	2KΩ, VARIABLE, TOP ADJUST		S27243 - 0306003
			(3) R143, R243, R343		
41					
42	12	*	20KΩ, VARIABLE, TOP ADJUST		S27243 - 0365177
			(12) R107, R112, , R207, R212, R307, R312 , R407, R412, R507, R512, R607, R612		
43	3	*	50KΩ, VARIABLE, TOP ADJUST		S27243 - 0365125
			(3) R181, R281, R381		
44	3	*	250KΩ, VARIABLE, TOP ADJUST		S27243 - 0305921
			(3) R173, R273, R373		
45	6	*	20KΩx10 NETWORK, T912-20K-100-10		- 0627991
			(6) R109, R209, R309, R409, R509, R609		
46	3	*	47KΩx4, 8 PIN NETWORK, SIL		S27076 - 0428247
			(3) R717, R720, R723		
			CAPACITORS		
50	6	*	220nF, 63V, POLYESTER		S21035 - 0466188
			(6) C109, C209, C309, C409, C509, C609		
51	64	*	100nF, 50V, MULTILAYER		S20648 - 0204648
			(64) C701, C702, C703, C704, C721, C722, C723, C724, C741, C742, C743 , C744, C761, C762, C764, C765, C769, C770, C771, C772, C773, C774, C777, C778, C779, C780, C783, C784, C785, C786, C789, C790, C791, C792, C793, C794, C795, C796, C797, C798, C799, C800, C801, C802, C803, C804, C805, C806, C807, C808, C809, C810, C811, C812, C813, C814, C815, C816, C817, C818, C819, C820, C821, C822		
52	2	*	33μF, 16V, ELECTROLYTIC, VERTICAL		S20832 - 0612887
			(2) C763, C766		
53	8	*	10μF, 50V, ELECTROLYTIC, VERTICAL		S20835 - 0616981
			(8) C767, C768, C775, C776, C781, C782, C787, C788		
54	12	*	100pF, 63V, RECTANGULAR, POLYSTYRENE		S21005 - 0449968
			(12) C107, C142, C143, C207, C242, C243, C307, C342, C343, C407, C507, C607		

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ITEM No.	No. OFF		DESCRIPTION	C'CT REF	BBC REF. OR DRG. No.
55	6	*	180pF, 63V, RECTANGULAR, POLYSTYRENE		S21005-0450025
			(6) C103, C203, C303, C403, C503, C603		
56	6	*	430pF, 63V, RECTANGULAR, POLYSTYRENE		S21005-0450112
			(6) C104, C204, C304, C404, C504, C604		
57	6	*	470pF, 63V, RECTANGULAR, POLYSTYRENE		S21005-0450120
			(6) C719, C720, C739, C740, C759, C760		
58	6	*	1nF, 63V, RECTANGULAR, POLYSTYRENE		S21005-045020X
			(6) C105, C205, C305, C405, C505, C605		
59	6	*	6·2nF, 63V, RECTANGULAR, POLYSTYRENE		S21005-0450399
			(6) C102, C202, C302, C402, C502, C602		
60	6	*	10nF, 63V, RECTANGULAR, POLYSTYRENE		S21006-0606140
			(6) C101, C201, C301, C401, C501, C601		
61	9	*	10nF, 100V, RECTANGULAR, POLYESTER		S21035-0466208
			(9) C108, C144, C208, C244, C308, C344, C408, C508, C608		
62	42	*	100nF, 100V, MINIATURE, LAYER, RS.114-402		-062759X
			(42) C705, C706, C707, C708, C709, C710, C711, C712, C713, C714, C715, C716, C717, C718, C725, C726, C727, C728, C729, C730, C731, C732, C733, C734, C735, C736, C737, C738, C745, C746, C747, C748, C749, C750, C751, C752, C753, C754, C755, C756, C757, C758		
63	3	*	1µF, 100V, MINIATURE LAYER, R.S.114-430		-0627601
			(3) C161, C261, C361		
64	9	*	2·2µF, 100V, MINIATURE, LAYER, R.S.114-446		-062761X
			(9) C106, C141, C206, C241, C306, C341, C406, C506, C606.		
65	3	*	10nF, 100V, MULTILAYER		-0099669
			(3) C823, C824, C825		
66					
67					
68					
69					

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ISS.	CHANGE.
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ITEM No.	No. OFF		DESCRIPTION	C'CT REF.	BBC REF. OR DRG. No.
			THERMISTORS		
70	18	*	P.T.C. 110mA, R.S.151-300		-0629464
			(18) R114, R115, R148, R150, R214, R215, R248, R250, R314, R315, R348, R350, R414, R415, R514, R515, R614, R615		
71	12	*	P.T.C. - RAYCHEM 21091		-0629472
			(12) R161, R162, R163, R164, R261, R262, R263, R264, R361, R362, R363, R364.		
			(SUITABLE ALTERNATIVE MID WEST Q50)		
72					
73					
74					
			DIODES		
75	36	*	VSK130, SCHOTTKY		-0530215
			(36) D107, D108, D109, D110, D145, D146, D147, D148, D207, D208, D209, D210, D245, D246, D247, D248, D307, D308, D309, D310, D345, D346, D347, D348, D407, D408, D409, D410, D507, D508, D509, D510, D607, D608, D609, D610.		
76	1	*	VZ12M4		-0147282
			(1) D719		
77	1	*	VZ13M4		-0147329
			(1) D722		
78	12	*	VZ15M4		-0147345
			(12) D165, D166, D171, D172, D265, D266, D271, D272, D365, D366, D371, D372		
79	106	*	1N4148		-0102612
			(106) D101, D102, D103, D104, D105, D106, D141, D142, D143, D144, D161, D162, D163, D164, D167, D168, D169, D170, D173, D174, D175, D176, D177, D201, D202, D203, D204, D205, D206, D241, D242, D243, D244, D261, D262, D263, D264, D267, D268, D269, D270, D273, D274, D275, D276, D277, D301, D302, D303, D304, D305, D306, D341, D342, D343, D344, D361, D362, D363, D364, D367, D368, D369, D370, D373, D374, D375, D376, D377, D401, D402, D403, D404, D405, D406, D501, D502, D503,		

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PARTS LIST

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ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
			D504, D505, D506, D601, D602, D603,		
			D604, D605, D606, D707, D710, D711,		
			D714, D715, D718, D720, D721, D723,		
			D724, D730, D732, D734		
			D111, D211, D311, D411, D511, D611		
80	3	*	LED, GREEN, MINIATURE, HLMP1503		-0178878
			(3) D178, D278, D378.		
81	9	*	1N5347B, ZENER		-0530223
			(9) D701, D702, D703, D708, D709, D712, D713, D716, D717.		
82	3	*	LED, RED, MINIATURE, HLMP1301		-017886X
			(3) D729, D731, D733		
83	4	*	1N4006		
			(4) D725, D726, D727, D728		-0102592
84					
			INDUCTORS		
85	6	*	39mH, TOKO 181LY-393		-0627636
			(6) L102, L202, L302, L402, L502, L602		
86	6	*	33mH, TOKO 181LY-333		-0614928
			(6) L101, L201, L301, L401, L501, L601		
87	9	*	BBC TYPE RM65/101		-0627628
			(9) L103, L141, L203, L241, L303, L341, L403, L503, L603.		
88					
89					
			TRANSISTORS		
70	5	*	BC107		-0112266
			(5) Q701, Q702, Q161, Q261, Q361		
71	3	*	BCY72		-011280X
			(3) Q162, Q262, Q362		
92	12	*	J175 P-CHANNEL FET		-0195702
			(12) Q101, Q201, Q301, Q401, Q501, Q601 Q103, Q203, Q303, Q403, Q503, Q603		
93					
93	6	*	J112-N CHANNEL FET		-0195729
			(6) Q102, Q202, Q302, Q402, Q502, Q602		

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CHANGE	ISS.
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ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
94	6	*	BC183LC		-0190730
			(6) Q104, Q204, Q304, Q404, Q504, Q604		
			I.C.'s		
			CAUTION, SSD's. TO AVOID DAMAGE FROM STATIC CHARGES GREAT CARE SHOULD BE TAKEN WHEN HANDLING THESE DEVICES.		
95	18	*	TL072CP		-0194800
			(18) U102, U141, U202, U241, U302, U341, U402, U502, U602, U714, U715, U716 U101, U201, U301, U401, U501, U601		
96	3	*	TL074CN		-0194819
			(3) U163, U263, U363		
97	3	*	LM319N		-0187213
			(3) U165, U265, U365		
98	1	*	LIC7915T -REGULATOR -15V.		-0192613
			(1) U711		
99	3	*	LM79L15ACZ - REGULATOR -15V		-0198850
			(3) U701, U704, U707		
100					
101	3	*	LM79L05ACZ, REGULATOR -5V		-0506597
			(3) U702, U705, U708		
102	1	*	LIC7815T, REGULATOR +15V		-0174931
			(1) U710		
103	6	*	INA105KP		-0530231
			(6) U161, U162, U261, U262, U361, U362		
104	3	*	LM13700N		-053024X
			(3) U164, U264, U364		
105	1	*	SSD/DIC74LS05N		-0171684
			(1) U712		
106	3	*	TDA1541A/N2		-0530258
			(3) U703, U706, U709		
107	1	*	EP600DC		-053009X
			(1) U717 - PROGRAMMED TO F1060A		-0700026X
108	1	*	TL431 CLP		-0504785
			(1) U713		

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ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
109					
110	2	*+	HEADER, 36 WAY, BERG STICK 75160-101-36		-0457322
111	3	△	LINK, 2 PIN, MADE BY CONTRACTOR FROM ITEM 110 (3) LK162, LK262, LK362		
112	15	□	LINK, 3 PIN, MADE BY CONTRACTOR FROM ITEM110 (15) LK141, LK142, LK161, LK163, LK164, LK241, LK242, LK261, LK263, LK264, LK341, LK342, LK361, LK363, LK364		
113	18	*	JUMPER, MINIJUMP - BERG 65474 (18) LK162, LK262, LK362, LK141, LK142, LK161, LK163, LK164, LK241, LK242, LK261, LK263, LK264, LK341, LK342, LK361, LK363, LK364.		-0464325
114					
115	2	*	HEATSINK, TO-220		-0446619
116					
117	A/R	*+	B.T.C. Ø1·8mm		
118	A/R	*+	SLEEVING, SYMEL, BLACK, 0·5mm BORE.		-0254265
119					
120	1	*	SSD BAG ANTI STATIC, 10" x 12"		-0613387

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ISS.	1
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ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	B B C REF. OR DRG. No.
			FIXINGS		FOR FIXING ITEMS
130	9		SCREW, CSK HD, M2·5 x 8 LG, M.S. Zn PL		1, 3 & 139
131	4		SCREW, PAN HD, M2·5 x 10 LG, M.S. Zn PL		1 & 5
132	2		SCREW, PAN HD, M3 x 8 LG, M.S. Zn PL		98, 102, 115
133					
134	15		WASHER, PLAIN, M2·5		
135	2		WASHER, PLAIN, M3		
136					
137	13		NUT, FULL, HEX, M2·5		
138	2		NUT, FULL, HEX, M3		
139	9	*+	SPACER, TUFNOL, TAPPED M2·5 x 3mm LG.		-0325675
140	1		CARTON CARDBOARD TO SPEC ED/C09/13		

Notes

*	Denotes items supplied to the contractor on embodiment loan
*+	Denotes items supplied to the contractor on embodiment loan, requiring special costing or supply action by B.B.C.
θ*	Denotes components supplied and fitted by B.B.C. on test.
θ+	Denotes coded plug in units supplied and fitted by B.B.C. on test.
Ø	Denotes items supplied and fitted by B.B.C. on installation.
Δ	DENOTES 18 OF ITEM 111 CAN BE MADE FROM 1 OFF ITEM 110
□	DENOTES 12 OF ITEM 112 CAN BE MADE FROM 1 OFF ITEM 110

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PLA4

CIRCUIT REFERENCE.....

PL1	5	R101	20	R175	13		
PL2	5	R102	41	R176	13		
		R103	25	R177	18	R261	71
		R104	18	R178	24	R262	71
TP101	6	R105	22	R179	35	R263	71
TP102	6	R106	25	R180	31	R264	71
TP103	6	R107	42	R181	43	R265	22
		R108	32	R182	30	R266	22
TP161	6	R109	45	R183	33	R267	22
TP162	6	R110	11	R184	22	R268	22
TP163	6	R111	27	R185	24	R269	34
TP164	6	R112	42	R186	17	R270	28
TP165	6	R113	26	R187	17	R271	28
		R114	70	R188	24	R272	21
TP201	6	R115	70	R189	19	R273	44
TP202	6	R116	10	R190	15	R274	35
TP203	6	R117	10			R275	13
		R118	14	R201	20	R276	13
TP261	6	R119	39	R202	41	R277	18
TP262	6	R120	36	R203	25	R278	24
TP263	6	R120	39	R204	18	R279	35
TP264	6	R141	26	R205	22	R280	31
TP265	6	R142	23	R206	25	R281	43
		R143	40	R207	42	R282	30
TP301	6	R144	23	R208	32	R283	33
TP302	6	R145	26	R209	45	R284	22
TP303	6	R146	26	R210	11	R285	24
TP361	6	R147	26	R211	27	R286	17
TP362	6	R148	70	R212	42	R287	
TP363	6	R149	26	R213	26	R288	
TP364	6	R150	70	R214	70	R289	
TP365	6	R151	10	R215	70	R290	
TP401	6	R152	10	R216			
TP402	6	R153	14	R217		R301	
TP403	6			R218	14	R302	
		R161	71	R219	39	R303	
		R162	71	R220	36	R304	
TP501	6	R163	71	R221	39	R305	
TP502	6	R164	71	R241	26	R306	
TP503	6	R165	22	R242	23	R307	
		R166	22	R243	40	R308	
TP601	6	R167	22	R244	23	R309	
TP602	6	R168	22	R245	36	R310	
TP603	6	R169	34	R246	26	R311	
		R170	28	R247	26	R312	
		R171	28	R248	70	R313	
		R172	21	R249	26	R314	
		R173	44	R250	70	R315	
		R174	35	R251	10	R316	
				R252	10		
				R253	14		

ORIGINAL FRAME SIZE 190mm x 277mm

THIRD ANGLE PROJECTION

All dimensions in millimetres unless otherwise stated:
Normal tolerances:
no decimal place – ± 1 mm unless
one decimal place – ± 0.3 mm otherwise
two decimal places – ± 0.1 mm stated

SCALE: – 0

ISS	CHANGE
1	1/2/89
2	12/5/89

BBC

DS/A4

C09/13
PARTS LIST

DRN.	DSI	D&ED
TCD.		D62641A4
CKD.		
APPD.	CC	SHT 11 OF 14

R297

CIRCUIT REFERENCES (Continued).....

R317	10	R415	70	R712	27	C308	61
R318	14	R416	10	R713	19	C309	50
R319	39	R417	10	R714	12		
R320	36	R418	14	R715	19	C341	64
R321	39	R419	39	R716	32	C342	54
R341	26	R420	36	R717	46	C343	54
R342	23	R421	39	R718	38	C344	61
R343	40	R501	20	R719	32		
R344	23	R502	41	R720	46	C361	63
R345	36	R503	25	R721	38		
R346	26	R504	18	R722	32	C401	60
R347	26	R505	22	R723	46	C402	59
R348	70	R506	25	R724	38	C403	55
R349	26	R507	42	R725	21	C404	56
R350	70	R508	32	R726	21	C405	58
R352	10	R509	45	R727	21	C406	64
R353	14	R510	11			C407	54
		R511	27	C101	60	C408	61
R361	71	R512	42	C102	59	C409	50
R362	71	R513	26	C103	55		
R363	71	R514	70	C104	56	C501	60
R364	71	R515	70	C105	58	C502	59
R369	34	R516	10	C106	64	C503	55
R370	28	R517	10	C107	54	C504	56
R371	28	R518	14	C108	61	C505	58
R372	21	R519	39	C109	50	C506	64
R373	44	R520	36			C507	54
R374	35	R521	39	C141	64	C508	61
R375	13	R601	20	C142	54	C509	50
R376	13	R602	41	C143	54		
R377	13	R603	25	C144	61	C601	60
R378	24	R604	18	C161	63	C602	59
R379	35	R605	22			C603	55
R380	31	R606	25	C201	60	C604	56
R381	43	R607	42	C202	59	C605	58
R382	30	R608	32	C203	55	C606	64
R383	33	R609	45	C204	56	C607	54
R384	22	R610	11	C205	58	C608	61
R385	24	R611	27	C206	64	C609	50
R386	17	R612	42	C207	54		
R387	17	R613	26	C208	61	C701	51
R388	24	R614	70	C209	50	C702	51
R389	19	R615	70			C703	51
R390	15	R616	10	C241	64	C704	51
		R617	10	C242	54	C705	62
R401	20	R618	14	C243	54	C706	62
R402	41	R619	39	C244	61	C707	62
R403	25	R620	36	C261	63	C708	62
R404	18	R621	39	C301	60	C709	62
R405	22	R701	12	C302	59	C710	62
R406	25	R702	12	C303	55	C711	62
R407	42	R703	12	C304	56	C712	62
R408	32	R704	12	C305	58	C713	62
R409	45	R705	12	C306	64	C714	62
R410	11	R706	12	C307	54	C715	19
R411	27	R707	14			C716	62
R412	42	R708	29				
R413	26	R709	29				
R414	70	R710	22				
		R711	16				

All dimensions in millimetres unless otherwise stated:
Normal tolerances:
no decimal place - ± 1 mm unless
one decimal place - ± 0.3 mm otherwise
two decimal places - ± 0.1 mm stated

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE
190mm x 277mm

ISS	CHANGE
1	1/2/89
2	12/5/89

BBC

DS/A4

C09/13
PARTS LIST

DRN.	DJI	D&ED
TCD.		D62641A4
CKD.		
APPD.	CCC	SHT 12 OF 76

R297

CIRCUIT REFERENCES (Continued).....

C717	62	C762	51	C807	51	Q501	92
C718	62	C763	52	C808	51	Q502	93
C719	57	C764	51	C809	51	Q503	92
C720	57	C765	51	C810	51	Q504	94
C721	51	C766	52	C811	51	Q601	92
C722	51	C767	53	C812	51	Q602	93
C723	51	C768	53	C813	51	Q603	92
C724	51	C769	51	C814	51	Q604	94
C725	62	C770	51	C815	51	Q701	90
C726	62	C771	51	C816	51	Q702	90
C727	62	C772	51	C817	51		
C728	62	C773	51	C818	51	L101	86
C729	62	C774	51	C819	51	L102	85
C730	62	C775	53	C820	51	L103	87
C731	62	C776	53	C821	51		
C732	62	C777	51	C822	51	L141	87
C733	62	C778	51	C823	65		
C734	62	C779	51	C824	65	L201	86
C735	62	C780	51	C825	65	L202	85
C736	62	C781	53			L203	87
C737	62	C782	53	Q101	92		
C738	62	C783	51	Q102	93	L241	87
C739	57	C784	51	Q103	92		
C740	57	C785	51	Q104	94	L301	86
C741	51	C786	51	Q161	90	L302	85
C742	51	C787	53	Q162	91	L303	87
C743	51	C788	53				
C744	51	C789	51	Q201	92	L341	87
C745	62	C790	51	Q202	93		
C746	62	C791	51	Q203	92	L401	86
C747	62	C792	51	Q204	94	L402	85
C748	62	C793	51	Q261	90	L403	87
C749	62	C794	51	Q262	91		
C750	62	C795	51			L501	86
C751	62	C796	51	Q301	92	L502	85
C752	62	C797	51	Q302	93	L503	87
C753	62	C798	51	Q303	92		
C754	62	C799	51	Q304	94	L601	86
C755	62	C800	51	Q361	90	L602	85
C756	62	C801	51	Q362	91	L603	87
C757	62	C802	51				
C758	62	C803	51				
C759	57	C804	51	Q401	92		
C760	57	C805	51	Q402	93		
C761	51	C806	51	Q403	92		
				Q404	94		

ORIGINAL FRAME SIZE 190mm x 277mm

THIRD ANGLE PROJECTION

All dimensions in millimetres unless otherwise stated:
Normal tolerances:
no decimal place – ± 1 mm unless
one decimal place – ± 0.3 mm otherwise
two decimal places – ± 0.1 mm stated

SCALE: – 0

ISS	CHANGE
1	1/2/89
2	12/5/89

BBC

DS/A4

C09/13
PARTS LIST

DRN.	DSI	D&ED
TCD.		D62641A4
CKD.		
APPD.	CCC	SHT 13 OF 16

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CIRCUIT REFERENCES (CONTINUED).....

U101	95	U706	106	D173	79	D301	79
U102	95	U707	99	D174	79	D302	79
		U708	101	D175	79	D303	79
U141	95	U709	106	D176	79	D304	79
U161	103	U710	102	D177	79	D305	79
U162	103	U711	98	D178	80	D306	79
U163	96	U712	105			D307	75
U164	104	U713	108	D201	79	D308	75
U165	95	U714	95	D202	79	D309	75
		U715	95	D203	79	D310	75
U201	95	U716	95	D204	79	D311	79
U202	95	U717	107	D205	79		
				D206	79	D341	79
U241	95			D207	75	D342	79
		D101	79	D208	75	D343	79
U261	103	D102	79	D209	75	D344	79
U262	103	D103	79	D210	75	D345	75
U263	96	D104	79	D211	79	D346	75
U264	104	D105	79	D241	79	D347	75
U265	97	D106	79	D242	79	D348	75
		D107	75	D243	79		
U301	95	D108	75	D244	79	D361	79
U302	95	D109	75	D245	75	D362	79
		D110	75	D246	75	D363	79
U341	95	D111	79	D247	75	D364	79
		D141	79	D248	75	D365	78
U361	103	D142	79			D366	78
U362	103	D143	79	D261	79	D367	79
U363	96	D144	79	D262	79	D368	79
U364	104	D145	75	D263	79	D369	79
U365	97	D146	75	D264	79	D370	79
		D147	75	D265	78	D371	78
U401	95	D148	75	D266	78	D372	78
U402	95			D267	79	D373	79
		D161	79	D268	79	D374	79
U501	95	D162	79	D269	79	D375	79
U502	95	D163	79	D270	79	D376	79
		D164	79	D271	78	D377	79
U601	95	D165	78	D272	78	D378	80
U602	95	D166	78	D273	79		
		D167	79	D274	79	D401	79
U701	99	D168	79	D275	79	D402	79
U702	101	D169	79	D276	79	D403	79
						D404	79
U703	106	D170	79	D277	79	D405	79
						D406	79
U704	99	D171	78	D278	80	D407	75
U705	101	D172	78			D408	75
						D409	75
						D410	75
						D411	79

ORIGINAL FRAME SIZE 190mm x 277mm

THIRD ANGLE PROJECTION

All dimensions in millimetres unless otherwise stated:
Normal tolerances:
no decimal place – ± 1 mm unless
one decimal place – ± 0.3 mm otherwise
two decimal places – ± 0.1 mm stated

SCALE: – 0

ISS	CHANGE
1	1/2/89
2	12/5/89

BBC

DS/A4

C09/13
PARTS LIST

DRN.	DSI
TCD.	
CKD.	
APPD.	CC

D & ED

D62641A4

SHT 14 OF 16

B297

CIRCUIT REFERENCES (CONTINUED).....

D501	79	D731	82
D502	79	D732	79
D503	79	D733	82
D504	79	D734	79
D506	79		
D507	75		
D508	75		
D509	75		
D510	75	LK141	112
~~D511~~	~~79~~	LK142	112
D601	79	LK161	112
D602	79	LK162	111
D603	79	LK163	112
D604	79	LK164	112
D605	79	LK241	112
D606	79	LK242	112
D607	75	LK261	112
D608	75	LK262	111
D609	75	LK263	112
D610	75	LK264	112
~~D611~~	~~79~~	LK361	112
D701	81	LK362	111
D702	81	LK363	112
D703	81	LK364	112
~~D707~~	~~79~~		
D708	81	LK341	112
D709	81	LK342	112
D710	79		
D711	79		
D712	81		
D713	81		
D714	79		
D715	79		
D716	81		
D717	81		
D718	79		
D719	78		
D720	79		
D721	79		
D722	77		
D723	79		
D724	79		
D725	83		
D726	83		
D727	83		
D728	83		
D729	82		
D730	79		

END OF CIRCUIT REFERENCES.

ORIGINAL FRAME SIZE 190mm x 277mm

THIRD ANGLE PROJECTION

All dimensions in millimetres unless otherwise stated:
Normal tolerances:
no decimal place - ± 1 mm unless
one decimal place - ± 0.3 mm otherwise
two decimal places - ± 0.1 mm stated

SCALE: – 0

ISS	CHANGE
1	1/2/89
2	12/5/89

BBC

DS/A4

C09/13
PARTS LIST

DRN.	DSE	D&ED
TCD.		D62641A4
CKD.		
APPD.	CCC	SHT 15 OF 16

R297

SHT.	ISS.	DETAILS OF CHANGE
2	2	R102 ... R602 ADDED TO ITEM 19 (WERE 200Ω VARIABLE).
3	2	R120.. R620 ADDED TO ITEM 36 R119.... R619 WERE A.O.T., R121...R621 ADDED (ITEM 39).
4	2	ITEM 41 DELETED, R102...R602. ITEM 50 WAS 33pF - 0204700.
6	2	ITEM 79 WAS 100 OFF.
7	2	D111....D611 ADDED. L701 (ITEM 88) DELETED
8	2	ITEM 94 ADDED U101... U601 WERE NE5534AN (ITEM 100) NOW ITEM 95. INFO D.BIRT (ISS 3 MODS) DSI 12/5/89

SHT.	ISS.	DETAILS OF CHANGE

ORIGINAL
FRAME SIZE
190mm x 277mm

BBC

YM 418/A4

DESIGNS DEPARTMENT

CODE:- C09/13 12/5/89

PARTS LIST CHANGE RECORD, ISSUE:- 2

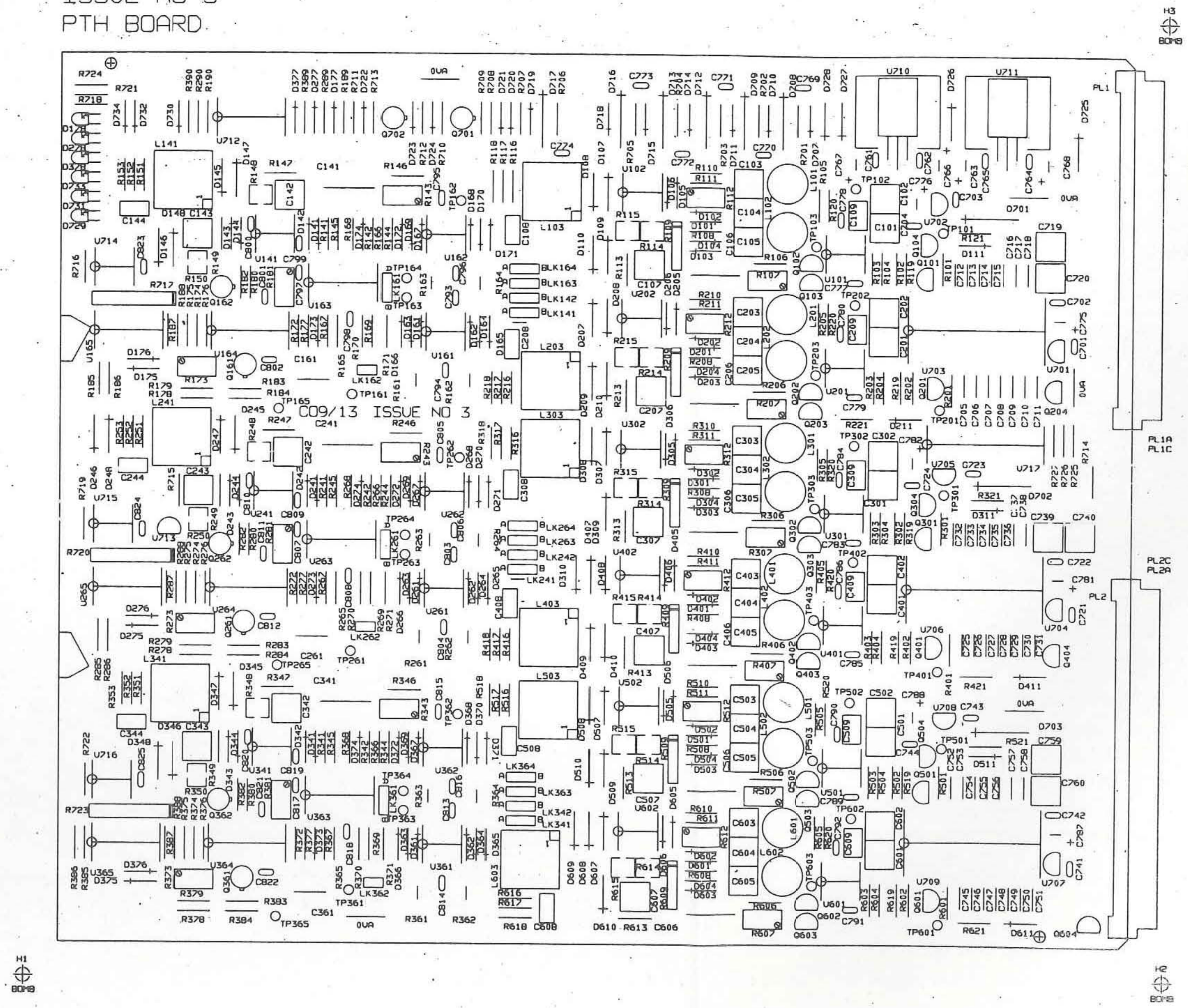
D 62641 A4

SHEET 16 OF 16

D27171A2

C09/13

ISSUE NO 3
PTH BOARD



SCALE:– 0

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE 400mm x 574mm

CHANGE

3 DSI 17.5.89

All dimensions in millimetres unless otherwise stated: Normal tolerances:

no decimal place	– ± 1	mm	unless
one decimal place	– ± 0.3	mm	otherwise
two decimal places	– ± 0.1	mm	stated

DRN.	DSI
TCD.	
CKD.	
APPD	

C09/13
ENHANCED COMP LOC

D.E.D

DSK27171A2

POWER SUPPLY - SXT 75/15

I/P

O/P

+S

-S

PL2 L N E

FL1

L(220)

L(110)

N

CT

TH1 VA1104

D16 D19 D17 D18 PY127

R26 220k C1 330

R4 180k

R5 180k

R9 1k

D11 MR817

D10 MR818

C6 680p

D12 MR818

R8 27R

D23 12V

D14 1N4934

C5 68n

R7 22R

L2

TR2 BU426A

R6 130

D15 BAX12

D20 1N4148

D21 1N4148

D13 1N4148

R1 200

R2 2k

R3 1·5R

R27 220k C2 330

C13 100n

C4 100n

T1

TR1 ZTX650

D5 1N4936

D6 1N4936

D1 S15SC4M

L1

R13c 0·12R

R13b 0·12R

R13a 0·12R

R30 0·22R

R10 100

R14 AOT

C17 1n

R32 5·1R

D8

R35 100R

TR4 TIP30

IC1 305

C11 47p

C12 10n

C7 100p

C10 47n

R17 330k

RV1 2k

R21 2k

C15 100n

C3a 2·2m

C3b 2·2m

R22 1k5

D55 1N4006

F1

PL1

R31 10k

R28 20

LK6

TR7 ZTX550

R34 10

R23 100

R33 1k

R19 13

TR5 ZTX550

TR8 ZTX450

D9 5V1

C9 22n

R18 47

R20 1k

R11 8·2R

D3 1N4936

TR3 BD204

R24 150

D2 S15S C4M

C8 47

TR6 ZTX650

R29 470

C16 4n7

R53 0·2R

IC51 L200 CV

R55 15k

R59 2k7

C55 100n

D51 BYV32-150

D52 BYV32-150

C51 220

R51 390R

AUX 1·5A D56 1N4006

R54 0·2R

IC52 L200

R56 15k

R60 2k7

C56 100n

D53 BYV32-150

D54 BYV32-150

C52 220

R52 390R

L51

AUX 1·5A D57 1N4006

note 1. AOT resistors R57 and R58 should not be fitted.

2. aux. output voltages are each 18V nominal.

SCALE:- 0

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE 574mm x 821mm

ISS	CHANGE	
1	31/1/89	
2	27-4-89	
3	23/5/89	

SWITCHED MODE POWER SUPPLIER

PS4/51 CIRCUIT

All dimensions in millimetres unless otherwise stated: Normal tolerances: no decimal place ± 1 mm unless; one decimal place ± 0·3 mm otherwise; two decimal places ± 0·1 mm stated

DRN.	CMD	DESIGN & EQUIPMENT DEPARTMENT
TCD.		
CKD.		D62830A1
APPD.	ccc	

D62830A1

DETAIL

ISS.	CHANGE
3	1/2/89
4	25/4/89

ITEM No.	No. OFF	DESCRIPTION	C'CT REF.	BBC REF. OR DRG. No.
		DRAWING LIST		
		CIRCUIT D62830A1		
		PARTS LIST D62831A4		
		ASSEMBLY & WIRING D62832A1		
		DETAIL 1 D62833A2		
		DETAIL 2 D62834A1		
		DETAIL 3 D62835A3		
		DETAIL 4 D62836A3		
		DETAIL 5 D62837A3		
		DETAIL 6 D62838A2		
		FRONT PANEL LEGEND D62840A1		
		FURTHER INFORMATION REQUIRED FOR MANUFACTURE		
		EA10484 - GENERAL ASSEMBLY.		
		UNIT SPEC - ED/PS4/51		
1	1	FRONT PANEL, 6U, EUROCARD BRICK CHASSIS MODIFIED BY CONTRACTOR TO :-		DETAIL 4 - D62836A3
2	1	SIDE PANEL (FIXED), 6U, EUROCARD, BRICK CHASSIS MODIFIED BY CONTRACTOR TO :-		DETAIL 1 - D62833A2
3	1	SIDE PANEL (HINGED), 6U, EUROCARD, BRICK CHASSIS MODIFIED BY CONTRACTOR TO :-		DETAIL 6 - D62838A2
4	2	SUPPORT PILLARS, 6U, EUROCARD, BRICK CHASSIS		
5	1	CODING PLATE, 6U, EUROCARD, BRICK CHASSIS MODIFIED BY CONTRACTOR TO :-		DETAIL 3 - D62835A3
6	1	HINGE ASSEMBLY KIT, BRICK CHASSIS		- 0630376
7	1	PERFORATED POWER SUPPLY CAGE MADE BY CONTRACTOR TO :-		DETAIL 2 - D62834A1
8	2	MOUNTING BRACKET, PLASTIC, BRICK CHASSIS		- 0628609
9	2	PLASTIC HANDLES & FIXING, BRICK CHASSIS		- 0628073
10	2	HANDLE CAP, PLASTIC, YELLOW		- 0466851
11	1	LABEL, WARNING, MAINS, SELF ADHESIVE		- 0628302

BBC

S/PLA4

PS4/51
POWER SUPPLY
PARTS LIST

DRN.	DSI
TPD.	
CKD.	
APPD	RCR

D & ED

D62831A4

SHT 1 OF 5

CHANGE	ISS.
1/2/89	4
25/4/89	5

ITEM No.	No. OFF	DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
12	1	LABEL, MAINS WARNING, 5 POLE CONNECTOR		
13	1	HEATSINK, REDPOINT TYPE Y211-1 ANODISED BK MODIFIED BY CONTRACTOR TO :-		-0628692 D62837A3 -DET 5
14	1	LABEL, SELF ADHESIVE VINYL, PSU WARNING MANUFACTURED TO DSK 27280A4		—
15	1	POWER SUPPLY, ADVANCE POWER SUPPLIES SXT 75/15		-0628589
16	1	FAN, 5V D.C., ULTRASLIM 62mm, RS 505-505		-0633213
17				
		CONNECTORS		
20	1	ERNIE, 11 POLE, FIXED PLUG (PL1)		S25092-0383312
21	1	ERNIE, 11 POLE, FIXED PLUG, MAINS (PL2)		-0628152
22	11	SOCKET TERMINAL, CRIMP, FREE, RS 532-800		
23	13	SPADE TERMINAL, CRIMP, FREE. RS 532-765		
24	4	SOCKET TERMINAL - EARTHING.		-0629192
25	3	SOCKET TERMINAL, SHROUDED, RS533-006		
		DIODES		
26	3	1N4006 (3) D1, D2, D3		-0102592
27				
28				
29				

BBC

PS4/51
PARTS LIST

DRN.	DSI
TPD.	
CKD.	
APPD	CCO

D & ED

D62831A4

SHT 2 OF 5

D62831A4

ISS.	CHANGE
2	1/2/89

ITEM No.	No. OFF	DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
30	1	FILTER, MAINS (FL1)		-0476509
31				
		WIRES & CABLES		
35	0.5m	PUF1/5M - BLACK		S14739 -0202477
36	0.5m	PUF1/5M - BLUE		S14739 -020253X
37	0.5m	PUF1/5M - GREEN/YELLOW		S14739 -0216785
38	0.5m	PUF1/5M - RED		S14739 -0202493
39	0.5m	PUF1/5M - ORANGE		S14739 -0202505
40	0.5m	PUF1/5M - BROWN		S14739 -0202485
41				
42				
43	0.5m	PUN1/1M - BLACK		S14626 -0216568
44				
45				
		FIXINGS & FASTNERS		FOR FIXING ITEMS
50	6	SCREW, M2.5 x 10 LG, INST HD, MS, CHR.PL.		1,8,6
51	4	SCREW, M2.5 x 10 LG, PAN HD, MS, Zn.PL.		3,20,21
52	10	SCREW, M2.5 x 8 LG, PAN HD, MS, Zn.PL.		3,8,6,4
53	3	SCREW, M2.5 x 6 LG, CSK HD, MS, Zn.PL.		2,5
54	1	SCREW, SELF TAPPING, TYPE B, 9.5 LG, Zn. PL.		-0430156
55	1	SCREW, M3 x 8 LG, CSK HD, MS. Zn PL		71
56	9	SCREW, M3 x 6 LG, CSK HD, MS, Zn. PL.		2,7,15,30,72
57	2	SCREW, M3 x 10 LG, PAN HD, M.S., Zn PL		13
58	12	NUT, M2.5		

BBC

S/PLA4

PS4/51 PARTS LIST

DRN.	DSI
TPD.	
CKD.	
APPD.	CCC

D & ED

D62831A4

SHT 3 OF 5

D62831A4

ISS. 3

CHANGE 1/2/89

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF	BBC REF. OR DRG. No.
59	1		NUT, M3		
60	3		NUT, M3, LOCKING BINX Bx213		
61	4		WASHER, M2·5, SHAKEPROOF		
62	1		WASHER, M6, PLAIN		
63	1		SOLDER TAG, S/E, M3		
64					
65	2		ANCHOR RIVET BUSH, M3		
66					
67					
68	1		HEATSINK COMPOUND, DOW CORING 340		-0498080
69					
70	1		CARTON CARDBOARD TO SPEC ED/PS4/51		
71	1		DOUBLE ENDED EARTH TAG, M3		-0629176
72	2		SINGLE ENDED EARTH TAG, M3		-0629184
			Notes.		
	✱		Denotes items supplied to the contractor on embodiment loan		
	✱ +		Denotes items supplied to the contractor on embodiment loan, requiring special costing or supply action by B.B.C.		
	θ ✱		Denotes components supplied and fitted by B.B.C. on test		
	θ +		Denotes coded plug in units supplied and fitted by B.B.C. on test.		
	Ø		Denotes items supplied and fitted by B.B.C. on installation		

BBC

S/PLA4

PS4/51 PARTS LIST

DRN.	DSI
TPD.	
CKD.	
APPD	CCC

D&ED

D62831A4

SHT 4 OF 5

SHT.	ISS.	DETAILS OF CHANGE	SHT.	ISS.	DETAILS OF CHANGE
1	4	CIRCUIT WAS A3.			
2	5	ITEM 16 ADDED.			

ORIGINAL FRAME SIZE 190mm x 277 mm

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED

BBC

VM418/A4

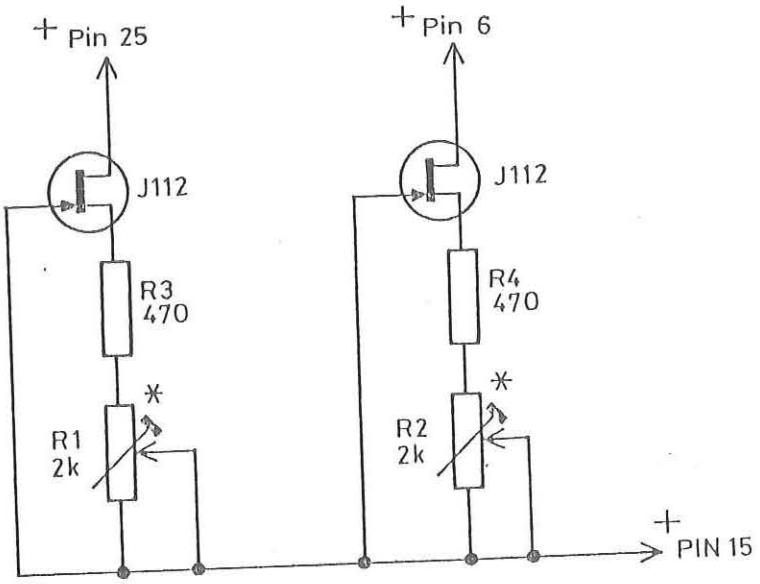
DESIGNS DEPARTMENT

CODE:- PS4/51 25/4/89

PARTS LIST CHANGE RECORD, ISSUE:- 2

D62831 A4

SHEET 5



NOTES

* Cemast 0306003
\+ 28 Pin header, replaces UXO3.

Setting Up

Equipment recquired :- 15V Power supplier.
Milliammeter.

Method

1. Set pots to maximum resistance.
2. Connect pin 15 to the negative pole of the 15V supply.
3. Connect pin 25 to the positive pole of the 15V supply in series with milliammeter, set R1 to give a current of 2mA.
4. Connect pin 6 in place of pin 25 to supply +. Set R2 for 2mA.

ORIGINAL FRAME SIZE 190mm x 277mm

THIRD ANGLE PROJECTION

All dimensions in millimetres unless otherwise stated:
Normal tolerances:
no decimal place ± 1 mm unless
one decimal place ± 0.3 mm otherwise
two decimal places ± 0.1 mm stated

SCALE:- 0

ISS	CHANGE	
1	10/11/88	

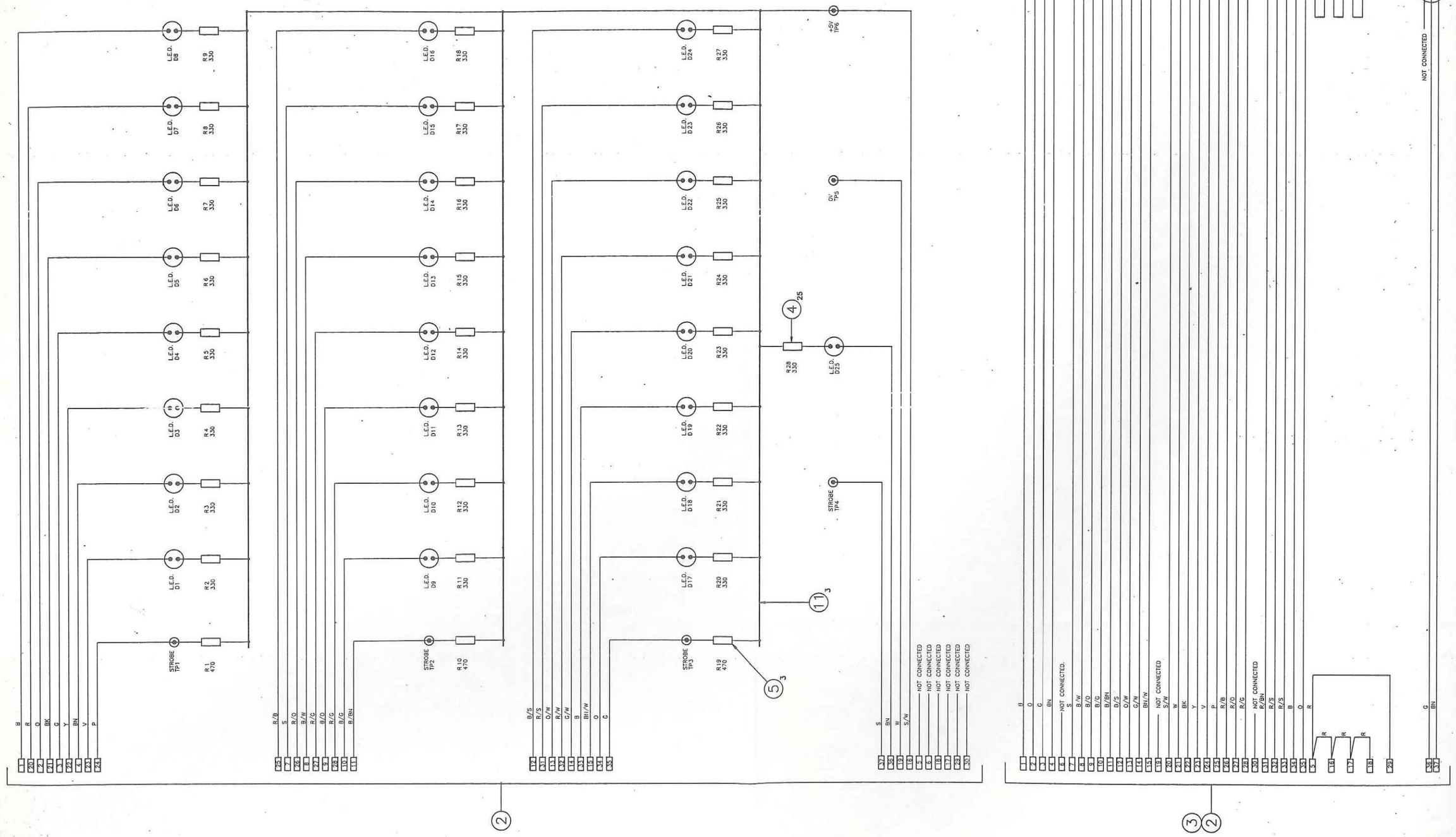
BBC

DS/A4

C09/13
TEST HEADER

DRN.	JDB	DESIGN & EQUIPMENT DEPT.
TCD.		DSK27206A4
CKD.		
APPD.	GRB	

R297



SCALE — 0

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE 574mm X 821mm

ISS	CHANGE
1	23—11—87

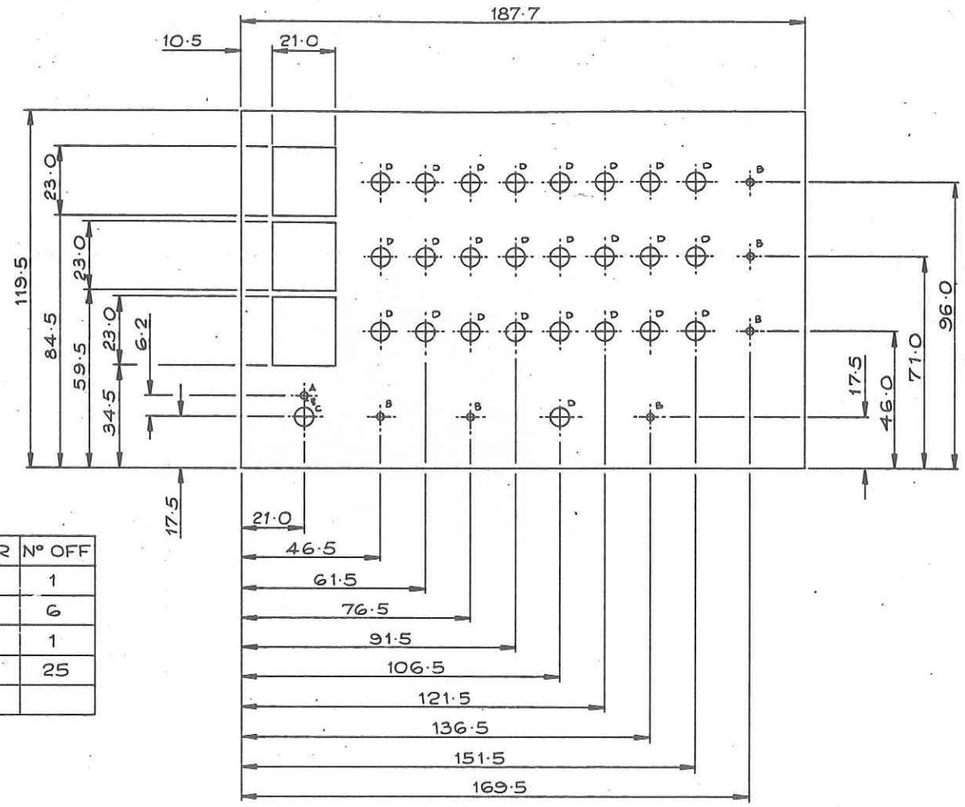
WIRING/ASSEMBLY. TE1/64

All dimensions in millimetres unless otherwise stated: Normal tolerances: no decimal place — ± 1 mm, one decimal place — ± 0.3 mm, two decimal places — ± 0.1 mm. Unless otherwise stated.

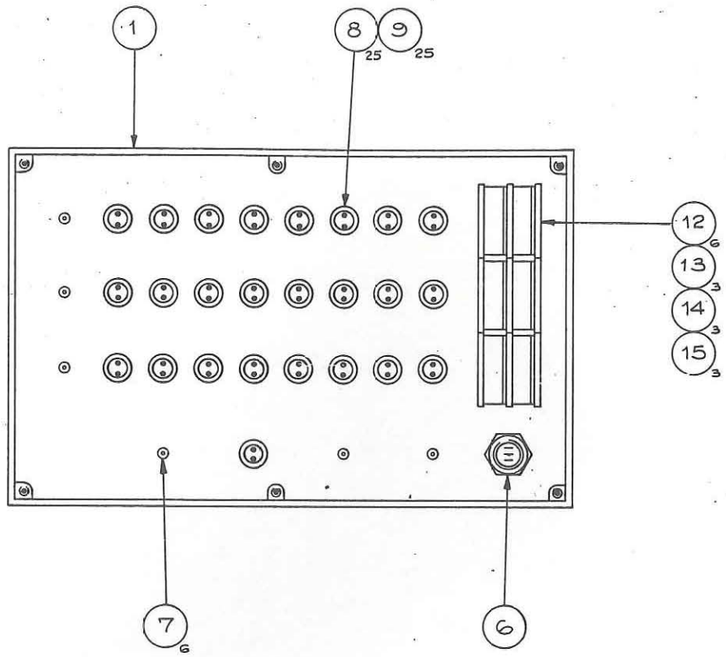
PLTD.	M.C.L.
TCD.	
CKD.	
APPD.	R.B.B.

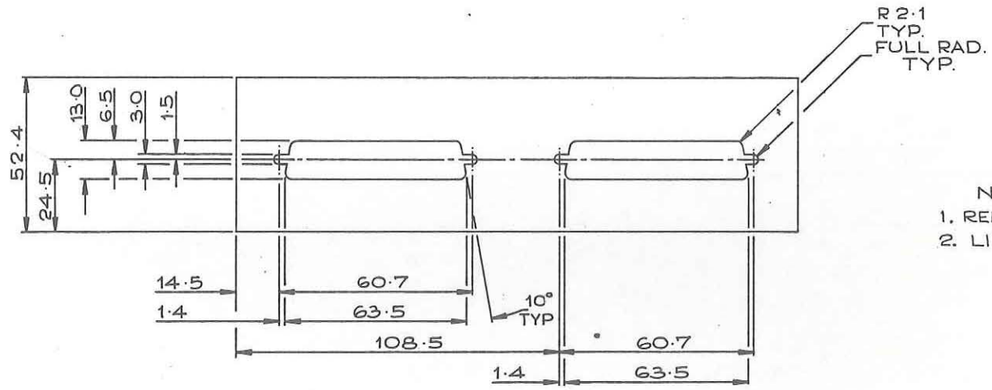
DESIGN AND EQUIPMENT DEPARTMENT

D64002A1



LETTER	DIAMETER	Nº OFF
A	ϕ2·2	1
B	ϕ5·4	6
C	ϕ6·2	1
D	ϕ6·4	25





NOTES.
1. REMOVE ALL SHARP EDGES AND BURRS.
2. LID REMOVED FOR CLARITY.

SCALE:– 0

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE
574mm x 821mm

CHANGE
T 28–11–89

DETAIL 1 /ASSEMBLY.

TE 1/64.

All dimensions in millimetres unless otherwise stated: Normal tolerances:
no decimal place – ± 1 mm unless
one decimal place – ± 0.3 mm otherwise
two decimal places – ± 0.1 mm stated

DRN. M.C.L. DESIGN & EQUIP. DEPT.
TCD.
CKD.
APPD.

D64003A1.

CHANGE	ISS.
23-11-89	1

ITEM No.	No. OFF	DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
		WIRING / ASSEMBLY.		D64002A1
		DETAIL 1 / ASSEMBLY.		D64003A1
		PARTS LIST.		D64004A4
		LEGEND TOP.		D64005A2
		LEGEND SIDE.		D64006A2
1	1	ALUMINIUM ALLOY BOX.		0027437.
2	2	'D' CONNECTOR, PLUG FIXED, 37 WAY.		0454600.
3	1	JACK POST ASSEMBLY.		0377384.
4	25	RESISTOR, 330Ω, METAL FILM 0·4W. R2-R9, R11-R18, R20-R28.		0099301.
5	3	RESISTOR, 470Ω, METAL FILM 0·4W. R1, R10, R19.		009904X.
6	1	SWITCH.		0098925.
7	6	TEST POINT. BALL TYPE. TP1-TP6.		0378294.
8	25	LED. GREEN. D1-D25.		0465653.
9	25	LED MOUNTING CLIPS.		0462781.
10	A/R	LACING TWINE (MEDIUM)		0039164.
11	A/R	B.T.C. WIRE. Ø0·6.		0051792.
12	6	SWITCH, BCD HEXIDECIMAL, 0-9, A-F. FARNELL TYPE No. PEHA 3000.		
13	3	SWITCH END CHEEK L.H. FARNELL TYPE No. 6090754.		
14	3	SWITCH END CHEEK R.H. FARNELL TYPE No. 6090756.		
15	3	SWITCH SPACER. FARNELL TYPE No. 6090760.		
16				
17				
18				
19				
20				
21				

BBC

/S/PLA4

TE1/64.
NICAM SIGNALLING TESTER.
PARTS LIST

DRN.	M.C.L.	DESIGN & EQUIP. DEPT.
TPD		D64004A4.
CKD		
APPD		SHEET 1 OF 3 SHEETS.

CHANGE	ISS.
23—11—89	1

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF	BBC REF. OR DRG. No.
22	A/R		CABLE. PUF 1/3M. BLUE.		020147X.
23	A/R		CABLE. PUF 1/3M. ORANGE.		0201488.
24	A/R		CABLE. PUF 1/3M. GREEN.		0201496.
25	A/R		CABLE. PUF 1/3M. BROWN.		0201508.
26	A/R		CABLE. PUF 1/3M. SLATE.		0201516.
27	A/R		CABLE. PUF 1/3M. BLUE/WHITE.		0406042.
28	A/R		CABLE. PUF 1/3M. BLUE/ORANGE.		0406050.
29	A/R		CABLE. PUF 1/3M. BLUE/GREEN.		0406069.
30	A/R		CABLE. PUF 1/3M. BLUE/BROWN.		0406077.
31	A/R		CABLE. PUF 1/3M. BLUE/SLATE.		0406085.
32	A/R		CABLE. PUF 1/3M. ORANGE/WHITE.		0406093.
33	A/R		CABLE. PUF 1/3M. GREEN/WHITE.		0406105.
34	A/R		CABLE. PUF 1/3M. BROWN/WHITE.		0406113.
35	A/R		CABLE. PUF 1/3M. SLATE/WHITE.		0406121.
36	A/R		CABLE. PUF 1/3M. WHITE.		0201524.
37	A/R		CABLE. PUF 1/3M. RED.		0201532.
38	A/R		CABLE. PUF 1/3M. BLACK.		0201540.
39	A/R		CABLE. PUF 1/3M. YELLOW.		0201559.
40	A/R		CABLE. PUF 1/3M. VIOLET.		0201567.
41	A/R		CABLE. PUF 1/3M. PINK.		0375860.
42	A/R		CABLE. PUF 1/3M. RED/BLUE.		040613X.
43	A/R		CABLE. PUF 1/3M. RED/ORANGE.		0406148.
44	A/R		CABLE. PUF 1/3M. RED/GREEN.		0406156.
45	A/R		CABLE. PUF 1/3M. RED/BROWN.		0406164.
46	A/R		CABLE. PUF 1/3M. RED/SLATE.		0406172.
47	A/R		CABLE. PUF 1/3M. RED/WHITE.		0406180.

BBC

3/PLA4

PARTS LIST. TE1/64.

DRN.	M.C.L.	DESIGN & EQUIP. DEPT.
TPD.		D64004A4.
CKD		
APPD.	R.B.W.	SHEET 2 OF 3 SHEETS

SHT.	ISS.	DETAILS OF CHANGE	SHT.	ISS.	DETAILS OF CHANGE

ORIGINAL FRAME SIZE 190 mm x 277 mm

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED

BBC

VM 418/A4

DESIGNS DEPARTMENT

CODE:- TE1/64

PARTS LIST CHANGE RECORD, ISSUE:- 1 23/11/89

D64004 A4

SHEET 3

NICAM 3 MKII SIGNALLING TEST BOX

MINIMUM SIZE TO CUT NEGATIVE

MSB CHANNEL 1/2 LSB STROBE X

CHANNEL 3/4 STROBE Y

CHANNEL 5/6 STROBE Z

2048 BIT 1

2048 BIT 0

+5V

OV

2048 DATA

2048 STROBE

TE1/64

BBC

D64005A2

SCALE 2:1

D64005A2

SCALE:– 0

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE 400mm x 574mm

ISS 1 CHANGE 29/8/89

SIGNALLING TEST BOX

TE1/64 LEGEND

All dimensions in millimetres unless otherwise stated: Normal tolerances:
no decimal place – ± 1 mm unless
one decimal place – ± 0.3 mm otherwise
two decimal places – ± 0.1 mm stated

DRN. J DB DESIGN & EQUIPMENT DEPARTMENT
TCD.
CKD.
APPD

D64005A2

R293

D64006A2

MINIMUM SIZE TO CUT NEGATIVE

TO CODER

TO DECODER

SCALE 2:1

SCALE: – 0

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE
400mm x 574mm

ISS	CHANGE	
1	29/8/89	

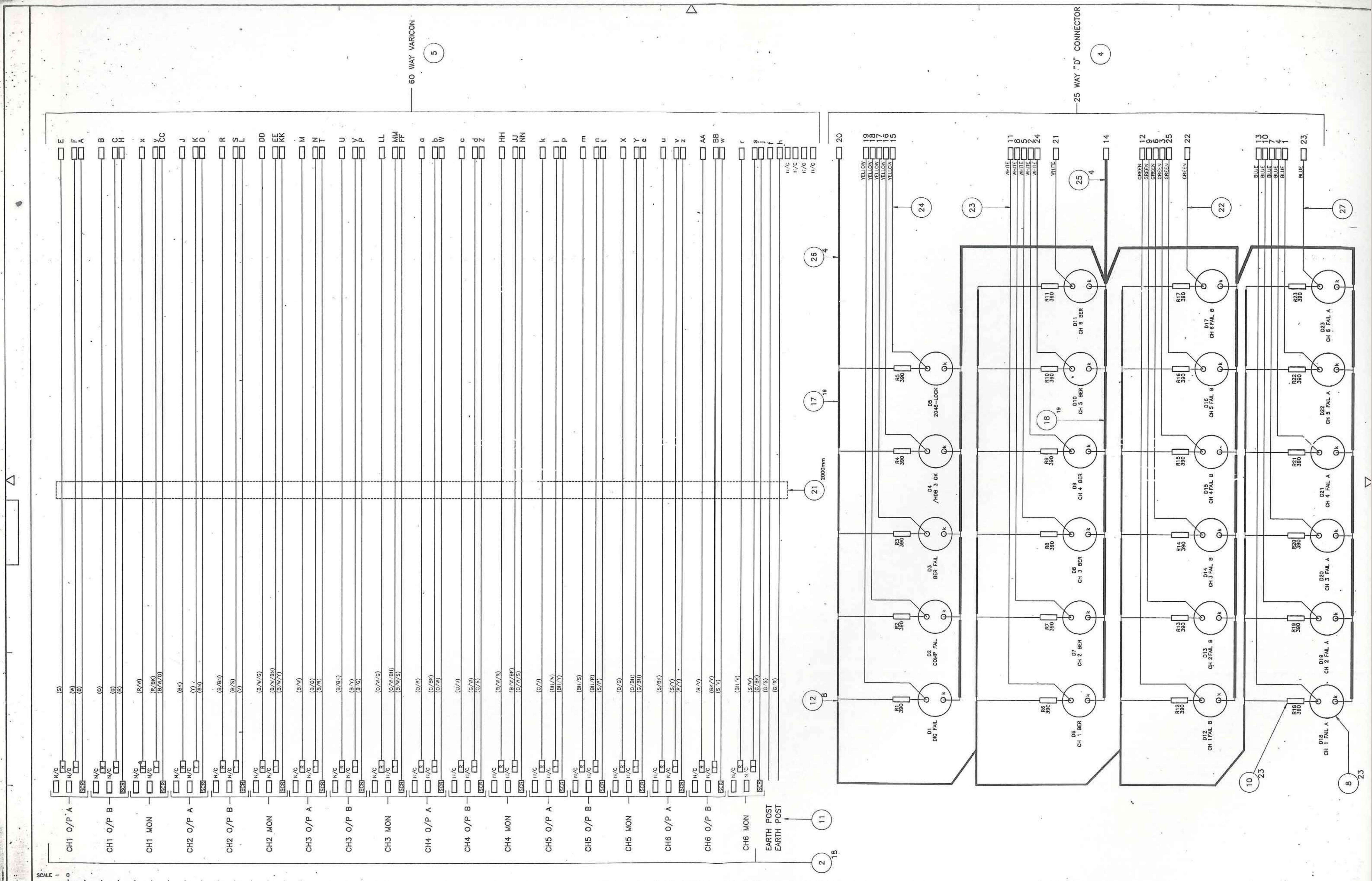
SIGNALLING TEST BOX

TE1/64
LEGEND

All dimensions in millimetres unless otherwise stated: Normal tolerances:
no decimal place – ± 1 mm unless
one decimal place – ± 0.3 mm otherwise
two decimal places – ± 0.1 mm stated

DRN.	J DB	DESIGN & EQUIPMENT DEPARTMENT
TCD.		
CKD.		D64006A2
APPD	R.B.D	

R293



SCALE – 0

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE 574mm X 821mm

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ISS	CHANGE
1	22-11-89

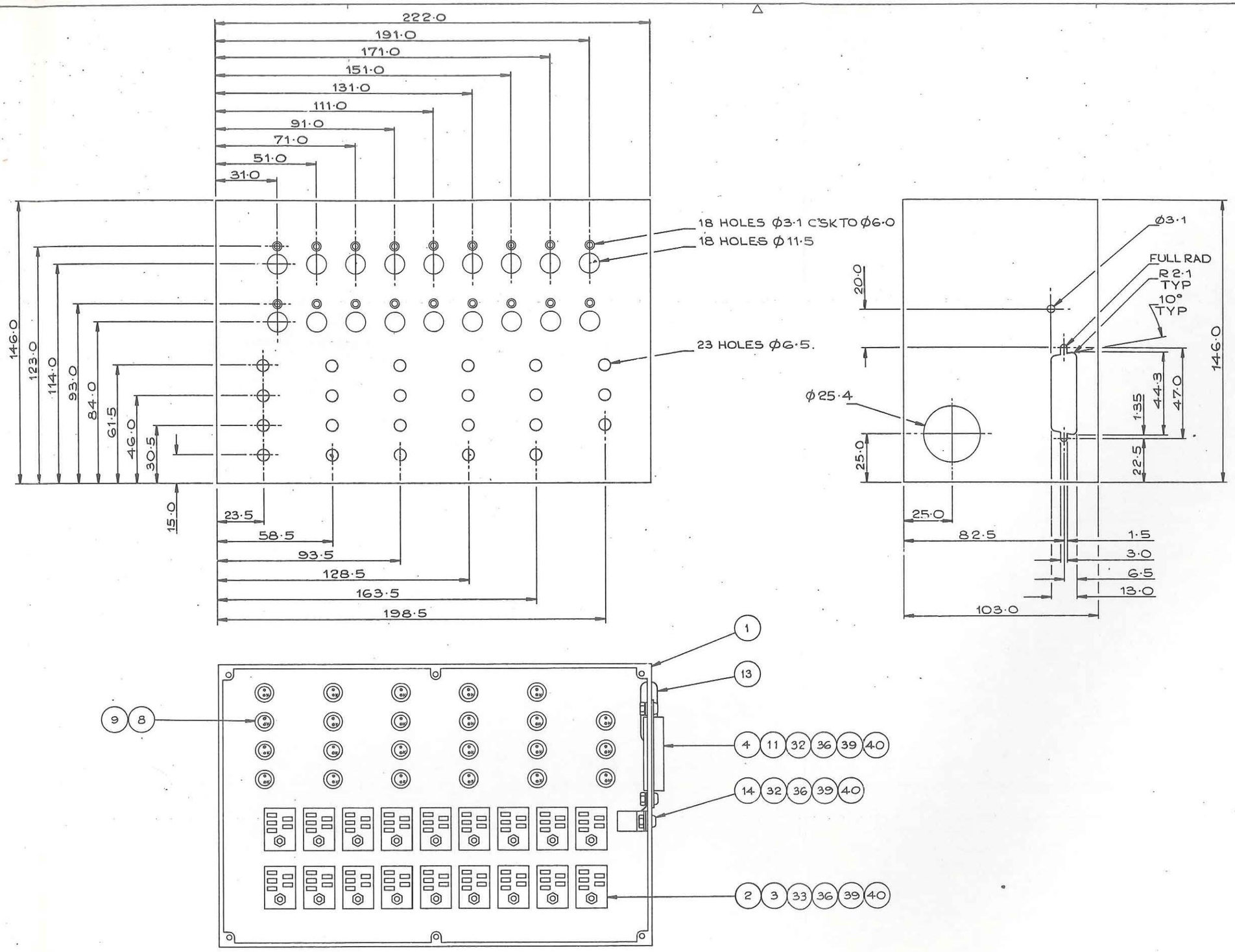
WIRING/ASSEMBLY DIAGRAM. TE1/65.

All dimensions in millimetres unless otherwise stated. Normal tolerances:
no decimal place – ± 1 mm
one decimal place – ± 0.3 mm
two decimal places – ± 0.1 mm
Unless otherwise stated

PLTD. M.C.L.
TCD.
CKD.
APPD.

DESIGN AND EQUIPMENT DEPARTMENT

D64009A1



VIEW ON INSIDE OF BOX.

SCALE: – 0

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE 574mm x 821mm

ISS 1 CHANGE 23—11—87

DETAIL 1/ASSEMBLY TE1/65.

All dimensions in millimetres unless otherwise stated: Normal tolerances:
no decimal place – ± 1 mm unless
one decimal place – ± 0.3 mm otherwise
two decimal places – ± 0.1 mm stated

DRN. M.C.L. DESIGN & EQUIP DEPT.
TCD.
CKD.
APPD. K.G.P. DG4010A1.

CHANGE	ISS.
23—11—89	1

ITEM No.	No. OFF	DESCRIPTION	CCT REF	BBC REF. OR DRG. No.
		WIRING/ASSEMBLY.		D64009A1
		DETAIL 1/ASSEMBLY.		D64010A1
		PARTS LIST.		D64011A4
		LEGEND.		D64012A2
1	1	CAST BOX. RS TYPE Nº. MODIFIED TO DETAIL 1.		
2	18	AUDIO JACK SOCKETS.		0379082.
3	18	JACK MOUNTING BLOCKS.		0025763.
4	1	25 WAY 'D' CONNECTOR PLUG.		0584064.
5	1	56 WAY VARICON PLUG		0206023.
6	56	VARICON CONTACTS CRIMP		0488776.
7	1	VARICON HOOD		0362308.
8	23	L.E.D's GREEN (23) D1 – D23.		0465610.
9	23	L.E.D. MOUNTING CLIP		0462781.
10	23	RESISTOR 390Ω METAL FILM 0·4W (23) R1 – R23.		0099354.
11	1	SOLDER TAG M3.		0033483.
12	A/R	B.T.C. WIRE. ϕ1·0		0051768.
13	1	GROMMET. I/D 19·1.		0251141.
14	1	'P' CLIP.		0250617.
15				
16				
17	A/R	SLEEVE ϕ1·0 BORE.		0254352.
18	A/R	SLEEVE ϕ1·0 BORE.		0254379.
19				
20				

BBC

TE1/65
NICAM 3 MKII TEST BOX.
PARTS LIST

DRN.	M.C.L	DESIGN & EQUIP. DEPT.
TPD.		D64011A4.
CKD.		
APPD.		SHEET 1 OF 3 SHEETS

ISS.	CHANGE
1	23-11-89

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
21	2m		CABLE PSF/60.		0306413.
22	A/R		CABLE PUF1/3M. GREEN.		0201496
23	A/R		CABLE PUF 1/3M. WHITE.		0201524.
24	A/R		CABLE PUF 1/3M. YELLOW.		0201559.
25	A/R		CABLE PUF 1/3M. BLACK.		0201540.
26	A/R		CABLE PUF 1/3M. RED.		0201532.
27	A/R		CABLE PUF 1/3M. BLUE		020147X.
28					
29					
30					
31					For fixing items.
32	3		SCREW M3 x 8Lg.		4, 14.
33	18		SCREW M3 x 16 Lg.		2.
34					
35					
36			NUT M3.		2,4,14
37					
38					
39			WASHER M3 PLAIN.		2,4,14.
40			WASHER M3 SHAKEPROOF.		2.4,14.
41					
42					
43					
44					
45					

BBC /PLA4

PARTS LIST.
TE1/65.

DRN.	M.C.L.	DESIGN & EQUIP DEPT.
TPD.		DG4011A4.
CKD		
APPD		SHEET 2 OF 3 SHEETS

SHT.	ISS.	DETAILS OF CHANGE	SHT	ISS	DETAILS OF CHANGE

ORIGINAL
FRAME SIZE
190mm x 277mm

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED

BBC

VM 418/A4

DESIGNS DEPARTMENT

CODE TE1/65

PARTS LIST CHANGE RECORD, ISSUE :- 1. 23/11/89

D64011 A4

SHEET 3

D64012A2

NICAM 3 MKII TEST BOX

CH1 O/PA CH1 O/PB CH1 MON CH2 O/PA CH2 O/PB CH2 MON CH3 O/PA CH3 O/PB CH3 MON

CH4 O/PA CH4 O/PB CH4 MON CH5 O/PA CH5 O/PB CH5 MON CH6 O/PA CH6 O/PB CH6 MON

CH1 FAIL A CH2 FAIL A CH3 FAIL A CH4 FAIL A CH5 FAIL A CH6 FAIL A

CH1 FAIL B CH2 FAIL B CH3 FAIL B CH4 FAIL B CH5 FAIL B CH6 FAIL B

CH1 BER CH2 BER CH3 BER CH4 BER CH5 BER CH6 BER

DIG FAIL COMP FAIL BER FAIL /HDB 3 OK 2048-LOCK

TE1/65

BBC

SCALE 2:1

MINIMUM SIZE TO CUT NEGATIVE

SCALE:- 0

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE 400mm x 574mm

ISS	CHANGE	
1	29/8/89	

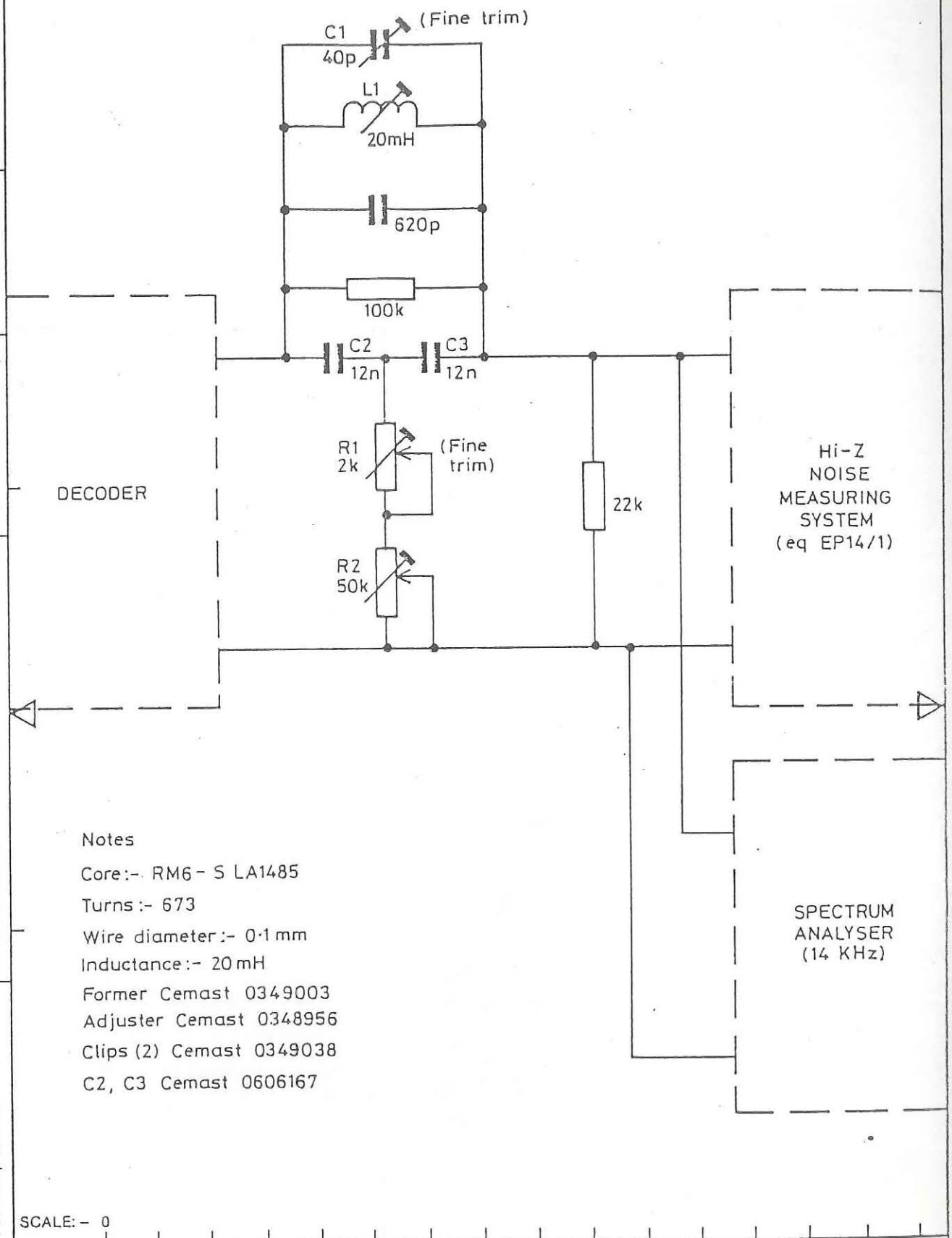
TEST BOX

TE1/65
LEGEND

All dimensions in millimetres unless otherwise stated: Normal tolerances:
no decimal place – ± 1 mm unless
one decimal place – ± 0.3 mm otherwise
two decimal places – ± 0.1 mm stated

DRN.	JDB	DESIGN & EQUIPMENT DEPARTMENT
TCD.		
CKD.		D64012A2
APPD	K.A.J.	

R293



Notes

Core:- RM6 - S LA1485

Turns:- 673

Wire diameter:- 0·1 mm

Inductance:- 20 mH

Former Cemast 0349003

Adjuster Cemast 0348956

Clips (2) Cemast 0349038

C2, C3 Cemast 0606167

SCALE:- 0

ORIGINAL FRAME SIZE 190mm x 277mm

THIRD ANGLE PROJECTION

All dimensions in millimetres unless otherwise stated:
Normal tolerances:
no decimal place – ± 1 mm unless
one decimal place – ± 0.3 mm otherwise
two decimal places – ± 0.1 mm stated

BBC

DS/A4

ISS	CHANGE
1	17/11/88

C09/13
TEST NOTCH FILTER

DRN.	JDB	DESIGN & EQUIPMENT DEPT.
TCD.		DSK27215A4
CKD.		
APPD.	ERB	

R297