DESIGN & EQUIPMENT DEPARTMENT

HANDBOOK A.1027(87)

CD4S/18 NICAM 3 SIGNALLING SPLITTER

.....
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for H.D.& E.D.

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1. INTRODUCTION

The NICAM 3 Signalling Splitter (CD4S/18) is a 4U unsupported card with an A-width front panel, which is used in conjunction with a NICAM 3 2-channel Decoder (CD3M/33 or equivalent) fed by a NICAM 3 Coder (CD2M/17) with a NICAM 3 Signalling Combiner (CD4S/17). Such a network provides two major facilities:

(i) Two RS232C serial character streams, input to the Combiner, are available as outputs from every Splitter on the network. One stream, designated MAIN, will be used to distribute Radio Data (RDS) update information via the national NICAM 3 network. The other stream, designated AUXILIARY, is available for any other future requirement, as yet unspecified. The channels have similar characteristics, but the MAIN channel is awarded a higher priority.

(ii) A 16-bit Transmitter Control word (TXCTRL) is output by every Splitter. The contents of this word are determind by 16-bits input to the Combiner, which may be sent either to all Splitters on the network or to individual Splitters or groups of Splitters. The individual bits may be used to control transmitter functions (such as mono/stereo switching) at each Splitter site.

There are two versions of the software, the version chosen being dependant on the location of the Splitter. Monitoring Splitters in Broadcasting House can be made to alarm in response to a Combiner reset. Splitters at transmitter site will not respond to a Combiner reset.

The Splitter is designed around the ADZE 2 general purpose microcomputer module, which is fully described in DDHB 6.267(85).

2. SPECIFICATION

Maximum supply voltage: +5.25 V
Nominal supply voltage: +5 V
Minimum supply voltage: +4.8 V

Nominal supply current: 0.75 A

Main serial (DCE) port:

Electrical characteristics:
To EIA std RS232C

Interface connections:
Data output (RXD)
Data input (TXD)
Handshake input (DTR)
Signal ground

Baud rate (input and output):
300, 600, 1200, 2400, 4800, 9600 baud, set from front panel

Data format:
8-bits, 1 stop bit, no parity

Flow control:
Both DTR and X-ON/X-OFF (DC1/DC3) are accepted

Auxiliary (DCE) port:

As main port

TXCTRL port:

Interface connections:
Signal ground
Data open collector outputs (16 off)

Maximum data output logic '1' voltage:
+30 V

Maximum data output logic '0' current:
40 mA

NICAM 3 Interface port:

Interface connections:
Strobe input optocoupler anode
Strobe input
Data optocoupler common anode
Data inputs (8 off)

Strobe input load (anode to input):
LED (1.5 V drop) with series 470R resistance

Nominal strobe input current (logic '0'):
5 mA

Maximum strobe input current:
15 mA

Input load (common anode to any data bit):
LED (1.4 V drop) with series 2k2 resistance

Nominal data input current (logic'0'):
1.6 mA

Maximum data input current:
20 mA

Dimensions:

4U high BMM unsupported card with A-width front panel

Weight:

Approximately 350 g

Connector:

112-way edge connector
See DSK26738 A4 for pinout details

3. OPERATION

3.1. Power Supplies

The unit requires a single supply of 5 V nominal. The voltage on the card must not fall below 4.75 V, because, quite apart from this being the lower limit at which operation of many of the ICs is guaranteed, the non-volatile RAM device, IC7, will disable RAM access below this voltage.

3.2. Serial Outputs

The MAIN and AUXILIARY serial output ports are normally connected to female 25-way D type connectors fixed to the parent cardframe. These should be wired as DCE ports, with suggested connections as follows:

1	Safety ground
2	TXD input
3	RXD output
4	(Connect to 5)
5	(Connect to 4)
6	Assert (high) level output
7	Signal ground
20	DTR input

Data receivers should be set to 8-bits, no parity. Flow control may be implemented in either of two ways; the Splitter will cease output if DTR becomes inactive (low), or if it receives an X-OFF character via TXD. Output will restart when DTR becomes active (high) or an X-ON character is received. Because both these flow control techniques are supported, the DTR input must be active to enable X-ON/X-OFF control. This condition will generally be supplied by the connected equipment, but an RS232C Assert level (high) is provided as an output from the Splitter in case it is needed.

3.3. TXCTRL Output

The 16-bit TXCTRL data output is buffered by high-voltage open-collector drivers. These are not internally pulled up in the logic '1' (off) state. External overvoltage protection must be provided if they are used directly to drive inductive loads such as relays.

3.4. NICAM 3 Data Port

The NICAM 3 data port connects directly to the signalling port of the NICAM 3 Decoder. The data inputs are optically isolated from the main circuit. The anodes of the optocouplers are connected together, and should be fed from a +5 V reference supply. The signalling bit inputs to the cathodes have internal series current limiting resistors, so that they may be driven directly by the open-collector NICAM 3 Decoder outputs. The open-collector strobe pulse from the decoder is buffered in a similar way, except that the coupler is a special high-speed type, and the internal limiting resistor has a lower value.

3.5. FAULT Output

The open-collector FAULT output is normally low (on). It is driven high (off) if the equipment detects a serious error condition (ie, whenever the front panel FAULT LED indicates a fault - described later). This polarity ensures that a fault is signalled as a result of power failure.

3.6. Non-volatile Memory

Because there are many options affecting the characteristics of the Splitter, these are set up interactively via the front panel (as described in the next section) and stored in non-voiatile memory. This memory is protected in three ways. A logic circuit prevents writing to memory when the power rail drops below 4.75 V, at whlch point an internal lithium battery cuts in to preserve the memory. Wlth power applied, the memory is electrically write-protected at all times except when the PROGRAM key is depressed. Furthermore, two copies of the system control data are maintained in non-volatile memory, both protected by 16-blt cyclic redundancy check codes.

3.7. Displays and Controls

The front panel contains 4 LEDs, 4 pushbutton keys and a 4-character alphanumeric display. The latter device has 4 functions; during normal (non-interactive) operation, it displays either the Combiner Source/Ident code for the most recently actioned TXCTRL packet, or a hexadecimal representation of the TXCTRL data output. If the unit detects a serious error, a code appears on the display accompanied by an indication on the FAULT LED and the FAULT signalling output; this takes priority over any other display. Less serious errors result in a display code and a WARNING LED indication. Finally, the display operates with the keys below it during setup and review of the various system options described below. All the programmed display messages are summarised in Appendix A.

3.7.1. CPU Normal LED

The green CPU Normal LED reflects the state of the 'watchdog timer' which resets the system in the event of a soft malfunction or on power-up. The LED should normally glow continuously; flashing indicates a probable hardware error.

3.7.2. Status Display

During normal (non-interactive) operation, the alphanumeric display shows either the Combiner Source/Ident code for the most recently actioned TXCTRL packet, or a hexadecimal representation of the current TX Control outputs.

3.7.3. Selecting A System Control Item

Use the SELECT key to select one of the system control items. Each time the key is pressed, the next item name is displayed. If the key is held down, the display will cycle through the items automatically until the key is released.

3.7.4. Examining The Item Setting

Once an item is selected, if no further keys are pressed, the Splitter will display a three-word explanation of the item code followed by the setting currently programmed for the item. This is displayed for a short time, then the Splitter will revert to its normal (non-Interactive) operation.

3.7.5. Examining Several Item Settings

SELECT may be pressed at any stage during the above sequence in order to select the next menu item in the sequence. Furthermore, the 3-word explanation may be bypassed or aborted by pressing the REVIEW key. Thus the settings of all items in the menu may be examined by alternately pressing SELECT and REVIEW.

3.7.6. Reviewing Alternative Settings

When the current setting of an item is displayed (accompanied by an indication on the CURRENT LED), alternative settings may be seen by pressing the REVIEW key. Like SELECT, this cycles through all the options and repeats automatically if held down.

3.7.7. Changing The Current Setting

When a setting has been selected with the REVIEW key, the PROGRAM key (coloured red) may be pressed to store that setting permanently. PROGRAM should be held down until the CURRENT LED indicates that the setting is now the current one. This is necessary because the non-volatile system control memory can be altered only when PROGRAM is pressed, and the programming operation involves copying a large block of data copied to that memory. The Splitter checks that the data has been copied successfully; if not, the display will indicate REPT accompanied by the WARNING LED, and the programming operation should be repeated.

When any item setting has been displayed for a short time without any keys pressed, the Splitter will exit its menu mode and revert to the background status display.

3.7.8. System Control Items in Detail

3.7.8.1. Serial Baud Rates (BR 1, BR 2)

These items determine the data rates of the Main (RDS) and Auxillary serial ports respectively. In both cases, the transmit and receive rates are identical. All 'standard' speeds (binary sequence) are supported from 300 to 9600 baud.

3.7.8.2. LED Characteristics (LEDS)

Different users have different views about LED indications. Some people prefer red LEDs which are normally off, others want green LEDs which are normally on. This equipment provides a choice via the LEDs setting. A variety of 'normally off' colour combinations for the 3 LEDs is available, in addition to all red, yellow or green 'normally on' options.

3.7.8.3. Status Display (SDPY)

Three options are available controlling the display of fault and warning messages. The instantaneous (INST) option means that every displayed message remains only for the duration of the offending condition (strictly for a short time after the condition clears). The HOLD option 'freezes' any fault or warning signal until the CLEAR key is pressed. The third option, FHWI, 'freezes' fault signals but displays warning messages on an instantaneous basis.

3.7.8.4. Normal Display (NDPY)

This determines what information is displayed during normal (non-interactive) operation. The NAME option sets the current Source/Ident code for display, the DATA option sets the current TXCTRL data in hexadecimal.

3.7.8.5. Combiner Source/Ident List (BH01..BE00)

These items control the behaviour of the Splitter when each of the possible Combiner Source/Ident codes is received in the TXCTRL packet. Each code may be set to OK (ie normal or expected codes) or ALRM (invalid codes, the receipt of which indicates a service routing error). If the Splitter receives one of the invalid codes, it ignores the packet data, displays the fault message 'IVID' and turns on the WARNING LED. A fault condition is also flagged by setting D9 of the TX control output bits. The Source/Ident list settings have no effect on the serial data channels.

3.7.8.6. Splitter Address List (ALLS..GLAS)

These items control the behaviour of the Splitter when each of the possible Splitter Address codes is received in a TXCTRL packet. Each code may be set to IGNR (ie, ignore packet data) or ACT (ie, packet is actionable). Only TXCTRL packets with a valid Combiner Source/Ident Code (see above) and an actionable Splitter Address Code are used to update the TXCTRL output word.

3.7.8.7. Initialise (INIT)

This item is used to reset the Splitter to its default state. With this item displayed the Splitter will reset when the PROGRAM key is pressed.

4. CIRCUIT DESCRIPTION

(Notation throughout: IC7p9 means IC7 pin 9. All addresses and data representations are stated in hexadecimal radix unless otherwise indicated. Numerical ranges are stated using the PASCAL convention eg, 0..3 means 0, 1, 2, 3.)

4.1. ADZE 2 Computer Module

The ADZE 2 module, which forms the hardware basis of this design, is fully described in DDHB 6.267(85). The 40-way main interface plug (PLB) is connected to a simiiar 40-way plug via a short ribbon cable, which may be disconnected to isolate the ADZE 2 module for testing (power supply connections are made via permanent PCB tracks). Modifications to the ADZE 2 are as follows:

(i) XLi is a 9.83 MHz crystal (30 pF parallel resonant) to facilitate division down to the standard serial baud rates.

(ii) IC5 is a Z80B-CPU, to run at the higher clock frequency.

(iii) IC6 is a 16k x 8 EPROM, 250 ns address access, eg, Intel 27i28-25.

(iv) IC7 is an 8k x 8 low-power static RAM, 200 ns address access, eg, Hitachi HM6264LP-15, with Dallas 'SmartSocket' DS1213 providing battery backup and protection logic.

(v) IC8 is an 8k x 8 static RAM, 200 ns address access, eg, Hitachi HM6264P-15 or HM6264LP-15.

(vi) LK3 and LK1 are 'standard' ADZE 2 memory configuration headers for IC6 and IC8 (see DSK25411 A3). LK2 is specially wired to provide write protection switching, see D60164 A2.

(vii) LK4 is wired with pins 4 and 5 connected, to provide a watchdog run time of 0.85 sec.

4.2. Front Panel

The front panel CPU Normal LED, pushbutton keys and alphanumeric display follow standard 'ADZE 2' practice (see DSK25412 A3). The remaining 3 LEDs are two-colour, common cathode devices whose cathodes are connected conventionally to bits 0, 1 and 2 of the ADZE 2 LED drive port. The anodes are switched by TR1 and TR2 under the control of bits 4 and 5 of the LED port. The arrangement allows any combination of the LEDs to be lit with the same colour, red (TR2 on), green (TR1 on) or yellow (both transistors on), by means of a single control byte written to the LED port.

4.3. Counter-Timer

IC20 is a Z80B-CTC, providing 4 counter-timer channels derived from the 4.9152 MHz system clock. It is configured as the highest priority device in the interrupt daisy-chain (IEI is connected to +5 V, and IEO feeds the next device in the chain), and mapped to port addresses C0..C3. Mode 2 Z80 interrupts are fully supported. Hardware reset is accomplished by the system watchdog timer.

Channel 0, which has the highest interrupt prlority, is externally triggered by the NICAM strobe pulse input (CLK/TRG0 pin). When initialised in timer mode by the software, it lnterrupts the CPU shortly after each strobe pulse, to indicate that a new byte of NICAM data is required.

Channels 1 and 2 are used to generate baud rate clocks for the two DART channels. They are initialised by the software to operate in cyclic counter mode, generating clock pulses at the zero-count pins, which feed the DART, IC21. The pulse frequency is 16 times the baud rate. No interrupts are requested by these channels.

Channel 3 is used without external connections, as a real-time clock reference for such things as timing the menu displays. It is initialised by the software to interrupt the CPU every 10 msec.

4.4. RS232 Communications

IC21, a Z80D-DART (Dual Asynchronous Receiver Transmitter), interfaces the CPU to the two bi-directional serial ports. IC29 and IC30 convert between 'TTL' logic levels and 'RS232' voltages; they each contain 4 lnverting buffers (2 send, 2 receive) powered by an internal voltage converter.

The Z80D-DART provides a subset of the more familiar Z80-S10 functions. In this application it uses port addresses A0..A3 and mode 2 interrupts, taking second priority to IC20 (IEI comes from IEO of IC20; IEO is the end of the daisy-chain). Hardware reset is accomplished by the system watchdog timer. Input and output handshake pins (CTS and DTR) are both connected to the RS232 drivers for each channel, although only CTS (Z80B-DART designation) is actually used.

4.5. TXCTRL Data Output

The 16-bit TXCTRL data is captured from the CPU data bus by octal latches IC23 (low byte) and IC24 (high byte), which form 'standard' ADZE 2 ports at addresses 0 and 20 respectively. The outputs are buffered by open collector drivers IC27, IC28 and IC29.

4.6. NICAM 3 Strobe Pulse Input

Because the NICAM strobe is of short duration (700 ns), its optocoupler IC32 is a special high-speed type, specified for 5 mA input current (hence the low value of R18, for 5 V input).

4.7. NICAM 3 Data Input

the 8-bit NICAM 3 data input is buffered and isolated by optocouplers IC34..IC37. These are dual couplers, specified for 1.6 mA input current. Resistors R21 and R22 set the current to this value with 5 V applied across the floating input terminals. R19 pulls the open collector coupler outputs to +5 V.

IC25 is a 'standard' ADZE 2 input port mapped to address 60. It is read after every NICAM 3 strobe pulse.

4.8. Fault Signalling Output

IC22 provides an 8-bit parallel output port at address 80. Bit 0 of this port carries the fault detection output, which is presented to the host equipment through high-voltage open-collector driver IC27.

5. SOFTWARE DESCRIPTION

5.1. Functionality

This section describes what the system does, in terms of inputs, processing and outputs.

5.1.1. Packet Structure

Every 3 ms a strobe pulse from the NICAM 3 Coder triggers channel 3 of the Z80-CTC, which subsequently interrupts the CPU requesting it to read the next byte of NICAM data. This must be read during the time window between 0.1 ms and 2.9 ms after the strobe pulse.

The input from the NICAM 3 decoder comprises a continuous stream of bytes, which are generated in groups of between 3 and 9 bytes referred to as 'packets'. Each packet comprises between 1 and 7 data bytes, followed by a 2 byte 'header' ('footer'?) containing the packet type, data length and protection code (checksum). There are 3 types of packet:

(i) MAIN (Type 0) This type of packet contains between 1 and 7 bytes of data for the main serial output port. Consecutive serial packets contain consecutive bytes from the serial data stream.

(ii) AUX (Type 1) This is similar to a MAIN packet, but contains data for the auxiliary serial output port.

(iii) TXCTL (Type 2) This contains the Combiner Source/Ident code and Splitter Address code as set up via the front panel, followed by a 16-bit TXCTRL word (received high byte first). A type 2 packet thus has a fixed data length of 4 bytes. The Source/Ident codes are numbered sequentially starting at 0 for BH01. The 25 BH Idents are numbered first, followed by 25 Idents for CF and so on. These are numbered in the same sequence as they appear in the menu lists. The destination codes are similarly numbered, starting at 0 for ALLS.

The formats of the packet data and header are summarised in Appendix B.

5.1.2. Packet Decoding

5.1.2.1. Establishing Frame Alignment

The packet sequence is not predictable at the Splitter, being determined by real-time events at the Combiner. The Splitter maintains a circular buffer containing the most recently received 32 NICAM 3 data bytes. Each time a new byte is received and added to the buffer, a sum and validity check are made to see whether the new byte completes a packet. If so, then that packet is decoded, and frame (packet) alignment is deemed to have been achieved. Otherwise, no further action is taken until the next NICAM 3 strobe pulse.

5.1.2.2. Maintaining Alignment

Once the first packet has been decoded, an additional validity check is made during subsequent packet checking; packets are accepted only if the start of each one immediately follows the end of the previous one. Since the maximum number of bytes in a packet is 9 (including the header), packet alignment is lost if more than this number of bytes has been received since the last valid packet, and the mode described in the previous section is resumed.

5.1.2.3. Serial Data Packets

Data bytes from serial data packets are placed, when the packets are decoded, in the Main and Auxiliary serial data queues. These are large (2 kbyte) circular 'FIFO' buffers, implemented as array variables and controlled by input and output pointer indices. They interface the packet data to the serial output ports, allowing for variable output baud rates and flow control.

5.1.2.4. TXCTRL Data Packets

If an apparently valid TXCTRL packet is decoded, its Combiner Source/Ident and Splitter Address codes are checked in the system control data block. If they are respectively valid and actionable, then the 16-bit TXCTRL word is output to the appropriate ports.

If the Combiner Source/Ident code is not valid, then the message 'IVID' is displayed and the WARNING LED is turned on. The fault condition is also flagged by setting D9 of the TX control output bits. Bits Ø and 8 are also set to logic 1. If the Splitter Address code is not actionable, then the packet is ignored.

5.1.3. Serial Outputs

A number of different events may indicate that a character can be sent from a serial queue to the output port. These include the transmitter buffer becoming empty, a new character being added to the queue, the arrival of an X-ON character, and a change in state of the DTR flow control input. In all cases, a central procedure is called which ascertains whether all the necessary conditions are met, and if so sends the next character.

5.1.4. NV RAM Management

The characteristics of the Splitter are controlled by the values of a number of 'system control variables' held in the main (volatile) RAM. When any of these variables is changed, a Cyclic Redundancy Check Code word is computed and stored with the system control block, allowing the integrity of the block to be continuously checked. Such checking occurs during normal operation of the Splitter, and any failure will cause the program to 'crash' in a controlled manner, allowing the system watchdog timer to reset the CPU.

Whenever the varlables are changed, two copies of the new working data block are made in the non-volatile RAM. These provide the initial settings of the working RAM variables following a system reset for whatever reason. The maintenance of 2 copies improves the chance of recovery from a failure occurring, for example, during the process of copying data lnto the non-volatile RAM.

5.1.5. Interactive Mode

The system tests the SELECT key continuously during normal operation, entering its interactive (menu) mode if it is pressed. Menu operations proceed in 'background' mode, ie, they are fully interruptible, and data processing continues under interrupt control.

A full description of the interactive mode has already been given (Operation section). The duration of each displayed message is controlled by the soft timer channels driven by CTC channel 3.

5.2. Design Overview

The Splitter software system may be split into 2 sub-systems; the handling of reai-time events which cause interrupts, and the 'background' tasks, including interactive (menu) operation, which are interruptible. Before these sub-systems can be used, various initialisation tasks are performed, which are described below under the heading 'module descriptions'.

5.2.1. Interrupt-Driven Software

When an event generates an interrupt request, and the CPU responds by entering the associated handier, further interrupts are disabled until the handler has finished executing and returned control to the background process. This single-level interrupt approach greatly simplifies the software design, although it does constrain the maximum time taken by interrupt handlers of low priority, to guarantee that a high priority event receives control wlthin an acceptable time. The following table summarises the response of the system to each interrupt-generating event, in descending order of priority.

Event	Response
NICAM strobe pulse	Read the next byte of data from the NICAM 3 Decoder, and apply the algorithm described above (Packet Decoding).
Clock tick (10 ms)	Increment all the soft timer variables.
Main serial port special receive condition	Read and discard the offending character, reset the SRC detector
Main serial port received character available	Read the character. If it is X-ON, then try to restart the main serial output stream. If X-OFF, then stop the stream.
Main serial port status change	Reset the status change detector. Try to start/continue the main serial output stream.
Main serial port transmit buffer empty	Cancel further interrupts for this event pending the next character transmission. Try to initiate this.
Aux serial port special receive condition	As for main port.
Aux serial port received character available	As for main port.
Aux serial port status change	As for main port.
Aux serial port transmit buffer empty	As for main port

The soft timer variable are 16-bit integers which may be set to zero and read (via dedicated procedures which locally disable interrupts) for such purposes as display duration timing.

The serial port special receive condition (SRC) arises from an input framing error or overrun, and should not normally occur. Received characters are buffered within the Z80-DART to a depth of 3 characters, to allow for a delay before interrupt service is granted.

5.2.2. Interruptible Software

The 'background' program continuously writes the most recently actioned Combiner Source/Ident code to the alphanumeric display, checks the system control variables CRC, and reads the state of the SELECT key. If the CRC check fails, it disables interrupts and halts the CPU to force a system reset. If SELECT is pressed, the menu driver is entered, allowing the operator to inspect and/or change the system control settings. The menu driver returns control to the background program when no front panel keys have been pressed for a preset time.

5.3. Coding Principles

5.3.1. Programming Tools

The firmware for the Splitter was developed under the VAX/VMS and CP/M operating systems, using PASCAL and Z80 Assembly Language. The front panel menu drivers were developed using the Whitesmiths native PASCAL compiler under VAX/VMS, and tested with a simulated front panel on a VT100 terminal. The remaining software was subsequently written under VAX/VMS and compiled/assembled under CP/M, using the Digital Research PASCAL/MT+ compiler and Microsoft M80 Macro Assembler. The modules were linked under CP/M by the Digital Research LINKMT linker. Initial testing in the Splitter hardware was carried out under the ADZE Interactive Monitor (AIM) with the program in RAM, before transfer to stand-alone ROM code.

The proportion of Assembly Language code has been kept to a minimum, but Assembly Language has always been used in preference to 'non-standard' PASCAL extensions. PASCAL and Assembly code are always in separate modules, without recourse to the INLINE feature of PASCAL/MT+.

5.3.2. Module Conventions

5.3.2.1. Procedure and Function Arguments

The convention adopted for all inter-module procedure calls is that used by PASCAL/MT+. This convention is relaxed for intra-module language calls.

Arguments are passed as 16-bit words on the stack. In the case of 8-bit arguments, the high byte is set to zero. A 16-bit absolute address is used to pass arguments by reference. PASCAL calls push the arguments onto the stack in the order in which they are written (leftmost first), followed by the return address.

Called procedures are responsible for removing the return address and all arguments from the stack. A function returns its value as a 16-bit word at the top of the stack.

5.3.2.2. Use of Z80 Registers

Registers are not generally preserved across procedure calls. All the general registers are available for use by a procedure, but interruptible procedures must not use IX, IY, or the alternate register set since these are not preserved across interrupts. Code generated by PASCAL/MT+ uses only the AF, HL, DE and BC registers.

5.3.2.3. Interrupt Status

In general, background code runs with interrupts enabled, interrupt handlers run with interrupts disabled and enable interrupts on completion. Code is not generally re-entrant; the exception is the procedures which report faults and warnings on the alphanumeric display. These may be called by both background and interrupt service code, and should therefore be modified with caution.

5.4. Environment

5.4.1. Memory Addresses

Address Range	Memory Type	Access
0000 .. 3FFF	Program EPROM	Read Only
8000 .. 9FFF	Non-volatile RAM	Read Only (normal) Read/Write (PROGRAM key pressed)
C000 .. DFFF	RAM	Read/Write

5.4.2. I/O Port Addresses

Address	I/O	Description
00	O	Tx Control Data, low byte
20	O	Tx Control, high byte
40	I	Auxiliary fault indication (low bit only)
60	I	Signalling byte from NICAM 3 Decoder
80	O	Fault indication (low bit only)
A0		DART channel 0 data
A1		DART channel 0 control
A2		DART channel 1 data
A3		DART channel 1 control
C0		CTC channel 0
C1		CTC channel 1
C2		CTC channel 2
C3		CTC channel 3
E0	O	Alpha display character 0 (rightmost)
E1	O	Alpha display character 1
E2	O	Alpha display character 2
E3	O	Alpha display character 3 (leftmost)
F4	I	Front panel switch states
F8	O	Front panel LED drives
FF	O	Watchdog timer reset

5.5. Program Synopsis

The details in this section are intended mainly to help you to find your way round the actual code, by summarising the functions of all the globally accessible procedures. Details are valid for all modules last revised before March 1991.

Program modules and component procedures are described here in alphanumeric order. Embedded procedure calls are named only if the name appears in the cross-reference list (ie, it is separately described here). Every program module is defined by two files; one contains the actual source code ('implementation module'), the other contains a set of definitions ('definition module') for this code, suitable for automatic inclusion in those other modules which use the code.

5.5.1. Module List

Modules should be linked in the following order:

SPKNL
SPIO
SPNVR
SPINTSRV
SPLITTER
SPPANEL
SPMENU
SPTEXT
SPVAR
CONVERT
B4LIB
PASLIB
AFTLIB

All object modules sourced in Assembly Language should be renamed to conform with the .ERL file extension required by LINKMT. PASLIB is the searchable PASCAL/MT+ run-time support library, which should be suffixed /S in the link list to force extraction of required modules only. Relocation bases are 0000 for program code, C000 for data.

5.5.2. Procedure Cross-Reference

(This list contains only globally accessible procedures and functions.)

Procedure	Module
AFEED	SPINTSRV
AHTXEN	SPKNL
ARX	SPINTSRV
ASEND	SPKNL
CALCRC	SPNVR
CALTXC	SPKNL
CHKCRC	SPNVR
CLEAR	SPIO
CLRDEB	SPPANEL
CONVT	CONVERT
COPY	SPNVR
CRASH	SPNVR
CTCIO	SPKNL
CTCI3	SPKNL
DISINT	SPKNL
DPYCHR	SPIO
DPYCURR	SPPANEL
DPYNORM	SPPANEL
ENINT	SPKNL
EXPLAIN	SPMENU
FAULT	SPPANEL
FOCOFF	SPKNL
FOCON	SPKNL
INIT	SPKNL
LEDDRV	SPIO

MFEED	SPINTSRV
MHTXEN	SPKNL
MRX	SPINTSRV
MSEND	SPKNL
NEXTITEM	SPMENU
PICKITEM	SPMENU
PICKSETTING	SPMENU
PRGDEB	SPPANEL
PROG	SPIO
QINIT	SPINTSRV
RESINT	SPKNL
REVDEB	SPPANEL
REVIEW	SPIO
RXO	SPKNL
RX1	SPKNL
SELDEB	SPPANEL
SELECT	SPIO
SETBR1	SPKNL
SETBR2	SPKNL
SETTXC	SPKNL
SETZERO	SPKNL
SPECO	SPKNL
SPEC1	SPKNL
SPMAIN	SPLITTER
STATO	SPKNL
STAT1	SPKNL
STROBE	SPINTSRV
TEXTDEFINE	SPTEXT
TICK	SPINTSRV
TIMER	SPKNL
TXO	SPKNL
TX1	SPKNL
VALID	SPKNL
WARN	SPPANEL

5.5.3. Entry Points

Event	Entry Point
Reset	SPKNL (beginning of module)
NICAM strobe pulse	CTCIO
Clock tick (10 ms)	CTCI3
Main serial SRC	SPECO
Main serial receive	RXO
Main serial status	STATO
Main serial TX ready	TXO
Aux serial SRC	SPEC1
Aux serial receive	RX1
Aux serial status	STAT1
Aux serial TX ready	TX1

5.5.4. Module CONVERT (MACRO-80 Source)

5.5.4.1. CONVT (Function)

Returns its argument unchanged. This function may, with care, be declared in any module to convert between compatible 16-bit data types for which no built-in conversion exists (cf, the CHR function).

5.5.5. Module SPINTSRV (PASCAL/MT+ Source)

This module contains interrupt service routines which are mostly called by the interrupt entry code in module SPKNL. Associated general purpose procedures are also in this module if they share data with the service routines or they are sensitive to the CPU status.

5.5.5.1. AFEED

IF (aux serial transmitter soft enable is TRUE) AND (AHTXEN is TRUE) AND (aux serial queue contains some data) THEN (call FROMQA to get the next byte. Call ASEND to send it).

5.5.5.2. ARX

IF argument character is X-ON THEN set aux serial transmitter soft enable to TRUE (enabled) and call AFEED. IF argument is X-OFF THEN set aux transmitter soft enable to FALSE (disabled).

5.5.5.3. MFEED

IF (main serial transmitter soft enable is TRUE) AND (MHTXEN is TRUE) AND (main serial queue contains some data) THEN (call FROMQM to get the next byte. Call MSEND to send it).

5.5.5.4. MRX

IF argument character is X-ON THEN set main serial transmitter soft enable to TRUE (enable) and call MFEED. IF argument is X-OFF THEN set main serial transmitter soft enable to FALSE (disabled).

5.5.5.5. QINIT

Set input and output pointers of both serial data queues to zero (le, queues empty). Initialise soft transmltter enabie switches to TRUE (enabled). Initialise packet decoding variables for a clean start in unlocked mode.

5.5.5.6. STROBE

Store the argument in the next stream buffer location. Cali VALID. IF a new packet is complete THEN (IF the new packet 'butts on' to the previous packet OR the packet structure is uniocked THEN decode the new packet and put the data in the main queue, aux queue or transmitter control outputs (call DECODE, which also cails CONVT and SETTXC, sets the background status display string and resets the TXCTRL activity timeout if a TXCTRL packet is actioned). Set mode to locked). Increment stream buffer pointer. Increment count of bytes since last packet was decoded. IF more bytes than the maximum per packet have been processed THEN set mode to unlocked.

5.5.5.7. TICK

Increment each of the 4 software timer variables.

5.5.6. Module SPIO (MACRO-80 Source)

This module contains procedures which access the front panel components.

5.5.6.1. CLEAR (Function)

Read the front panel switch port. Return the state of the CLEAR button as a boolean value.

5.5.6.2. DPYCHR

Use the character position argument to select an alphanumeric character output port. Output the ASCII character argument to this port.

5.5.6.3. LEDDRV

Combine the 4 argument values to form a byte controlling the LED colour and the state of the 3 front panel LEDs. Output this byte to the LED port.

5.5.6.4. SELECT (Function)

Read the front panel switch port. Return the state of the SELECT button as a boolean value.

5.5.6.5. REVIEW (Function)

Read the front panel switch port. Return the state of the REVIEW button as a boolean vaiue.

5.5.6.6. PROG (Function)

Read the front panel switch port. Return the state of the PROGRAM button as a boolean value.

5.5.7. Module SPKNL (MACRO-80 Source)

This module contains the code associated with system reset, device initialisation and interrupt entries. Entry on system reset initialises the stack pointer and jumps to SPMAIN. Interrupt entry points are inciuded in this description.

5.5.7.1. AHTXEN (Function)

Read DART 1 control register 0. Return TRUE if and only if CTS is active and TX buffer is empty.

5.5.7.2. ASEND

Output the argument to DART channel 1.

5.5.7.3. CTCIO (CTC Ch 0 Interrupt)

Save context. Call TICK. IF integrity pattern is OK THEN reset watchdog timer. Restore context. Re-enable interrupts.

5.5.7.4. CTCI3 (CTC Ch 3 Interrupt)

Save context. Input data from NICAM. Reset timer channel to trigger on next strobe pulse. Call STROBE with data as argument. Restore context. Re-enable interrupts.

5.5.7.5. DISINT

Record Interrupt status. Disable interrupts

5.5.7.6. ENINT

Enable interrupts.

5.5.7.7. FOCOFF

Switch off the Fault open collector output.

5.5.7.8. FOCON

Switch on the Fault open collector output.

5.5.7.9. INIT

Store integrity check pattern in RAM. Initialise I-register and set interrupt mode 2. Set CTC chan 0 to interrupt to CTCI0 every 10 ms. Set CTC chan 3 to interrupt to CTCI3 100 µs after the next NICAM strobe pulse. Initialise DART channels. Set up DART channel 0 to interrupt to RX0, TX0, SPEC0, or STAT0 on received character, transmitter ready, special receive condition (eg, over-run), status (CTS transition) respectively. Set up DART channel 1 similarly (RX1, TX1, SPEC1, STAT1). Enable interrupts.

5.5.7.10. MHTXEN (Function)

Read DART channel 0 control register 0. Return TRUE if and only if CTS is active and TX buffer is empty.

5.5.7.11. MSEND

Output the argument to DART channel 0.

5.5.7.12. RESINT

Restore interrupt status prior to last DISINT call.

5.5.7.13. RX0
(DART Channel 0 Character Received Interrupt)

Save context. Input the character. Call MRX with character as argument. Restore context. Re-enable interrupts.

5.5.7.14. RX1
(DART Channel 1 Character Received Interrupt)

Save context. Input the character. Call ARX with character as argument. Restore context. Re-enable interrupts.

5.5.7.15. SETBR1

Disable interrupts. Set DART channel 1 baud rate according to the integer argument. Enable interrupts.

5.5.7.16. SETBR2

Disable interrupts. Set DART channel 2 baud rate according to the integer argument. Enable interrupts.

5.5.7.17. CALTXC

Calculate TXC value from buffer content and two supplied masks.

5.5.7.18. SETTXC

Recover the two integer arguments. Output the iow byte of each to the two transmitter control ports.

5.5.7.19. SETZERO

Disable interrupts. Set one of the 4 software timer variables to zero, as specified by the argument. Reset interrupts.

5.5.7.20. SPEC0
(DART Chan 0 Special Receive Interrupt)

Save context. Reset interruptlng condition. Read and discard the character. Restore context. Re-enable interrupts.

5.5.7.2i. SPEC1
(DART Chan 1 special Receive Interrupt)

Save context. Reset interrupting condition. Read and discard the character. Restore context. Re-enable interrupts.

5.5.7.22. STAT0
(DART Channel 0 Status Change Interrupt)

Save context. Call MFEED. Clear the interrupting condition. Restore context. Re-enable interrupts.

5.5.7.23. STAT1
(DART Channel 1 Status Change Interrupt)

Save context. Call AFEED. Clear the interrupting condition. Restore context. Re-enable interrupts.

5.5.7.24. TIMER (Function)

Disable interrupts. Read and return the value of the software timer variable specified by the argument. Reset interrupts.

5.5.7.25. TX0
(DART Tx Buffer 0 Ready Interrupt)

Save context. Cancei further TX0 interrupts pending next character for transmission. Call MFEED. Restore context. Re-enable interrupts.

5.5.7.26. TX1

(DART Tx Buffer 1 Ready Interrupt)

Save context. Cancel further TX1 interrupts pending next character for transmission. Call AFEED. Restore context. Re-enable interrupts.

5.5.7.27. VALID (Function)

Recover two arguments giving the stream buffer start address, and the offset of the most recently received byte. Check sum, packet type and size for validity. Check TXCTRL packet addressing codes for valid range. IF valid THEN transfer the packet data, type and size to the variables whose addresses are the remaining 3 arguments, return TRUE, ELSE return FALSE.

5.5.8. Module SPLITTER (PASCAL/MT+ Source)

This module functions as the 'main program'. It will eventually perform routine 'background' tasks (eg, system testing), and control operator access. All other system activity is initiated by interrupts.

5.5.8.1. SPMAIN

Call SETTXC with 'all ones' pattern as argument. Clear fault and warning flags. Set background display string to '----'. IF working data is not valid (call CHKCRC) AND one of the non-volatile copies is OK THEN call COPY to load the NV data, ELSE initialise all the working data and text arrays to default settings (call TEXTDEFINE). Call QINIT. Call INIT. Reset the TXCTRL timeout counter. Set serial baud rates.

Enter a 'forever' loop which displays the default message (Source/Ident received or hex TXCTRL data). If data has timed out (ie, no TX control bits received) then display NTXC message and set to logic '1' bits D0 and D8 of the TX control bits, all other bits being latched.

Call CHKCRC (if this fails, call CRASH), and SELDEB in turn, until SELDEB returns TRUE signifying operator intervention. Call PICKITEM, EXPLAIN and PICKSETTING to allow operator to inspect and/or change a system control item, then resume the the 'forever' loop.

5.5.9. Module SPMENU (PASCAL/MT+ Source)

This module contains the procedures which interact with the operator for system control setting.

5.5.9.1. EXPLAIN

Display a 3-word explanation of the currently active system control item. Each word is displayed for the same pre-determined time. Abort the procedure if the SELECT or REVIEW button is pressed (call SELDEB and REVDEB). Calls SETZERO and TIMER (Channel DWELL) to control display timing, DPYNORM to display each word.

5.5.9.2. NEXTITEM

Increment the global variable ITEM, which points to the current system control item under review. IF end of list is reached THEN wrap to start.

5.5.9.3. PICKITEM

Allow the operator to choose an item to examine. Each time he pushes the SELECT button (call SELDEB), display the next item. If he holds the button down, start auto-repeatlng items, increasing the auto-repeat speed to a pre-determined maxlmum. Exit when SELECT has been released for a pre-determined time, or if the REVIEW button is pressed (call REVDEB).

DYNORM is called to display the item text. SETZERO and TIMER (using channel DWELL) are called to control display timing.

5.5.9.4. PICKSETTING

Allow the operator to review possible settings for the current ltem. Each time he pushes the REVIEW button (call REVDEB), display the next setting text. Calls DPYNORM or DPYCURR according to non-current/current setting being displayed. If operator holds the button down, start auto-repeating settings, increasing the auto-repeat speed to a pre-determined maximum.

IF he presses PROGRAM (call PRGDEB), THEN (change the system controi setting to match the currently displayed settlng. Call CALCRC. Copy working data to both NV RAM areas (call COPY). Check the copy CRCs. (Call CHKCRC.) If an error exlsts then call WARN with the message 'REPT'. Call DPYCURR to re-display the setting as current). Exit when REVIEW and PROGRAM have been released for a pre-determined time, or SELECT button is pressed (call SELDEB).

SETZERO and TIMER (uslng channel DWELL) are called to control display timlng.

5.5.10. Module SPNVR (MACRO-80 Source)

This module contains the procedures which generate and check REDCODE CRCs and move data between working RAM and NV RAM.

5.5.10.1. CALCRC (Functlon)

Compute size of data area. Compute and return REDCODE over working data.

5.5.10.2. CHKCRC (Function)

Compute size of data area. Select start address accordlng to the argument. Compute REDCODE over the area. Compare with stored REDCODE after data. Return TRUE if codes agree, FALSE otherwise.

5.5.10.3. COPY

Compute size of data area. Select source and destination start addresses accordlng to the two arguments. Copy data and REDCODE from source to destlnation.

5.5.10.4. CRASH

Dlsable interrupts, halt CPU.

5.5.11. Module SPPANEL (PASCAL/MT+ Source)

This module contains procedures which allow the front panel to be accessed at a hlgher level than the prlmitive procedures in module SPIO.

5.5.11.1. CLRDEB (Functlon)

Call CLEAR repeatedly untll the same value has been returned a pre-determined number of times. Return this value.

5.5.11.2. DPYCURR

IF fault or warning flag is set THEN wait a pre-determined time or until CLEAR is pressed (call CLRDEB) as appropriate, clearing the flag. (Calls SETZERO and TIMER using channel ALERT.) Call FOCON. Set LEDs to indicate CURRENT status (call LEDDRV) and display the argument message (call DPYCHR).

5.5.11.3. DPYNORM

IF fault or warning flag is set THEN wait a pre-determined time or until CLEAR is pressed (call CLRDEB) as appropriate, clearing the flag. (Calls SETZERO and TIMER using channel ALERT.) Call FOCON. Set LEDs to indicate NORMAL status (call LEDDRV) and display the argument message (call DPYCHR).

5.5.11.4. FAULT

IF no fault currently displayed, AND CLEAR not pressed THEN (Set the front panel LEDs to indicate a fault (call LEDDRV). Display the argument message (call DPYCHR). Call FOCOFF. Set fault flag).

5.5.11.5. PRGDEB (Function)

Call PROG repeatedly until the same value has been returned a pre-determlned number of times. Return this value.

5.5.11.6. REVDEB (Function)

Call REVIEW repeatedly until the same value has been returned a pre-determined number of times. Return this value.

5.5.11.7. SELDEB (Function)

Call SELECT repeatedly until the same value has been returned a pre-determined number of times. Return this value.

5.5.11.8. WARN

IF fault flag is not set AND CLEAR is not pressed, THEN (set the front panel LEDs to indlcate a warning (call LEDDRV). Display the argument message (call DPYCHR). Call FOCON. Set warning flag).

5.5.12. Module SPTEXT (PASCAL/MT+ Source)

This module defines all text associated with the operator menu.

5.5.12.1. TEXTDEFINE

Set up all the text and class fields for the menu options, explanations and setting options.

6. MAINTENANCE

IMPORTANT NOTE: The ADZE 2 module must be isolated for testing by the removal of the ribbon jumper between PLB and PLE. (This isolates everything except the power supply to the ADZE 2 module.)

The module may then be tested in accordance with DDHB 6.267(85). Note that the power consumption will be higher than normal, because the custom half of the PCB is still connected to the supply.

The reminder of this section describes testing of the rear half of the Splitter card, assuming a correctly functioning ADZE 2 module.

6.1. Test Apparatus Required

Stabilised power supply, 5 V limited to 1.5 A
Dual-trace Oscilloscope, 25 MHz bandwidth
Signature Analyser, Hewlett Packard 5004A or similar
Test jigs to DSK26740 A3
EPROM type 27128 programmed to P4605

Throughout the test sequence the front panel display '> ' is a prompt inviting the operator to press PROGRAM to continue with the next test.

6.2. Power Connection

(a) Plug the unit into the test jig and switch on the supply. Measure the current consumption.

(b) Current should be in the range of 600 - 800 mA.

(c) If less, check the distribution of both +5 V and ground to all ICs. If more, look for short circuits between +5 V and ground, or signs of overheating.

6.3. PROM, RAM and Alphanumeric Display

(a) Remove P5992 (or P5993) and replace with P4605 (IC6).

Upon switch-on the green CPU LED on the front panel should flash continuously with a period of about 1 sec. Press PROGRAM and hold down for one second. A checksum test will be carried out on the PROM followed by a full read/write rest on the RAM.

The test sequence will only start if these initial tests have been passed.

(b) (i) The CPU LED should stay ON
(ii) The alphanumeric display should read '0000' for 2 secs then '****' for 2 secs followed by '> '

(c) If the CPU LED continues to flash, check:

(i) That LK1 - LK3 are correctly configured
(ii) The wiring from LK2 to S4
(iii) That IC6 - IC8 are correctly inserted into their sockets
(iv) The redcode of IC6 (this should be 717C)

If the CPU LED stays on but reverts back to flashing once the prompt is displayed, then suspect IC20 and the 40-way ribbon connector between PLB and PLE.

If the alphanumeric display is wrong check that it has been inserted into its holder correctly. If the display is blank (and hot) it is likely to be wrongly orientated.

6.4. Front Panel Pushbuttons

(a) Press PROGRAM to continue.

Press each pushbutton in turn (starting from the top) when prompted by the display. For example, in the first instance the display will read 'PRES' 'CLR '.

(b) As each button is pressed the display should read ' OK ' before inviting you to press the next button. When all buttons have been tested the '> ' prompt should be displayed.

(c) If there is no response when a button is pressed check that the switch has been inserted into the PCB the correct way round. Note that a display showing '????' means that the wrong button has been pressed.

6.5. Front Panel LEDs

(a) Press PROGRAM to continue.

(b) The LEDs should light sequentially from top to bottom; first with the colour RED, followed by YELLOW, and finally GREEN. The alphanumeric display should display the name of the current colour.

(c) If two or more LEDs light simultaneously check for solder bridges on both PCBs especially in the vicinity of PLC and 2SK1.

If the colour of any LED does not match the current colour shown in the display check:

(i) The orientation of the LED
(ii) The values of R1 - R5 on PCB No.2

6.6. Transmitter Control Outputs

(a) Press PROGRAM to continue.

(b) The LEDs D0 - D15 on the test jig should light one at a time, starting with D0 and ending with D15. The LED currently lit should be shown on the front panel display.

(c) If one or more outputs fail, check that WRREQ pulses reach IC23 p 11 and IC24 p11, and that these ICs are being enabled (pin 1). Check also IC27 - IC29.

Note that these outputs are open-collector outputs with pull-up resistors inside the test jig.

6.7. Fault Output

(a) Press PROGRAM to continue.

(b) Following the name of the test, the red FAULT LED on the test jig should light for approximately 3 seconds. During this time the front panel display should read 'F ON'. The LED should then go out with the message 'FOFF' displayed for a further 3 seconds.

(c) If the FAULT output is not toggled suspect IC22 or IC27. Check that WRREQ pulses reach IC22 p11 and that enable pulses reach p1.

Note that this output is also open-collector with its pull-up resistor within the test jig.

6.8. Aux Fault Input

(a) Press PROGRAM to continue.

(b) The front panel display should read ' OK '. Note that the FAULT LED on the test jig will flash momentarily.

(c) If 'FAIL' is displayed check that IC33 is plugged into its socket correctly. Check that pins 1 and 8 of IC33 carry +5 V and that R20 is 1 kΩ. Also check that RDREQ pulses appear on IC26 p1 and enable pulses on p19.

With the unit displaying the FAIL condition it will remain in this state until the power to it is interrupted.

6.9. NICAM Data Input

(a) Press PROGRAM to continue.

(b) Each NICAM data bit will be toggled in turn, and if all eight bits are received correctly then ' OK ' should be displayed. Since the transmitter control bits are used as a source of dummy NICAM data, the LEDs labelled D0 - D7 on the test jig will show a burst of activity during the test.

(c) If 'FAIL' is displayed check that IC34 - IC37 carry +5 V on pins 1, 4 and 8. In this condition all but one of the LEDs D0 - D7 will be on. The LED which is OFF corresponds to the failed data bit, and so indicates which of IC34 - IC37 should be checked first.

Interrupt the power supply to remove the FAIL condition. Check that during this test there are RDREQ pulses on IC25 p1 and enable pulses on p19.

6.10. Hard Handshake Inputs

(a) Press PROGRAM to continue.

(b) (i) Main Channel

With the Hard H/S switch on the test jig in the HI position the display should read 'M HI'. With the switch in the LO position the display should read 'M LO'.

Press PROGRAM.

(ii) Aux Channel

With the switch in the HI position the display should read 'A HI'. With the switch in the LO position the display should read 'A LO'.

Make sure that the switch is left in the HI position before continuing with the next test.

(c) If the LEDs do not respond to the Hard H/S switch check that the RS232 level changes on PLA4 (main) and PLA10 (aux). Suspect IC30 (main) or IC31 (aux).

Note that the RS232 levels for both main and aux channels are provided by IC30.

6.11. Serial Data Channels

(a) Press PROGRAM to continue.

(b) (i) Main Channel

The display should read ' OK '. Press PROGRAM.

(ii) Aux Channel

The display should read ' OK '. The end of the test sequence is marked by a flashing 'END' message in the display. If it is required to return to the beginning of the sequence, this can be done by pressing CLEAR.

(c) If 'FAIL' is displayed, restart the sequence by interrupting the power supply and check that during this test a burst of RS232 data reaches PLA3 (main) or PLA9 (aux) whilst the front panel display is blank. This should appear simultaneously on IC30 p2 (main) or IC31 p2 (aux). Check that IC21 is receiving positive going timing pulses from the CTC on pins 13, 14 and 27. These should be 0.2 microsecs, ±0.05 microsecs, wide with a repetition rate of 6.5 microsecs, ±1 microsec.

This completes the Test Procedure. Replace P4605 with P5992 or P5993.

6.12. Software Maintenance

You should read and understand the entire section on software, and study the program modules themselves before attempting any software modifications; despite its physical size, this is not a trivial system!

The master files are held on the same magtape volume as the DSR master for this handbook. The version history of each module must be updated with full details of any permanent changes, as must the descriptions in this handbook. Also remember that every source module has a corresponding definition module which must be kept in agreement.

APPENDIX A: DISPLAY MESSAGES

Status message (displayed during normal operation):

----	No TX control packets received since reset
xxxx	Source/Ident code of last actioned TX control packet (see menu options BH01 .. BE00)

Fault messages (accompanied by open-collector signal):

NVR	Non-Volatile RAM (unable to recover correct settings - defaults used)
MOFL	Main queue Over-Flow (RDS assembler is not accepting data - some serial data lost)
AOFL	Aux queue Over-Flow
IVID	InValid IDent received on TX control packet

Warning messages:

REPT	REPeaT (when using the PROGRAM key, settings were not copied successfully to non-volatile RAM - try again)

Menu messages:

Select	Explanation		Review/Program
BR1	RDS BAUD RATE		300/ 600/1200/2400/4800/9600
BR2	AUX BAUD RATE		300/ 600/1200/2400/4800/9600
LEDS	COLS FROM TOP	*	RRG+/RYG+/RGG+/YYG+/YGG+/RRR-/YYY-/GGG-
SDPY	MESS DISP TIME	**	INST/FHWI/HOLD
NDPY	NORM OPER DISP		NAME/DATA
ALLS	CTRL ADRS ALLS		IGNR/ACT
ALLT	CTRL ADRS ALLT		IGNR/ACT
ENGD	CTRL ADRS ENGD		IGNR/ACT
WALS	CTRL ADRS WALS		IGNR/ACT
SCOT	CTRL ADRS SCOT		IGNR/ACT
ULST	CTRL ADRS ULST		IGNR/ACT
GLAS	CTRL ADRS GLAS		IGNR/ACT

* + means active on
- means active off

** FWHI = Faults Hold, Warnings Inst

With the following menu messages, pressing PROGRAM will toggle the CURRENT LED. When this LED is ON then the displayed 'service' is selected.

Note that in the version installed at transmitter sites, BH00 can not be de-selected.

Select	Explanation	Review
BH	SRCE CODE BH01	BH01/BH02/BH03/BH04/BH05/BH06/BH07/ BH08/BH09/BH10/BH11/BH12/BH13/BH14/ BH15/BH16/BH17/BH18/BH19/BH20/BH21/ BH22/BH23/BH24/BH00 (ZZ00)
CF	SRCE CODE CF01	CF01/CF02/CF03/CF04/CF05/CF06/CF07/ CF08/CF09/CF10/CF11/CF12/CF13/CF14/ CF15/CF16/CF17/CF18/CF19/CF20/CF21/ CF22/CF23/CF24/CF00
FI	SRCE CODE FI01	FI01/FI02/FI03/FI04/FI05/FI06/FI07/ FI08/FI09/FI10/FI11/FI12/FI13/FI14/ FI15/FI16/FI17/FI18/FI19/FI20/FI21/ FI22/FI23/FI24/FI00
GW	SRCE CODE GW01	GW01/GW02/GW03/GW04/GW05/GW06/GW07/ GW08/GW09/GW10/GW11/GW12/GW13/GW14/ GW15/GW16/GW17/GW18/GW19/GW20/GW21/ GW22/GW23/GW24/GW00
RK	SRCE CODE RK01	RK01/RK02/RK03/RK04/RK05/RK06/RK07/ RK08/RK09/RK10/RK11/RK12/RK13/RK14/ RK15/RK16/RK17/RK18/RK19/RK20/RK21/ RK22/RK23/RK24/RK00
VW	SRCE CODE WV01	VW01/VW02/VW03/VW04/VW05/VW06/VW07/ VW08/VW09/VW10/VW11/VW12/VW13/VW14/ VW15/VW16/VW17/VW18/VW19/VW20/VW21/ VW22/VW23/VW24/VW00
GN	SRCE CODE GN01	GN01/GN02/GN03/GN04/GN05/GN06/GN07/ GN08/GN09/GN10/GN11/GN12/GN13/GN14/ GN15/GN16/GN17/GN18/GN19/GN20/GN21/ GN22/GN23/GN24/GN00
AL	SRCE CODE AL01	AL01/AL02/AL03/AL04/AL05/AL06/AL07/ AL08/AL09/AL10/AL11/AL12/AL13/AL14/ AL15/AL16/AL17/AL18/AL19/AL20/AL21/ AL22/AL23/AL24/AL00
BE	SRCE CODE BE01	BE01/BE02/BE03/BE04/BE05/BE06/BE07/ BE08/BE09/BE10/BE11/BE12/BE13/BE14/ BE15/BE16/BE17/BE18/BE19/BE20/BE21/ BE22/BE23/BE24/BE00

APPENDIX B: PACKET FORMAT

Byte 1	⟨Packet data⟩	
. . .	. . .	
Byte N	⟨Packet data⟩	
Byte N+1	Bits 7 .. 5	⟨Checksum bits 10 .. 8⟩
	Bits 4 .. 3	⟨Packet type⟩
	Bits 2 .. 0	⟨Data length, N⟩
Byte N+2	⟨Checksum bits 7 .. 0⟩	

Notes

(i) Checksum is the binary sum of the N data bytes and byte N+1, with the checksum field of the latter set to zero.

(ii) Main Serial Data packets (type 0) have data length N in the range 1 .. 7. Data from consecutive main serial packets constitute a transparent stream of bytes.

(iii) Auxiliary Serial Data packets (type 1) are similar to Main serial packets.

(iv) Transmitter Control Data packets (type 2) have N=4 and a fixed data byte format:

Byte 1	⟨Combiner Source/Ident Code⟩
Byte 2	⟨Splitter Address Code⟩
Byte 3	⟨TXCTRL Data High Byte⟩
Byte 4	⟨TXCTRL Data Low Byte⟩

Source/Ident and Address Codes start at zero, and are numbered in the same sequence as the options displayed in the set-up menu.

(v) Packet type 3 is not used.

IC CIRCUIT REFERENCE	TYPE	SUPPLY CONNECTIONS		
		+5V	0V	-5V
IC 1	LS14	14	7	
IC11	LS08	14	7	
IC16	LS32	14	7	

PLD
SA test points
clock
clock
start stop
ground
PLB (see note)

IC1a IC1b IC1c IC1d IC1e
IC2a LS74A
IC3 MC74HC4040
IC4 MC74HC4040
LK4 1 SEC 1/2 1/4 1/8
XL1 9·83MHz
C1 60p
C2 390p
C3 100p
C4 33p
C5 33p
C21 330nF
C6–C19 100n
C20 47
R1 12k
R2 15k
R3 1k
R4 7·5k
R5 220
R6 1·2k
R7 22
R8 1k
R9 330
R10 1k
R11 1k
R12 1k
R13 4×330
R14 4×330
R15 8×1k
R16 22k
TR1 BC109
TR2 2N3906
4·915MHz
watchdog reset
CPU normal
PLC

MI
NMI
INT
RESET
CK
WAIT

IC5 Z80B-CPU
IC6 27128N 0000–7FFF
IC7 5565PL/15 8000–BFFF
IC8 5565PL/15 C000–FFFF
LK1
LK2 10k
LK3

port group decoder
IC12 LS138
CO–DF
A0–BF
80–9F
60–7F
40–5F
20–3F
00–1F
port group decodes

address buffer
IC15 LS541

LED output port
IC17 LS273
LED outputs

switch input port
IC18 LS541
switch inputs

IC19 NM232CD
SKA
RS232

Memory address decoder
IC10a LS139
IC11a

data bus buffer
IC9 LS245

write-only gate
IC10b LS139
internal port decoder
IC13 LS138
MSB
LSB
data bus
port group decodes
F0–F3
EC–EF
E8–EB
E4–E7
E0–E3
FC–FF
F8–FB
F4–F7
E0–FF decode

IC16a IC16b IC16c IC16d
mem RD
mem WR
10 WR
10 RD
IC14 LS139
IC11b
4 INT ACK
EXTL RD

WRREQ
RDREQ
IORQ
A1
A0

SCALE :- 0

Parts list:-D60163A4

THIRD ANGLE PROJECTION
ORIGINAL FRAME SIZE 674mm x 421mm
CHANGE
A 15-3-86
B 13-11-86
C L1-2 87

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(ADAPTABLE Z80 HALF CARD (A02E) MK II)

CD4S/18
NICAM DATA COMBINER CIRCUIT

All dimensions in millimetres unless otherwise stated.
Normal tolerances:
no decimal place ± 1·0 mm unless
one decimal place ± 0·2 mm otherwise
two decimal places ± 0·01 mm stated

DRN. LL.
TCD.
CKD.
APPD. JR

DESIGNS DEPARTMENT
D60162A1
Sheet 1 of 2 sheets

D60162A1

Interface to ADZE-2 module

PLE

CK 4
INT 5
PORT decode A0-BF 10
Reset 6
MI 8
PORT decode C0-DE 9
A1 20
A0 21
IORQ 34
RD 36

IC20 Z80B CTC
IC21 Z80B DART

RS232C Interface +5V — IC29 NM232CD — Main
RS232C Interface +5V — IC30 NM232CD — Aux

PLA
5 RS232 High out
2 H/S (Soft)
3 Data
4 H/S (Hard)
6 RS232 Low out
7 Signal earth
8 H/S (Soft)
9 Data
10 H/S (Hard)
11 Signal earth

Note: All PLA pins except PLA26 & PLA27 are connected on both sides of the board (e.g. PLA/17 = PLA/17 C & W)

D7 23
D6 24
D5 25
D4 26
D3 27
D2 28
D1 29
D0 30
WRREQ 35
RDREQ 37

IC22 LS377 Latches
IC23 LS377 Latches
IC24 LS377 Latches
IC25 LS541 3-state gates
IC26 LS541 3-state gates

PORT decode 80-9F 11
PORT decode 00-1F 15
PORT decode 20-3F 14
PORT decode 60-7F 12
PORT decode 40-5F 13

Opto-isolators

R17 1k
R18 470
R19 8x 1k
R20 1k
R23 3k
R21 4x2·2k
R22 4x2·2k

IC32 HCPL 2630
IC33 HCPL 2731
IC34 HCPL 2731
IC35 HCPL 2731
IC36 HCPL 2731
IC37 HCPL 2731

PLA 26W Opto ISO common
PLA 26C Aux fault
PLA 12 D7
PLA 13 D6
PLA 14 D5
PLA 15 D4
PLA 16 D3
PLA 17 D2
PLA 18 D1
PLA 19 D0
NICAM data in
PLA 20 Opto ISO common

PLA / PLB
Distributed decoupling 10 capacitors all 100n
C22 100n
C31 100n
C32 100n
C33
C37 5 capacitors all 100n distributed decoupling (i.e. 1 per device)

IC27 7407
IC28 7407
IC29 7407
Open collector drivers

Chassis

Opto ISO common 22
NICAM strobe 21
Signal earth 27W
Fault 27C
Signal earth 47
PLA D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
16 bit data out

D60162A1

SCALE — 0

Parts List D60163A4

THIRD ANGLE PROJECTION
ORIGINAL FRAME SIZE 574mm x 821mm
CHANGE SS 21/3/86 B 13-11-86 C 4-2-87

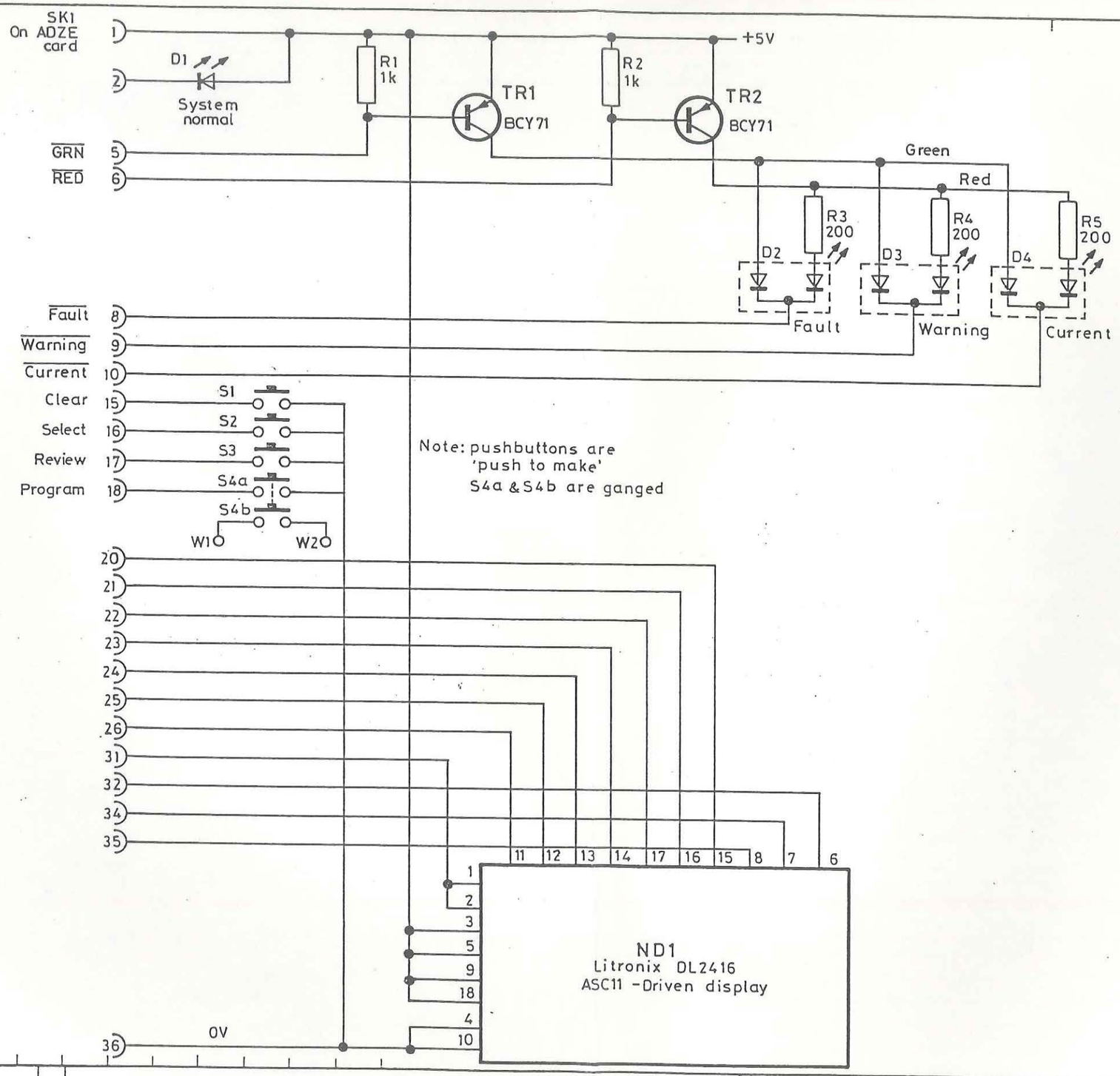
NICAM DATA SPLITTER

CD4S/18
CIRCUIT

All dimensions in millimetres unless otherwise stated: Normal tolerances: no decimal place — ± 1 mm unless; one decimal place — ± 0·3 mm otherwise; two decimal places — ± 0·1 mm stated

DRN.
TCD. A.R.T.
CKD.
APPD. J.R.

DESIGN & EQUIPMENT DEPARTMENT
D60162A1
Sheet 2 of 2 sheets



THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE
277mm x 400mm

ISS	CHANGE
1	18—11—86

NICAM 3 DATA COMBINER / SPLITTER

CD4S/17 & 18

BOARD NO2

All dimensions in millimetres unless otherwise stated: Normal tolerances:
no decimal place — ± 1 mm unless
one decimal place — ± 0·3 mm otherwise
two decimal places — ± 0·1 mm stated

DRN.		DESIGN & EQUIPMENT DEPT.
TCD.	A.R.T.	D60170A3
CKD.		
APPD.	JR	

CHANGE	IS
18-11-86	1
21-11-86	2

ITEM No.	No. OFF		DESCRIPTION	C'CT REF.	BBC REF. OR DRG. No.
			DRAWING NUMBERS		
			CIRCUIT (2 SHEETS) P.B. N°1 D60162A1		
			PARTS LIST D60163A4		
			ASSEMBLY & WIRING D60164A2		
			DETAILS D60165A2		
			P.B. MASTERS N°1 (PHOTO PLOT) D60166A3S		
			P.B. DRILLING D60167A3		
			ENHANCED COMP. LOC N°1 DSK26158A3		
			P.B. MASTER N°2 (PHOTO PLOT) D60306A3S		
			ENHANCED COMP. LOC N°2 DSK26235A3		
			P.B. DRILLING N°2 D60307A3		
			FRONT PANEL LEGEND D60169A2		
			CIRCUIT P.B. N°2 D60170A3		
			FURTHER INFORMATION REQUIRED FOR MANUFACTURE		
			UNIT WIRING INFORMATION EA10140		
			UNIT ASSEMBLY INFORMATION EA10484		
			SPEC ED/CD45/18		
1	1	*+	CODING PLATE, 4U		0326593
			SLOT POSITIONS ARE MODIFIED BY		
			ED. WORKSHOPS BEFORE ISSUE TO CONTRACTOR	TO	D60165A2 DET.
2	1	*	CH1/64A FRONT PANEL		0326613
			MODIFIED BY CONTRACTOR TO:-		D60165A2 DET.
3	1	*	HANDLE		0326569
			ENGRAVED BY CONTRACTOR TO:-		D60165A2 DET.
4	1	*	THUMBSCREW		0326656
5					
6	1	*+	EARTHING WASHER		0400310
7					
8	1	*+	NYLON BUSH		040102X
9					
10	2	*	MOUNTING BLOCK		0351590
11					
12	1	*	PRINTED BOARD N°1		D60166A3S
			TO SPEC. ED/PB/CD45/18/1/P.T.H.		0608705
13					
14	1	*	PRINTED BOARD N°2		D60306A3S
			TO SPEC. ED/PB/CD45/17&18/2		0611358
15					
16					
17	3	*	SWITCH C&K 8181-S-H-C-7527-2		0610377
18	1	*	SWITCH C&K 8225-S-H-C-7527-3		0612398
19					
20	1	*	LIGHT EMITTING DIODE GREEN	2D1	0465653
21	3	*	LIGHT EMITTING DIODE TRI-COLOUR CQX95	2D2-2D4	0608930
22	1	△	DISPLAY FILTER 25X35 MADE FROM ITEM 23		
23	1	*+	POLARISED DISPLAY FILTER R.S. N°. 586-548		0611461
24	1	*	ALPHANUMERIC DISPLAY LITRONIX DL 2416		0525749

BBC

DS/PLA4/1

CD45/18
NICAM DATA SPLITTER
PARTS LIST

DRN.	J.H.
TPD	
CKD	
APPD	ARC

DESIGN & EQUIPMENT DEPT.

D60163 A4

SHEET 1 OF 6 SHEETS

CHANGE	IS
18-11-86	1

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
25	2	*+	SPACER, ROUND 5MM, M2·5 CLEAR		0207465
26	1	*+	SPACER ROUND INSULATING 5MALG. TAPPED M2·5		0325677
27					
28					
29					
30					
31	1	*	CABLE ASSEMBLY D60159A3		0610902
32					
33					
34					
35					
36					
37					
38					
39	10	*	I.C. SOCKET TRANSMISSION 8 POLE		0445453
40	3	*	I.C. SOCKET TRANSMISSION 14 POLE		0445461
41	2	*	I.C. SOCKET TRANSMISSION 16 POLE		040704X
42	7	*	I.C. SOCKET TRANSMISSION 20 POLE		0439423
43	4	*	I.C. SOCKET TRANSMISSION 28 POLE		0445043
44	2	*	I.C. SOCKET TRANSMISSION 40 POLE		0445488
45	4	*	SNAP OFF SOCKET STRIP 20 WAY HARWIN D01 937-2001		0608949
46	1	*	NON VOLITILE RAM SOCKET SMART DS 1213		0611453
47					
48					
49					
50	4	*	DIL PIN HEADER 8 PIN		0446469
51					
52					
53					
54					
55					
56					
			CAPACITORS		
57	1	*	47NF 25V ELECT.	IC20	037540X
58	30	*	100nF 50V CERAMIC FILM IC6-IC19, IC22-IC37		0204648
59	2	*	33pF 100V SINGLE PLATE IC4	IC5	0429820
60	1	*	100pF 63V P.C.B. MOUNTING	IC3	0449968
61	1	*	390pF 125V P.C.B. MOUNTING	IC2	0450164
62	1	*	330nF 50V MULTILAYER	IC21	038983X
63					
64					
65					
66					
67					
68					
69					
70					
71					
72					
73	1	*	60pF MAX, 250V VARIABLE	IC1	0333683
74					
75					

BBC

DS/PLA4/1

CD45/18

PARTS LIST

DRN.	J.H.
TPD.	
CKD.	
APPD.	ARL

DESIGN & EQUIPMENT DEPT.

D60163 A4

SHEET 2 OF 6 SHEETS

CHANGE	IS
18-11-86	1

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
76					
77					
78					
79					
80					
			RESISTORS		
81	1	*	22Ω 2% 0·4W	1R7	0088976
82	1	*	220Ω 2% 0·4W	1R5	0099023
83	1	*	330Ω 2% 0·4W	1R9	0099031
84	9	*	1·0KΩ 2% 0·4W 2R1, 2R2, 1R3, 1R8, 1R10, 1R11, 1R12, 1R17, 1R20		0099082
85	1	*	1·2KΩ 2% 0·4W	1R6	0099102
86	1	*	7·5KΩ 2% 0·4W	1R4	0228027
87	1	*	12KΩ 2% 0·4W	1R1	0228043
88	1	*	15KΩ 2% 0·4W	1R2	0099370
89	1	*	22KΩ 2% 0·4W	1R16	0228078
90	2	*	8X1·0KΩ S.I.L. RESISTOR NETWORK 1R15	1R19	0427980
91	2	*	4X330Ω S.I.L. RESISTOR NETWORK 1R13	1R14	0428141
92	1	*	3KΩ 2% 0·4W	1R23	0099362
93	1	*	470Ω 2% 0·4W	1R18	009904X
94	3	*	200Ω 2% 0·4W 2R3 —	2R5	0099015
95	2	*	4X2·2KΩ S.I.L. RESISTOR NETWORK 1R21	1R22	042B192
96	1	*	10KΩ 2% 0·4W	1LK2	0099224
97					
98					
99					
100					
101					
102					
103					
104					
105					
106					
107					
108					
109					
110					
111			TRANSISTORS		
111	1	*	2N3906	1TR2	0122804
112	1	*	BC109	1TR1	0112282
113	2	*	BCY71	2TR1-2	0112798
114					
115					
116					
117					
118					
119					
120					
121					
122					
123					
124					
125					

BBC

DS/PLA4/1

CD4S/18

PARTS LIST

DRN.	J.H.
TPD.	
CKD.	
APPD	ARL

DESIGN & EQUIPMENT DEPT.

D60163 A4

SHEET 3 OF 6 SHEETS

ISS	CHANGE	
4	18-11-86	

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
126					
			INTEGRATED CIRCUITS		
			CAUTION STATIC SENSITIVE DEVICES		
			HANDLE WITH CARE		
127	1	*	DIC 74LS08N	IIC11	0178362
128	2	*	DIC 74LS138N IIC12	IIC13	0184526
129	2	*	DIC 74LS139N IIC10	IIC14	0173296
130	1	*	DIC 74LS14N	IIC1	0188604
131	1	*	DIC 74LS245N	IIC9	0196698
132	1	*	DIC 74LS273N	IIC17	0191151
133	1	*	DIC 74LS32N	IIC16	0178843
134	4	*	DIC 74LS541N IIC15, IIC18, IIC25	IIC26	0508019
135	1	*	DIC 74LS74AN	IIC2	018212X
136	2	*	SSD/MC 74HC4040 IIC3	IIC4	0521269
137	1	*	Z80B-CPU	IIC5	0519585
138	1	*	Z80B-DART	IIC21	0525757
139	1	*	Z80B-CTC	IIC20	0506913
140	3	*	NM232CD RS232 CONVERTER IIC19, IIC30	IIC31	0523070
141	3	*	DIC 74LS377N IIC22, IIC23	IIC24	0182111
142	3	*	DIC 7407N IIC27, IIC28	IIC29	0153497
143	1	*	HCPL 2630 OPTO ISOLATOR	IIC32	0502188
144	5	*	HCPL 2731 OPTO ISOLATOR IIC33-	IIC37	0505443
145	1	*+	SSD/2712BN-25ONS	IIC6	0516366
146	2	*	DIC TC5565 PL/15 IIC7	IIC8	0526230
147					
148					
149					
150					
151					
			CRYSTALS		
152	1	*	9.83MHz: INTERFACE QUARTZ DEVICES HC18-U	IXL1	0485861
153					
154					
155					
156					
157					
			PLUGS		
158	2	*	SINGLE ROW, 36 PIN SHROUDLESS HEADER	PLC,D	0457322
159	2	*	FIXED .I.D.C. 40 WAY		0491343
160					
161					
162					
			SOCKETS		
163	1	*	6 POLE RIGHT ANGLE MOLEX TYPE A38-00-1336	1SKA	0494022
164	1	*	36 POLE HARWIN M20-989-36-05		0609047
165					
166					
167					
168					
169					

BBC

DS/PLA4/1

CD45/18

PARTS LIST

DRN.	J.H.
TPD.	
CKD.	
APPD.	ARL

DESIGN & EQUIPMENT DEPT.

D60163A4

SHEET 4 OF 6 SHEETS

CHANGE	ISS
18-11-86	1

ITEM No.	No. OFF		DESCRIPTION		C'C'T REF.	B B C REF. OR DRG. No.
170						
171						
172						
173						
174						
175						
176			FOR FIXING ITEMS:			
			SCREWS			
177	2		M2·5 X 6 LG. PAN HD. M.S. ZN. PL.	10,		
178	1		M2·5 X 5 LG CSK. HD M.S. ZN. PL.	26		
179	2		M2·5X 10LG CSK. HD M.S. ZN. PL.	1		
180	2		M3 X 6 LG INST. HD. M.S. CR. PL.	3		
181	2		M3 X 10 LG INST. HD. M.S. CR. PL.	10		
182						
183						
184						
185						
186						
187						
188						
			NUTS			
189	2		M2·5, HEX, FULL M.S. ZN. PL.	1		
190	4		M3, HEX. FULL M.S. ZN. PL.	10,3		
191						
192						
193						
194						
195						
			WASHERS			
196	10		M2·5 PLAIN, M.S. ZN. PL.	1		
197	4		M3 SHK. PROOF, M.S. ZN. PL.	10,3		
198						
199						
200						
201	A/R	*+	WIRE PUFI/3M WHITE			0201524
202	A/R	*+	WIRE PUFI/3M BLUE			020147X
203	A/R		WIRE 1MM B.T.C.			
204	A/R		WIRE 0·6MM B.T.C.			
205	1	*	FOAM PACK			0342743

NOTES:

△	DENOTES 4 OFF ITEM 22 CAN BE MADE FROM 1 OFF ITEM 23
*	Denotes items supplied to the contractor on embodiment loan.
*+	Denotes items supplied to the contractor on embodiment loan, requiring special costing or supply action by B.B.C.
θ*	Denotes components supplied and fitted by B.B.C. on test.
θ+	Denotes coded plug in units supplied and fitted by B.B.C. on test.
Ø	Denotes items supplied and fitted by B.B.C. on installation.

BBC

DS/PLA4/1

CD45/18

PARTS LIST

DRN.	J.H.	DESIGN & EQUIPMENT DEPT.
TPD.		
CKD.		D60163 A4
APPD.	ARL	SHEETS OF 6 SHEETS

SHT	ISS.	DETAILS OF CHANGE	SHT	ISS.	DETAILS OF CHANGE
1	2	ITEM 17 DESCRIPTION REVISED. ITEM 18 C/M Nº WAS 0610385 J.H. 21-11-86			

DESIGN & EQUIPMENT DEPARTMENT

CODE CD43/18

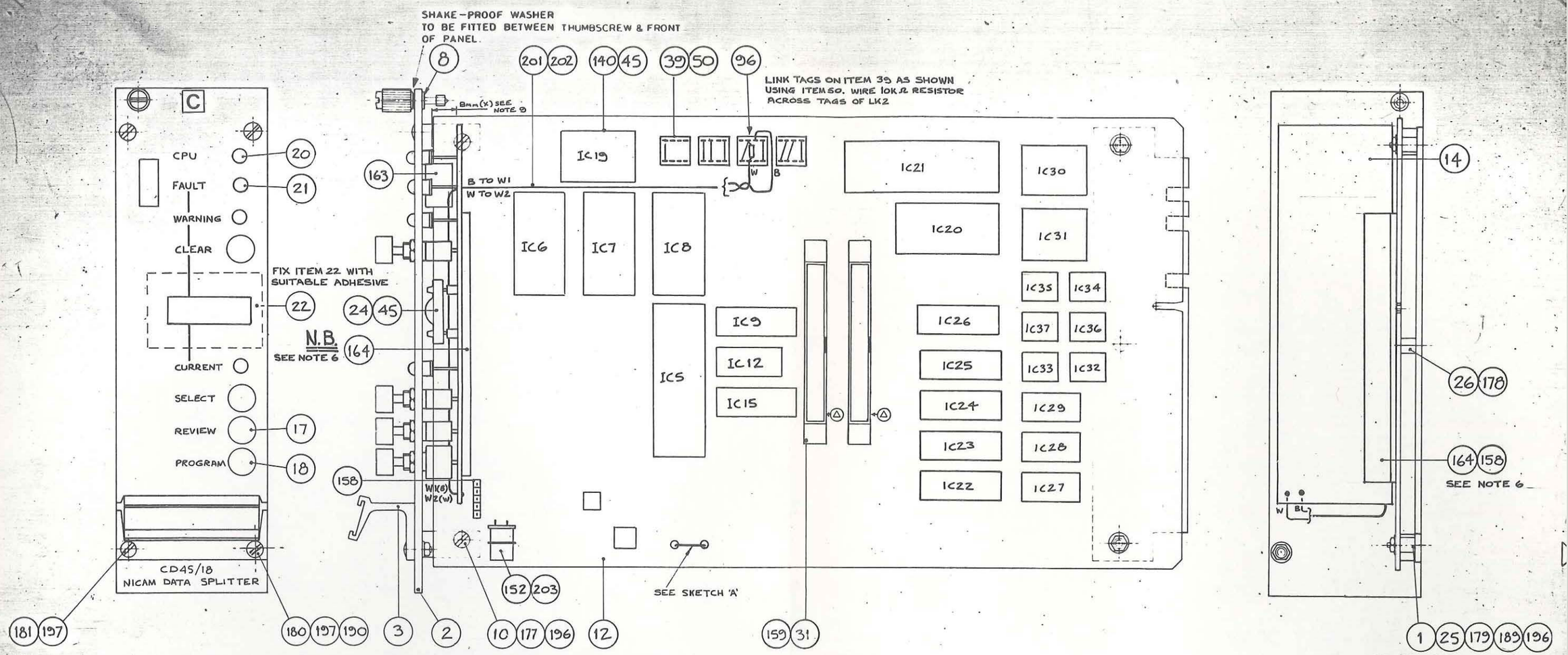
BBC

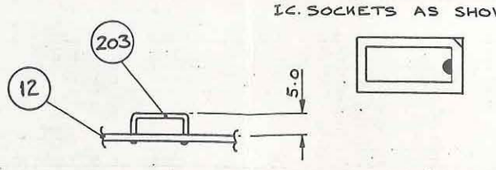
DS/SPA4

PARTS LIST CHANGE RECORD ISSUE:- 1

D60163 A4

SHEET 6 OF 6 SHEETS





SKETCH 'A'

10. I.C.'S NOT SHOWN ARE FITTED DIRECTLY INTO BOARD WITH OUT I.C. SOCKETS AS SHOWN:

NOTES:

1. ASSEMBLY TO BE IN ACCORDANCE WITH EA10484 NOTES 1,7.
2. COMPONENTS TO BE WIRED TO PRINTED BOARD IN ACCORDANCE WITH EA10140 NOTES 1,7, 9 & 16
3. I.C.s SHOWN NUMBERED TO HAVE I.C. SOCKETS FITTED (ITEM Nos 39-45)
4. I.C. No 7 TO BE FITTED INTO ITEMS 43 & 46.
5. MAXIMUM SOLDERING TIME OF 2D1-2D4 260°C-5 SECONDS.
6. ITEM 164 TO BE FITTED TO WIRING SIDE OF BOARD 2
7. S1-S4 (P.B. No 2) [Nc No c] CORNER LINE TO INDICATE PIN 'C'
8. D1-D4 (P.B. No 2) [D] CORNER LINE TO INDICATE FLAT ON DIODE
9. DIMESION 'X' TO BE 8mm (DISTANCE BETWEEN BACK FACE OF DIODES & P.B. No 2)

CIRCUIT - D60162A1
PARTS LIST:- D60163A4

PN1/29J SCALE:-1:1 0 150

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE 400mm x 574mm

ISS	CHANGE
1	18-11-86
2	8-2-88

CD4S/18 ASSEMBLY & WIRING

All dimensions in millimetres unless otherwise stated
Normal tolerances:
no decimal place — ± 1 mm unless
one decimal place — ± 0·3 mm otherwise
two decimal places — ± 0·1 mm stated

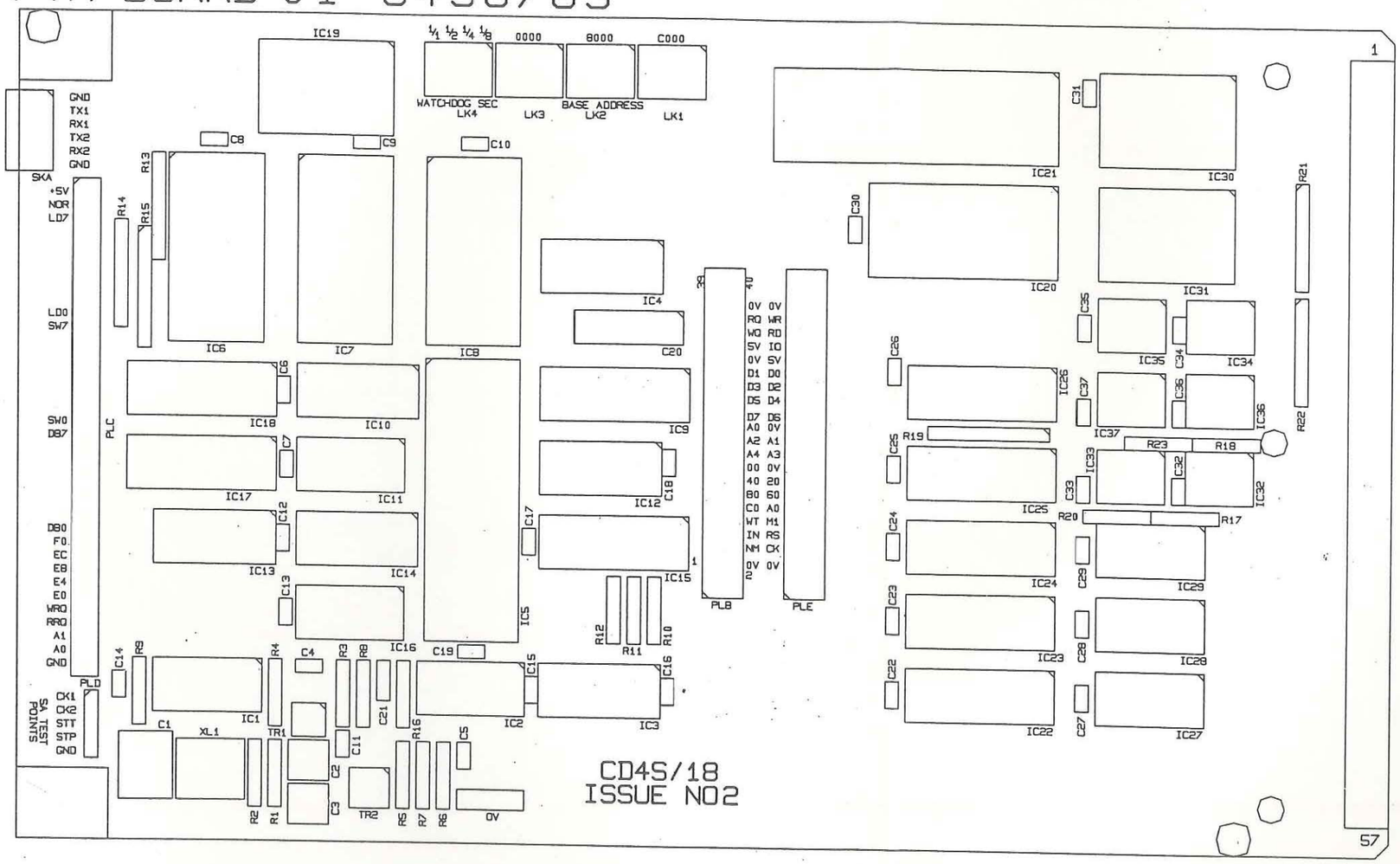
DRN. J.H.
TCD.
CKD.
APPD. ARL

DESIGN & EQUIPMENT DEPT.

D60164 A2

S&H LTD. LSOS

CD4S/18
ISSUE NO2
PTH BOARD 01 3456789



01 3456789

SCALE:- 1:1

Original Frame Size	BBC
VM552A3 277mm x 400mm	DS A3

CHANGE	ISS.
27-10-86	2

Issue no of this drawing must be the same as the photo-master issue.

ENHANCED COPY OF COMP. LOC. PHOTO PLOT

CD4S/18
P.B. Nº 1

DRN	TCD	CKD	APPD.
J.H.			ARL

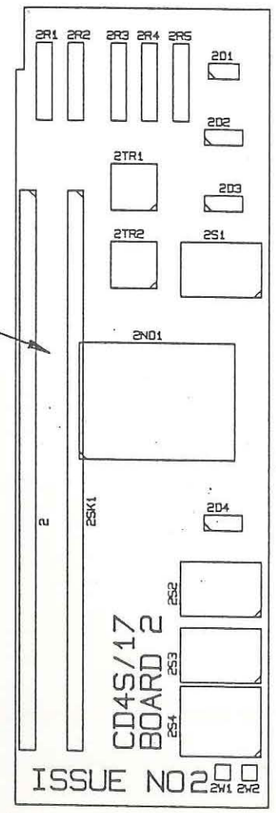
DESIGN & EQUIPMENT DEPT.

DSK26158A3

CD4S/17
BOARD 2
ISSUE NO2
PTH BOARD

N.B.

2 SK1 ITEM 164 ON PARTS LIST TO BE FITTED TO WIRING SIDE OF BOARD.



01 3459867

SCALE:- 1:1

Original Frame Size	BBC
V.M552A3 277mm x 400mm	DS A3

CHANGE	ISS
24-10-86	2

Issue no. of this drawing must be the same as the photo-master issue.

ENHANCED COPY OF COMP. LOC. PHOTO PLOT

CD4S/17
P.B. Nº2

DRN.	TCD.	CKD.	APPD.
J.H.			ARL

DESIGN & EQUIPMENT DEPT

DSK26235A3

Pin no. *		Pin no.		Pin no.	
1.	Chassis earth	20.	Opto. iso. common	39.	16-bit data out D7
2.	Data in (MAIN)	21.	Nicam strobe in	40.	. . . D6
3.	Data out (MAIN)	22.	Opto. iso common	41.	. . . D5
4.	H/S hard in (MAIN)	23	0V	42.	. . . D4
5.	RS23 high out	24	—	43.	. . . D3
6.	RS232 low out	25	0V	44.	. . . D2
7.	Signal earth.	26c.	Aux. fault in 26w. Opto. iso common	45.	. . . D1
8.	Data in (AUX)	27c.	Fault out 27w. Signal earth	46.	. . . DØ
9.	Data out (AUX)	28.	+5V	47.	Signal earth
10.	H/S hard in (AUX)	29.	+5V	48.	N.C.
11.	Signal earth	30.	+5V	49.	.
12.	Nicam data in D7	31.	16-bit data out D15	50.	.
13.	. . . D6	32.	. . . D14	51.	.
14.	. . . D5	33.	. . . D13	52.	.
15.	. . . D4	34.	. . . D12	53.	.
16.	. . . D3	35.	. . . D11	54.	.
17.	. . . D2	36.	. . . D10	55.	.
18.	. . . D1	37.	. . . D9	56.	.
19.	. . . DØ	38.	. . . D8	57.	0V

* Wiring side is connected to component side unless otherwise indicated.

ORIGINAL FRAME SIZE 190mm x 277mm

THIRD ANGLE PROJECTION

All dimensions in millimetres unless otherwise stated:
Normal tolerances:
no decimal place — ± 1 mm unless
one decimal place — ± 0.3 mm otherwise
two decimal places — ± 0.1 mm stated

BBC

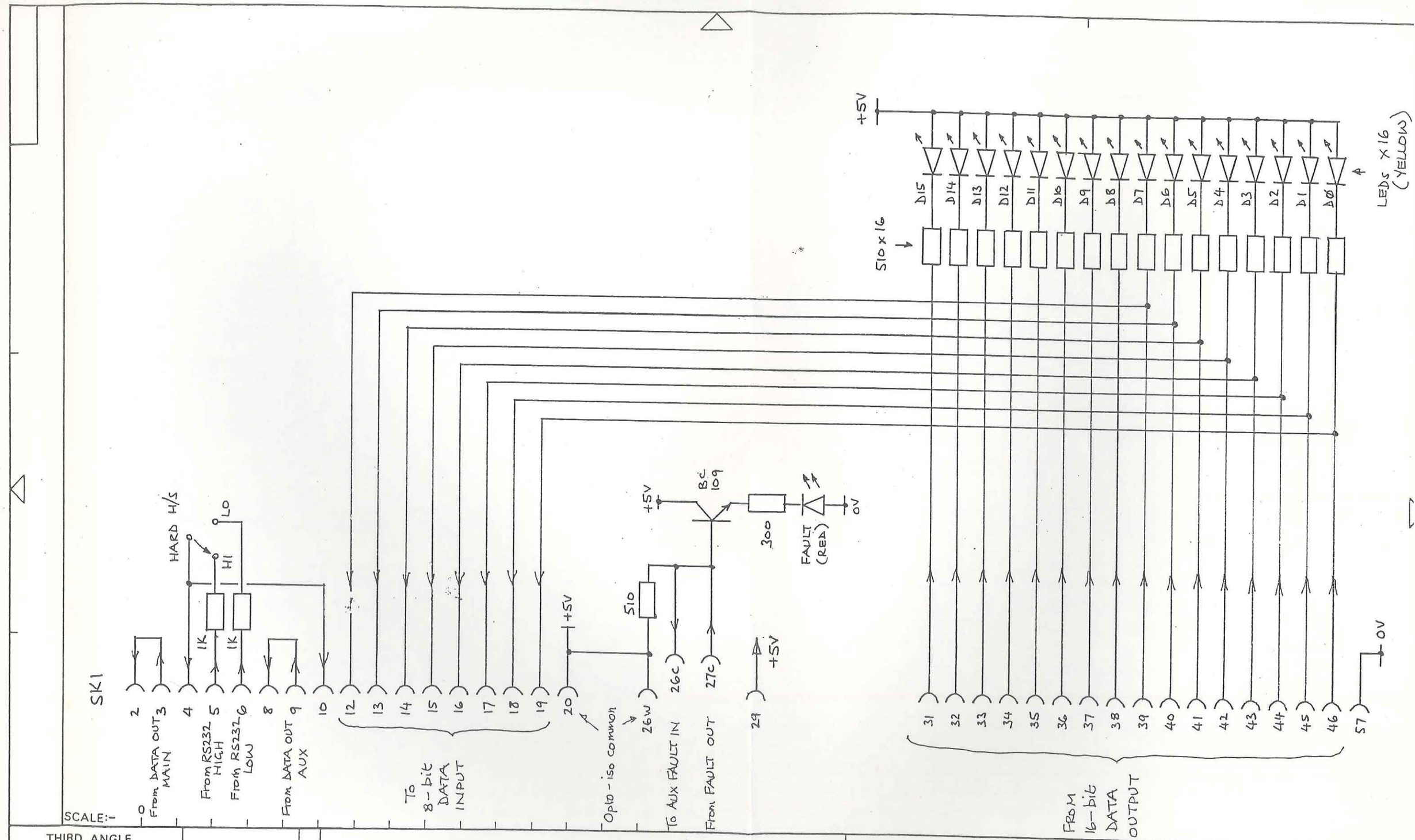
DS/A4

SCALE

ISS | CHANGE | 17-8-87

CD4S/18 NICAM DATA SPLITTER
CONNECTOR PIN-OUT

DRN.	DND	D & ED
TCD.		DSK 26738 A4
CKD.		
APPD	DND	



SCALE:-

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE
277mm x 400mm

ISS CHANGE 17-8-87

TEST BOX FOR NICAM DATA SPLITTER.
CD 45/17

All dimensions in millimetres unless otherwise stated: Normal tolerances:
no decimal place — ± 1 mm unless
one decimal place — ± 0·3 mm otherwise
two decimal places — ± 0·1 mm stated

DRN.	DND
TCD.	
CKD.	
APPD.	DND

D & ED

DSK 26740 A3