DESIGN & EQUIPMENT DEPARTMENT

HANDBOOK A.1026(87)

CD4S/17 NICAM-3 Signalling Combiner

.....
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for H.D.& E.D.

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1 INTRODUCTION

The NICAM-3 Signalling Combiner (CD4S/17) is a 4U unsupported card with an A-width front panel, which is used in conjunction with a NICAM-3 2-channel Coder (CD2M/17 or equivalent) and one or more NICAM-3 Decoders (CD3M/33) each with a NICAM-3 Signalling Splitter (CD4S/18). Such a network provides two major facilities:

I) Two RS232C serial character streams, input to the Combiner, are available as outputs from every Splitter on the network. One stream, designated MAIN, will be used to distribute Radio Data (RDS) update information via the national NICAM-3 network. The other stream, designated AUXILIARY, is available for any other future requirement, as yet unspecified. The inputs have similar characteristics, but the MAIN input is awarded a higher priority.

II) A 24-bit parallel input, designated Transmitter Control (TXCTRL). A 16-bit field of this input accepts 16 "static" switching functions (e.g. mono/stereo) which appear at a corresponding 16-bit output port of any splitter or group of splitters on the network, to which the data is addressed. Addressing will ultimately be controlled via the remaining 8 input bits, but earlier versions of the Combiner send all TXCTRL data to the same address as set up via the front panel.

The Combiner is designed around the ADZE 2 general purpose microcomputer module, which is fully described in D.D.H.B. 6.267(85).

2 SPECIFICATION

Maximum supply voltage: +5.25V
Nominal supply voltage: +5V
Minimum supply voltage: +4.8V

Nominal supply current: 0.75A

Main serial (DCE) port:
- Electrical characteristics:
  - To EIA std. RS232C
- Interface connections:
  - Data input (TXD)
  - Data output (RXD)
  - Handshake output (DSR)
  - Signal ground
- Baud rate (input and output):
  - 300,600,1200,2400,4800,9600

baud, set from front panel

Data format:
8 bits, 1 stop bit, no parity

Flow control:
Both DSR and X-ON/X-OFF (DC1/DC3)
are output.

AUXILIARY (DCE) port:
As main port.

TXCTRL port:
Interface connections:
Data optocoupler common anode
Data inputs (16 off)
Address optocoupler common anode
Address inputs (8 off)

Input load (common anode to any data bit):
LED (1.4V drop) with series 2k2 resistance

Nominal data input current (logic "0"):
1.6mA
Maximum data input current:
20mA

NICAM-3 Interface port:
Interface connections:
Strobe input optocoupler anode
Strobe input
Data output common ground
Data output open collectors (8 off)

Strobe input load (anode to input):
LED (1.5V drop) with series 470R resistance

Nominal strobe input current (logic "0"):
5mA
Maximum strobe input current:
15mA

Maximum data output logic "1" voltage
+30V
Maximum data output logic "0" current
40mA

Dimensions: 4U high BMM unsupported card with
A-width front panel.

Weight: Approx 350g
Connector: 112-way edge connector

See DSK26737A4 for pinout details.

3 OPERATION

3.1 Power Supplies

The unit requires a single supply of 5V nominal. The voltage on the card must not fall below 4.75V, because, quite apart from this being the lower limit at which operation of many of the ICs is guaranteed, the non-volatile RAM device, IC7, will disable RAM access below this voltage.

3.2 Serial Inputs

The MAIN and AUXILIARY serial input ports are normally connected to female 25-way D type connectors fixed to the parent cardframe. These should be wired as DCE ports, with suggested connections as follows:

1	Safety ground
2	TXD input
3	RXD output
4	(Connect to 5)
5	(Connect to 4)
6	DSR output
7	Signal ground

Data sources should be set to 8 bits, no parity. Flow control may be implemented in either of two ways; when the Combiner needs to stop the incoming flow, it drops the DSR output and sends an X-OFF character to RXD. When it is able to accept data again, it raises DSR and sends an X-ON character. Either protocol may be used to control the data source. In order to avoid potential lockout conditions with X-ON/X-OFF handshaking, the Combiner sends an X-ON every 5 seconds if no incoming data is detected.

3.3 TXCTRL Input

The 16-bit TXCTRL data input is optically isolated from the main circuit. The anodes of the 16 data couplers are connected together and should be fed from a +5V reference supply; each coupler input should then be connected to 0V to send a logic "0". or left floating to send a logic "1". This arrangement facilitates the use of open-collector drivers. Data inputs have individual current-limit resistors, whose values are appropriate for a 5V supply. Additional series resistors should be used with higher

input reference voltages.

3.4 NICAM-3 Data Port

The NICAM-3 data port connects directly to the signalling port of the NICAM-3 Coder. The open-collector strobe pulse from the coder enters via an optocoupler similar to those used for the TXCTRL inputs mentioned above, except that the coupler is a special high-speed type, and the internal pullup resistor has a lower value. The 8-bit parallel data output is buffered by high-voltage open-collector drivers, whose pull-up resistors are provided by the NICAM-3 Coder.

3.5 FAULT output

The open-collector FAULT output is normally low (on). It is driven high (off) if the equipment detects a serious error condition (i.e. whenever the front panel FAULT LED indicates a fault - described later). This polarity ensures that a fault is signalled as a result of power failure.

3.6 Non-volatile memory

Because there are many options affecting the characteristics of the Combiner, these are set up interactively via the front panel (as described in the next section) and stored in non-volatile memory. This memory is protected in three ways. A logic circuit prevents writing to memory when the power rail drops below 4.75V, at which point an internal lithium battery cuts in to preserve the memory. With power applied, the memory is electrically write-protected at all times except when the PROGRAM key is depressed. Furthermore, two copies of the system control data are maintained in non-volatile memory, both protected by 16-bit cyclic redundancy check codes.

3.7 Displays and Controls

The front panel contains 4 LEDs, 4 pushbutton keys and a 4-character alphanumeric display. The latter device has 4 functions; during normal (non-interactive) operation, it displays the ident code assigned to the combiner. If the unit detects a serious error, a code appears on the display accompanied by an indication on the FAULT LED and the FAULT signalling output; this takes priority over any other display. Less serious errors result

In a display code and a WARNING LED indication. Finally, the display operates with the keys below it during setup and review of the various system options described below. All the programmed display messages are summarised in Appendix A.

3.7.1 CPU Normal LED

The green CPU Normal LED reflects the state of the "watchdog timer" which resets the system in the event of a soft malfunction or power-up. The LED should normally glow continuously; flashing indicates a probable hardware error.

3.7.2 Status Display

During normal (non-interactive) operation, the alphanumeric display shows the ident code of the combiner.

3.7.3 Selecting A System Control Item

Use the SELECT key to select one of the system control items. Each time the key is pressed, the next item name is displayed. If the key is held down, the display will cycle through the items automatically until the key is released.

3.7.4 Examining The Item Setting

Once an item is selected, if no further keys are pressed, the Combiner will display a three-word explanation of the item code followed by the setting currently programmed for the item. This is displayed for a short time, then the Combiner will revert to its normal (non-interactive) operation.

3.7.5 Examining Several Item Settings

SELECT may be pressed at any stage during the above sequence in order to select the next menu item in the sequence. Furthermore, the 3-word explanation may be bypassed or aborted by pressing the REVIEW key. Thus the settings of all items in the menu may be examined by alternately pressing SELECT and REVIEW.

3.7.6 Reviewing Alternative Settings

When the current setting of an item is displayed (accompanied by an indication on the CURRENT LED), alternative settings may be seen by pressing the REVIEW key. Like SELECT, this cycles through all the options and repeats automatically if held down.

3.7.7 Changing The Current Setting

When a setting has been selected with the REVIEW key, the PROGRAM key (coloured red) may be pressed to store that setting permanently. PROGRAM should be held down until the CURRENT LED indicates that the setting is now the current one. This is necessary because the non-volatile system control memory can be altered only when PROGRAM is pressed, and the programming operation involves copying a large block of data to that memory. The Combiner checks that the data has been copied successfully; if not, the display will indicate REPT accompanied by the WARNING LED, and the programming operation should be repeated.

When any item setting has been displayed for a short time without any keys pressed, the Combiner will exit its menu mode and revert to the background status display.

3.7.8 System Control Items In Detail

3.7.8.1 Serial Baud Rates (BR 1, BR 2) - These items determine the data rates of the Main (RDS) and Auxiliary serial ports respectively. In both cases, the transmit and receive rates are identical. All "standard" speeds (binary sequence) are supported from 300 to 9600 baud.

3.7.8.2 LED Characteristics (LEDS) - Different users have different views about LED indications. Some people prefer red LEDs which are normally off, others want green LEDs which are normally on. This equipment provides a choice via the LEDS setting. A variety of "normally off" colour combinations for the 3 LEDs is available, in addition to all red, yellow or green "normally on" options.

3.7.8.3 Status Display (SDPY) - Three options are available controlling the display of fault and warning messages. The instantaneous (INST) option means that every displayed message remains only for the duration of the offending condition (strictly

for a short time after the condition clears). The HOLD option "freezes" any fault or warning signal until the CLEAR key is pressed. The third option, FHWI, "freezes" fault signals but displays warning messages on an instantaneous basis.

3.7.8.4 Combiner Ident (IDNT) - This item controls the Combiner Ident Code which is sent in every TXCTRL packet. The ident code is used to identify the "service" accompanied by the signalling data, and every Splitter (CD4S/18) attached to the network is set up to accept only a subset of the ident code list. This provides a measure of protection against incorrect service routing within the network. The selected ident code is displayed continuously during normal (non-interactive) operation. It has no affect on the serial data channels.

3.7.8.5 Splitter Address (ADRS) - This item controls the Splitter Address Code which is sent in every TXCTRL packet. It provides a means of controlling the number of Splitters (CD4S/18) which will accept data from a given combiner; each Splitter is set up to accept only a subset of the address code list. The addressing facility differs from the ident code facility in that splitters simply ignore data containing a "non-actionable" address, whereas they will raise a fault condition on receiving an invalid ident code.

4 CIRCUIT DESCRIPTION

(Notation throughout: IC7p9 means IC7 pin 9. All addresses and data representations are stated in hexadecimal radix unless otherwise indicated. Numerical ranges are stated using the PASCAL convention e.g. 0..3 means 0,1,2,3).

4.1 ADZE 2 Computer Module

The ADZE 2 module, which forms the hardware basis of this design, is fully described in D.D.H.B. No. 6.267 (85). The 40-way main interface plug (PL8) is connected to a similar 40-way plug via a short ribbon cable, which may be disconnected to isolate the ADZE 2 module for testing (power supply connections are made via permanent PCB tracks). Modifications to the ADZE 2 are as follows:

i) XL1 is a 9.83MHz crystal (30pF parallel resonant) to facilitate division down to the standard serial baud rates.

ii) IC5 is a Z80B-CPU, to run at the higher clock frequency.

iii) IC6 is a 16k x 8 EPROM, 250ns address access, e.g. Intel 27128-25.

iv) IC7 is an 8k x 8 low-power static RAM, 200ns address access, e.g. Hitachi HM6264LP-15, with Dallas "SmartSocket" DS1213 providing battery backup and protection logic.

v) IC8 is an 8k x 8 static RAM, 200ns address access, e.g. Hitachi HM6264P-15 or HM6264LP-15.

vi) LK3 and LK1 are "standard" ADZE 2 memory configuration headers for IC6 and IC8 (see DSK25411A3). LK2 is specially wired to provide write protection switching, see D60155A2.

vii) LK4 is wired with pins 4 and 5 connected, to provide a watchdog run time of 0.85 sec.

4.2 Front Panel

The front panel CPU Normal LED, pushbutton keys and alphanumeric display follow standard "ADZE 2" practice (see DSK25412A3). The remaining 3 LEDs are two-colour, common cathode devices whose cathodes are connected conventionally to bits 0,1 and 2 of the ADZE 2 LED drive port. The anodes are switched by TR1 and TR2 under the control of bits 4 and 5 of the LED port. The arrangement allows any combination of the LEDs to be lit with the same colour, red (TR2 on), green (TR1 on) or yellow (both transistors on), by means of a single control byte written to the LED port.

4.3 Counter-timer

IC20 is a Z80B-CTC, providing 4 counter-timer channels derived from the 4.9152MHz system clock. It is configured as the highest priority device in the interrupt daisy-chain (IEI is connected to +5V, and IEO feeds the next device in the chain), and mapped to port addresses C0..C3. Mode 2 Z80 interrupts are fully supported. Hardware reset is accomplished by the system watchdog timer.

Channel 0, which has the highest interrupt priority, is externally triggered by the NICAM strobe pulse input (CLK/TRG0 pin). When initialised in timer mode by the software, it interrupts the CPU shortly after each strobe pulse, to indicate that a new byte of NICAM data is required.

Channels 1 and 2 are used to generate baud rate clocks for the two DART channels. They are initialised by the software to operate in cyclic counter mode, generating clock pulses at the zero-count pins, which feed the DART, IC21. The pulse frequency is 16 times the baud rate. No interrupts are requested by these channels.

Channel 3 is used without external connections, as a real-time clock reference for such things as timing the menu displays. It is initialised by the software to interrupt the CPU every 10msec.

4.4 RS232 Communications

IC21, a Z80B-DART (Dual Asynchronous Receiver-Transmitter), interfaces the CPU to the two bidirectional serial ports. IC29 and IC30 convert between "TTL" logic levels and "RS232" voltages; they each contain 4 inverting buffers (2 send, 2 receive) powered by an internal voltage converter.

The Z80B-DART provides a subset of the more familiar Z80-SIO functions. In this application it uses port addresses A0..A3 and mode 2 interrupts, taking second priority to IC20 (IEI comes from IEO of IC20; IEO is the end of the daisy-chain). Hardware reset is accomplished by the system watchdog timer. Input and output handshake pins (CTS and DTR) are both connected to the RS232 drivers for each channel, although only DTR is actually used.

4.5 TXCTRL data input

The 16-bit TXCTRL data input is buffered and isolated by optocouplers IC36..IC43. These are dual couplers, specified for 1.6mA input current. The resistors R23..R26 set the current to this value with 5V applied across the floating input terminals. R17..R19 pull the open collector coupler outputs to +5V.

IC23 and IC24 are "standard" ADZE 2 parallel input ports mapped to addresses 0 (low byte) and 20 (high byte) respectively. Data changes on these inputs are sensed by software polling.

4.6 TXCTRL address Input

Optocouplers IC32..IC35 and input port IC22 interface the 8-bit TXCTRL address input to the CPU at port address 40. This port is ignored by the current software.

4.7 NICAM-3 Strobe Pulse Input

Because the NICAM strobe pulse is of short duration (700ns), its optocoupler IC31 is a special high-speed type, specified for 5mA input current (hence the low value of R20, for 5V input).

4.8 NICAM-3 Data Output

IC26, a "standard" ADZE 2 parallel output port at address 60, interfaces the output data to the NICAM-3 Coder via the high-voltage open-collector drivers IC28 and IC27. The driver outputs should normally be pulled up to +5V externally.

4.9 Fault signalling output

IC25 provides an 8-bit parallel output port at address 80. Bit 0 of this port carries the fault detection output, which is presented to the host equipment through high-voltage open-collector driver IC27.

5 SOFTWARE DESCRIPTION

5.1 Functionality

This section describes what the system does, in terms of inputs, processing and outputs.

5.1.1 Serial Data Inputs

The presence of valid data at either of the serial inputs generates an interrupt, and subsequently the system reads the data and places it in a circular queue (buffer) associated with that port. Data is removed from a queue whenever it is possible to transmit it to the NICAM interface. If a queue approaches full occupancy, then the combiner attempts to stop the input by sending an X-OFF character to the port, and dropping the DSR handshake line. If this fails to

halt the input (i.e. the data source does not respond to the handshake signal) and the queue subsequently becomes full, then a fault condition is signalled and further incoming data is ignored. When the queue is nearly empty, the Combiner sends an X-ON character and raises DSR to signal to the source that it is ready to accept further data.

If a queue remains empty, the Combiner sends an X-ON character at regular (5 second) intervals, to prevent any sustained "lock-out" condition from occurring. The queue lengths are minimal (16 bytes) to prevent the build-up of an unduly large time delay due to data "in transit".

5.1.2 Packet Structure

Every 3ms a strobe pulse from the NICAM-3 Coder triggers channel 3 of the Z80-CTC, which subsequently interrupts the CPU requesting the next byte of NICAM data. This must be generated during the time window between 0.1ms and 2.9ms after the strobe pulse.

The output to the NICAM-3 Coder comprises a continuous stream of bytes, which are generated in groups of between 3 and 9 bytes referred to as "packets". Each packet comprises between 1 and 7 data bytes, followed by a 2-byte "header" ("footer"?) containing the packet type, data length and protection code (checksum). There are 3 types of packet;

I) MAIN (type 0). This type of packet contains between 1 and 7 bytes of data from the main serial input port. Consecutive serial packets contain consecutive bytes from the serial data stream.

II) AUX (type 1). This is similar to a MAIN packet, but contains data from the auxiliary serial input port.

III) TXCTL (type 2). This contains the combiner ident code and splitter address code as set up via the front panel, followed by a 16-bit TXCTRL word (sent high byte first). A type 2 packet thus has a fixed data length of 4 bytes. The ident and destination codes are numbered in the same sequence as the items in the menu lists, starting at 0 for BH01 and ALLS respectively.

The formats of the packet data and header are summarised in Appendix B.

5.1.3 Packet Sequence

The NICAM-3 output is continuous, in that packets are always generated even when no new data is available. The packet sequence is controlled by a set of rules based on the importance of the 3 data sources.

TXCTRL data has the highest priority of all, because it controls real-time transmitter switching, for example at programme junctions. The overall delay through a combiner/NICAM-3/splitter network in response to a change of TXCTRL settings must be less than 50msec. To achieve this, the TXCTRL input is sampled after every NICAM-3 strobe pulse to see whether it has changed since the last TXCTL packet was sent. If it has, then the system sends a new TXCTL packet as soon as possible. This is usually after completion of the packet currently being sent, although if this is a serial data packet, it may be terminated immediately by appending a header (i.e. the length of a serial packet may be "trimmed" while the packet is under construction - a benefit of placing the "header" after the data). If the TXCTRL data does not change, then a timer is used to force a TXCTL packet to be sent regularly (once per second), so that a remote splitter switched on from cold will capture the data within a short time.

If a TXCTL packet is not required, the main and auxiliary data queues are examined to see whether any data is waiting. Main data takes priority over auxiliary data, unless there are more than 7 bytes in the auxiliary queue and less than 7 in the main queue. If any data is queued, then a serial packet is started. It is terminated when the relevant queue is empty, or when 7 bytes of data have been sent (or TXCTRL data changes as described above).

If the preceding checks produce no packet data, then TXCTL packets are sent containing the current TXCTRL settings.

5.1.4 NV RAM Management

The characteristice of the Combiner are controlled by the values of a number of "system control variables" held in the main (volatile) RAM. When any of these variables is changed, a Cyclic Redundancy Check Code word is computed and stored with the system control block, allowing the integrity of the block to be continuously checked. Such checking occurs during normal operation of the Combiner, and any failure will cause the program to "crash" in a controlled manner, allowing the system watchdog timer to reset the CPU.

Whenever the variables are changed, two copies of the new working data block are made in the non-volatile RAM. These provide the initial settings of the working RAM variables following a system reset for whatever reason. The maintenance of 2 copies improves the chance of recovery from a failure occurring, for example, during the process of copying data into the non-volatile RAM.

5.1.5 Interactive Mode

The system tests the SELECT key continuously during normal operation, entering its interactive (menu) mode if it is pressed. Menu operations proceed in "background" mode, i.e. they are fully interruptible, and data processing continues under interrupt control.

A full description of the interactive mode has already been given (Operation section). The duration of each displayed message is controlled by the soft timer channels driven by CTC channel 3.

5.2 Design overview

The Combiner software system may be split into 2 subsystems; the handling of real-time events which cause interrupts, and the "background" tasks, including interactive (menu) operation, which are interruptible. Before these subsystems can be used, various initialisation tasks are performed, which are described below under the heading "module descriptions".

5.2.1 Interrupt-driven Software

When an event generates an interrupt request, and the CPU responds by entering the associated handler, further interrupts are disabled until the handler has finished executing and returned control to the background process. This single-level interrupt approach greatly simplifies the software design, although it does constrain the maximum time taken by interrupt handlers of low priority, to guarantee that a high priority event receives control within an acceptable time. The following table summarises the response of the system to each interrupt-generating event, in descending order of priority.

Event	Response
NICAM strobe pulse	Output the next byte of packet data to the NICAM-3 Coder. This interrupt handler does all the

	decision-making and computation needed to generate the continuous packet stream.
Clock tick (10ms)	Increment all the soft timer variables.
Main serial port special receive condition	Read and discard the offending character, reset the S.R.C. detector.
Main serial port received character available	Read the character, add it to the main queue. This handler is also responsible for flow control and overflow detecion and signalling.
Aux serial port special receive condition	As for main port
Aux serial port received character available	As for main port

The soft timer variables are 16-bit integers which may be set to zero and read (via dedicated procedures which locally disable interrupts) for such purposes as display duration timing.

The serial port special receive condition (S.R.C.) arises from an input framing error or overrun, and should not normally occur. Received characters are buffered within the Z80-DART to a depth of 3 characters, to allow for a delay before interrupt service is granted.

5.2.2 Interruptible Software

The "background" program continuously writes the combiner ident code to the alphanumeric display, checks the system control variables' CRC, and reads the state of the SELECT key. If the CRC check fails, it disables interrupts and halts the CPU to force a system reset. If SELECT is pressed, the menu driver is entered, allowing the operator to inspect and/or change the system control settings. The menu driver returns control to the background program when no front panel keys have been pressed for a preset time.

5.3 Coding principles

5.3.1 Programming Tools

The firmware for the Combiner was developed under the VAX/VMS and CP/M operating systems, using PASCAL and Z80 Assembly Language. The front panel menu drivers were developed using the Whitesmiths native PASCAL compiler under VAX/VMS, and tested with a simulated front panel on a VT100 terminal. The remaining software was subsequently written under VAX/VMS and compiled/assembled under CP/M, using the Digital Research PASCAL/MT+ compiler and Microsoft M80 Macro Assembler. The modules were linked under CP/M by the Digital Research LINKMT linker. Initial testing in the Combiner hardware was carried out under the ADZE Interactive Monitor (AIM) with the program in RAM, before transfer to stand-alone ROM code.

The proportion of Assembly Language code has been kept to a minimum, but Assembly Language has always been used in preference to "non-standard" PASCAL extensions. PASCAL and Assembly code are always in separate modules, without recourse to the INLINE feature of PASCAL/MT+.

5.3.2 Module Conventions

5.3.2.1 Procedure And Function Arguments - The convention adopted for all inter-module procedure calls is that used by PASCAL/MT+. This convention is relaxed for intra-module assembly language calls.

Arguments are passed as 16-bit words on the stack. In the case of 8-bit arguments, the high byte is set to zero. A 16-bit absolute address is used to pass arguments by reference. PASCAL calls push the arguments onto the stack in the order in which they are written (leftmost first), followed by the return address.

Called procedures are responsible for removing the return address and all arguments from the stack. A function returns its value as a 16-bit word at the top of the stack.

5.3.2.2 Use Of Z80 Registers - Registers are not generally preserved across procedure calls. All the general registers are available for use by a procedure, but interruptible procedures must not use IX,IY, or the alternate register set since these are not preserved across interrupts. Code generated by PASCAL/MT+ uses only the AF, HL, DE and BC registers.

5.3.2.3 Interrupt Status - In general, background code runs with interrupts enabled, interrupt handlers run with interrupts disabled and enable interrupts on completion. Code is not generally re-entrant; the exception is the procedures which report faults and warnings on the alphanumeric display. These may be called by both background and interrupt service code, and should therefore be modified with caution.

5.4 Environment

5.4.1 Memory Addresses

Address Range	Memory Type	Access
0000 .. 3FFF	Program EPROM	Read Only
8000 .. 9FFF	Non-volatile RAM	Read Only (normal) Read/Write (PROGRAM key pressed)
C000 .. DFFF	RAM	Read/Write

5.4.2 I/O Port Addresses

Address	I/O	Description
00	I	Tx Control Data, low byte
20	I	Tx Control Data, high byte
40	I	Tx Control Address
60	O	Signalling byte to NICAM-3 coder
80	O	Fault indication (low bit only)
A0		DART channel 0 data
A1		DART channel 0 control
A2		DART channel 1 data
A3		DART channel 1 control
C0		CTC channel 0
C1		CTC channel 1
C2		CTC channel 2
C3		CTC channel 3
E0	O	Alpha display character 0 (rightmost)
E1	O	Alpha display character 1
E2	O	Alpha display character 2
E3	O	Alpha display character 3 (leftmost)
F4	I	Front panel switch states
F8	O	Front panel LED drives
FF	O	Watchdog timer reset

5.5 Program Synopsis

The details in this section are intended mainly to help you to find your way round the actual code, by summarising the functions of all the globally accessible procedures. Details are valid for all modules last revised before 12-Jun-1987.

Program modules and component procedures are described here in alphanumeric order. Embedded procedure calls are named only if the name appears in the cross-reference list (i.e. it is separately described here). Every program module is defined by two files; one contains the actual source code ("implementation module"), the other contains a set of definitions ("definition module") for this code, suitable for automatic inclusion in those other modules which use the code.

5.5.1 Module List

Modules should be linked in the following order:

CMKNL
CMIO
CMNVR
CMINTSRV
COMBINER
CMPANEL
CMMENU
CMTEXT
CMVAR
B4LIB
PASLIB
AFTLIB

All object modules sourced in Assembly Language should be renamed to conform with the .ERL file extension required by LINKMT. PASLIB is the searchable PASCAL/MT+ run-time support library, which should be suffixed /S in the link list to force extraction of required modules only. Relocation bases are 0000 for program code, CD00 for data.

5.5.2 Procedure Cross-reference

(This list contains only globally accessible procedures and functions)

Procedure	Module
CALCRC	CMNVR

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CMVAR
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5.5.2 Procedure Cross-reference

(This list contains only globally accessible procedures and functions)

Procedure	Module
CALCRC	CMNVR

CHKCRC	CMNVR
CLEAR	CMIO
CLRDEB	CMPANEL
CMMAIN	COMBINER
COPY	CMNVR
CRASH	CMNVR
CTCIO	CMKNL
CTCI3	CMKNL
DISINT	CMKNL
DPYCHR	CMIO
DPYCURR	CMPANEL
DPYNORM	CMPANEL
ENINT	CMKNL
EXPLAIN	CMMENU
FAULT	CMPANEL
FOCOFF	CMKNL
FOCON	CMKNL
HEAD	CMKNL
HSOFF	CMKNL
HSON	CMKNL
INIT	CMKNL
LEDDRV	CMIO
NEXTITEM	CMMENU
PICKITEM	CMMENU
PICKSETTING	CMMENU
PROG	CMIO
PRGDEB	CMPANEL
QINIT	CMINTSRV
RESINT	CMKNL
REVDEB	CMPANEL
REVIEW	CMIO
RX0	CMKNL
RX1	CMKNL
SELDEB	CMPANEL
SELECT	CMIO
SETBR1	CMKNL
SETBR2	CMKNL
SETZERO	CMINTSRV
SPEC0	CMKNL
SPEC1	CMKNL
STROBE	CMINTSRV
TEXTDEFINE	CMTEXT
TICK	CMINTSRV
TIMER	CMINTSRV
TOQA	CMINTSRV
TOQM	CMINTSRV
TXCTLH	CMKNL
TXCTLL	CMKNL
WARN	CMPANEL

5.5.3 Entry Points

Event	Entry point
Reset	CMKNL (beginning of module)
NICAM strobe pulse	CTC10
Clock tick (10ms)	CTC13
Main serial S.R.C.	SPEC0
Main serial receive	RX0
Aux serial S.R.C.	SPEC1
Aux serial receive	RX1

5.5.4 Module CMINTSRV (PASCAL/MT+ Source)

This module contains interrupt service routines which are mostly called by the interrupt entry code in module CMKNL. Associated general purpose procedures are also in this module if they share data with the service routines or they are sensitive to the CPU status.

5.5.4.1 QINIT - Set input and output pointers of both serial data queues to zero (i.e. queues empty). Set packet control pointers to indicate ready to start new packet. Set soft timers for TXCTRL packet, main X-ON and aux X-ON repeaters to zero.

5.5.4.2 SETZERO - Disable interrupts. Set one of the 4 software timer variables to zero, as specified by the argument. Reset interrupts.

5.5.4.3 STROBE - This function returns the next byte to be sent to NICAM. IF ready to start a new packet THEN decide what type of packet it should be and set up as much of it as possible in the array NEWPKT. (If either serial queue is empty and the X-ON repeater has timed out, then send X-ON and reset the repeat timer). ELSE IF a serial packet is being sent AND there is no reason to terminate it THEN extend the current packet. ELSE IF a serial packet is being sent AND it must be terminated THEN generate and

store the header bytes. Return the next byte from the current packet and step the pointer to the following byte.

5.5.4.4 TICK - Increment each of the 4 software timer variables.

5.5.4.5 TIMER (Function) - Disable interrupts. Read and return the value of the software timer variable specified by the argument. Reset interrupts.

5.5.4.6 TOQA - IF aux serial queue is not full THEN (store argument data in aux queue. Increment input pointer with wraparound. IF queue occupancy is now at critical level THEN call HSOFF.) ELSE IF no fault is being displayed THEN display fault status message "AOFL" (call FAULT). Reset the aux X-ON repeat timer.

5.5.4.7 TOQM - IF main serial queue is not full THEN (store argument data in main queue. Increment input pointer with wraparound. IF queue occupancy is now at critical level THEN call HSOFF.) ELSE IF no fault is being displayed THEN display fault status message "MOFL" (call FAULT). Reset the main X-ON repeat timer.

5.5.5 Module CMIO (MACRO-80 Source)

This module contains procedures which access the front panel components.

5.5.5.1 CLEAR (Function) - Read the front panel switch port. Return the state of the CLEAR button as a boolean value.

5.5.5.2 DPYCHR - Use the character position argument to select an alphanumeric character output port. Output the ASCII character argument to this port.

5.5.5.3 LEDDRV - Combine the 4 argument values to form a byte controlling the LED colour and the state of the 3 front panel LEDs. Output this byte to the LED port.

5.5.5.4 SELECT (Function) - Read the front panel switch port. Return the state of the SELECT button as a boolean value.

5.5.5.5 REVIEW (Function) - Read the front panel switch port. Return the state of the REVIEW button as a boolean value.

5.5.5.6 PROG (Function) - Read the front panel switch port. Return the state of the PROGRAM button as a boolean value.

5.5.6 Module CMKNL (MACRO-80 Source)

This module contains the code associated with system reset, device initialisation and interrupt entries. Entry on system reset initialises the stack pointer and jumps to CMMAIN. Interrupt entry points are included in this description.

5.5.6.1 CTCI0 (CTC Ch 0 Interrupt) - Save context. Call STROBE. Output the returned data byte to NICAM. Reset timer channel to trigger on next strobe pulse. Restore context. Re-enable interrupts.

5.5.6.2 CTCI3 (CTC Ch 3 Interrupt) - Save context. Call TICK. IF integrity pattern is OK THEN reset watchdog timer. Restore context. Re-enable interrupts.

5.5.6.3 DISINT - Record interrupt status. Disable interrupts.

5.5.6.4 ENINT - Enable interrupts.

5.5.6.5 FOCOFF - Switch off the Fault open collector output

5.5.6.6 FOCON - Switch on the Fault open collector output

5.5.6.7 HEAD - Recover 3 arguments. Combine channel (second arg) with data length (third arg). Compute 16-bit sum over this composite and existing data in packet (start address first arg, length third arg). Combine high byte of sum with channel/length composite to give first header byte; store in packet after existing data. Store low byte of sum as second header byte after first header byte.

5.5.6.8 HSOFF - Send X-OFF character (DC3) to main or aux serial transmitter as determined by argument. Set corresponding DTR line to inactive (not ready) state.

5.5.6.9 HSON - Send X-ON character (DC1) to main or aux serial transmitter as determined by argument. Set corresponding DTR line to active (ready) state.

5.5.6.10 INIT - Store integrity check pattern in RAM. Initialise I-register and set interrupt mode 2. Set CTC chan 0 to interrupt to CTC10 50usec after the next NICAM strobe pulse. Set CTC chan 3 to interrupt to CTC13 every 10msec. Initialise DART channels. Set up DART channel 0 to interrupt to RX0 or SPEC0 on received character, special receive condition (e.g. overrun) respectively. Set up DART channel 1 similarly (RX1, SPEC1). Enable interrupts.

5.5.6.11 RESINT - Restore interrupt status prior to last DISINT call.

5.5.6.12 RX0 (DART Channel 0 Character Received Interrupt) - Save context. Input the character. Call TOQM with character as argument. Restore context. Re-enable interrupts.

5.5.6.13 RX1 (DART Channel 1 Character Received Interrupt) - Save context. Input the character. Call TOQA with character as argument. Restore context. Re-enable interrupts.

5.5.6.14 SETBR1 - Disable interrupts. Set DART channel 1 baud rate according to the integer argument. Enable interrupts.

5.5.6.15 SETBR2 - Disable interrupts. Set DART channel 2 baud rate according to the integer argument. Enable interrupts.

5.5.6.16 SPEC0 (DART Chan 0 Special Receive Interrupt) - Save context. Reset interrupting condition. Read and discard the character. Restore context. Re-enable interrupts

5.5.6.17 SPEC1 (DART Chan 1 Special Receive Interrupt) - Save context. Reset interrupting condition. Read and discard the character. Restore context. Re-enable interrupts

5.5.6.18 TXCTLH - Read and return TX Control data high byte.

5.5.6.19 TXCTLL - Read and return TX Control data low byte.

5.5.7 Module CMMENU (PASCAL/MT+ Source)

This module contains the procedures which interact with the operator for system control setting.

5.5.7.1 EXPLAIN - Display a 3-word explanation of the currently active system control item. Each word is displayed for the same predetermined time. Abort the procedure if the SELECT or REVIEW button is pressed (call SELDEB and REVDEB).

Calls SETZERO and TIMER (Channel DWELL) to control display timing, DPYNORM to display each word.

5.5.7.2 NEXTITEM - Increment the global variable ITEM, which points to the current system control item under review. IF end of list is reached THEN wrap to start.

5.5.7.3 PICKITEM - Allow the operator to choose an item to examine. Each time he pushes the SELECT button (call SELDEB), display the next item. If he holds the button down, start autorepeating items, increasing the autorepeat speed to a predetermined maximum. Exit when SELECT has been released for a predetermined time, or if the REVIEW button is pressed (call REVDEB).

DPYNORM is called to display the item text. SETZERO and TIMER (using channel DWELL) are called to control display timing.

5.5.7.4 PICKSETTING - Allow the operator to review possible settings for the current item. Each time he pushes the REVIEW button (call REVDEB), display the next setting text. Calls DPYNORM or DPYCURR according to non-current/current setting being displayed. If operator holds the button down, start autorepeating settings, increasing the autorepeat speed to a predetermined maximum. IF he presses PROGRAM (call PRGDEB), THEN (Change the system control setting to match the currently displayed setting. Call CALCRC. Copy working data to both NV RAM areas (call COPY). Check the copy CRCs. (call CHKCRC). If an error exists then call WARN with message 'REPT'. Call DPYCURR to re-display the setting as current). Exit when REVIEW and PROGRAM have been released for a predetermined time, or SELECT button is pressed (call SELDEB).

SETZERO and TIMER (using channel DWELL) are called to control display timing.

5.5.8 Module CMNVR (MACRO-80 Source)

This module contains the procedures which generate and check REDCODE CRCs and move data between working RAM and NV RAM.

5.5.8.1 CALCRC - Compute size of data area. Compute REDCODE over working data, store it after data (in global variable WKGCRC).

5.5.8.2 CHKCRC (Function) - Compute size of data area. Select start address according to the argument. Compute REDCODE over the area. Compare with stored REDCODE after data. Return TRUE if codes agree, FALSE otherwise.

5.5.8.3 COPY - Compute size of data area. Select source and destination start addresses according to the two arguments. Copy data and REDCODE from source to destination.

5.5.8.4 CRASH - Disable interrupts, halt CPU.

5.5.9 Module CMPANEL (PASCAL/MT+ Source)

This module contains procedures which allow the front panel to be accessed at a higher level than the primitive procedures in module CMIO.

5.5.9.1 CLRDEB (Function) - Call CLEAR repeatedly until the same value has been returned a predetermined number of times. Return this value.

5.5.9.2 DPYCURR - IF fault or warning flag is set THEN wait a predetermined time or until CLEAR is pressed (call CLRDEB) as appropriate, clearing the flag. (Calls SETZERO and TIMER using channel ALERT). Call FOCON. Set LEDs to indicate CURRENT status (call LEDDRV) and display the argument message (call DPYCHR).

5.5.9.3 DPYNORM - IF fault or warning flag is set THEN wait a predetermined time or until CLEAR is pressed (call CLRDEB) as appropriate, clearing the flag. (Calls SETZERO and TIMER using channel ALERT). Call FOCON. Set LEDs to indicate NORMAL status (call LEDDRV) and display the argument message (call DPYCHR).

5.5.9.4 FAULT - Set the front panel LEDs to indicate a fault (call LEDDRV). Display the argument message (call DPYCHR). Call FOCOFF. Set fault flag.

5.5.9.5 PRGDEB (Function) - Call PROG repeatedly until the same value has been returned a predetermined number of times. Return this value.

5.5.9.6 REVDEB (Function) - Call REVIEW repeatedly until the same value has been returned a predetermined number of times. Return this value.

5.5.9.7 SELDEB (Function) - Call SELECT repeatedly until the same value has been returned a predetermined number of times. Return this value.

5.5.9.8 WARN - IF fault flag is not set THEN (Set the front panel LEDs to indicate a warning (call LEDDRV). Display the argument message (call DPYCHR). Call FOCON. Set warning flag).

5.5.10 Module CMTEXT (PASCAL/MT+ Source)

This module defines all text associated with the operator menu.

5.5.10.1 TEXTDEFINE - Set up all the text and class fields for the menu options, explanations and setting options.

5.5.11 Module COMBINER (PASCAL/MT+ Source)

This module functions as the "main program". It will eventually perform routine "background" tasks (e.g. system testing), and control operator access. All other system activity is initiated by interrupts.

5.5.11.1 CMMAIN - Clear fault and warning flags. IF working data is not valid (call CHKCRC) AND one of the non-volatile copies is OK THEN call COPY to load the NV data, ELSE initialise all the working data and text arrays to default settings (call TEXTDEFINE). Call QINIT. Call INIT. Call SETBR1 and SETBR2 to initialise the serial port baud rates. Then enter a "forever" loop which calls DPYNORM (displaying the source ident code for this combiner), CHKCRC (if this fails, call CRASH) and SELDEB in turn, until SELDEB returns TRUE signifying operator intervention. Call PICKITEM, EXPLAIN and PICKSETTING to allow operator to inspect and/or change a system control item, then resume the "forever" loop.

6 MAINTENANCE

IMPORTANT NOTE - The ADZE 2 module must be isolated for testing by the removal of the ribbon jumper between PLB and PLE. (This isolates everything except the power supply to the ADZE 2 module). The module may then be tested in accordance with D.D.H.B. No. 6.267(85). Note that the power consumption will be higher than normal, because the custom half of the PCB is still connected to the supply.

The remainder of this section describes testing of the rear half of the Combiner card, assuming a correctly functioning ADZE 2 module.

6.1 Test apparatus required

Stabilised power supply, 5V limited to 1A
Dual-trace Oscilloscope, 25MHz bandwidth
Signature analyser, Hewlett Packard 5004A or similar
Test jigs to DSK26739A3

Throughout the test sequence the front panel display '> ' is a prompt inviting the operator to press PROGRAM to continue with the next test.

6.2 Power connection

6.2.a Plug the unit into the test jig and switch on the supply. Measure the current consumption.

6.2.b Current should be in the range 600..800mA

6.2.c If less, check the distribution of both +5V and ground to all ICs. If more, look for short circuits between +5V and ground, or signs of overheating.

6.3 PROM, RAM and alphanumeric display

6.3.a Remove P4602 and replace with P4604 (IC6).

Upon switch-on the green CPU LED on the front panel should flash continuously with a period of about 1 sec. Press PROGRAM and hold down for one second. A checksum test will be carried out on the PROM followed by a full read/write test on the RAM.

The test sequence will only start if these initial tests have been passed.

6.3.b

(i) The CPU LED should stay ON

(ii) The alphanumeric display should read:-
'0000' for 2 sec.
then '****' for 2 sec. followed by '> '

6.3.c

If the CPU LED continues to flash, check:-

(i) that LK1-LK3 are correctly configured.

(ii) the wiring from LK2 to S4.

(iii) that IC6-IC8 are correctly inserted into their sockets.

(iv) the redcode of IC6. (This should be 1E8B).

If the CPU LED stays on but reverts back to flashing once the prompt is displayed, then suspect IC20 and the 40-way ribbon connector between PLB and PLE.

If the alphanumeric display is wrong check that it has been inserted into its holder correctly. If the display is blank (and hot) it is likely to be wrongly orientated.

6.4 Front Panel Pushbuttons

6.4.a Press PROGRAM to continue.

Press each pushbutton in turn (starting from the top) when prompted by the display. For example in the first instance the display will read 'PRES' 'CLR '.

6.4.b As each button is pressed the display should read 'OK ' before inviting you to press the next button. When all buttons have been tested the '>' prompt should be displayed.

6.4.c If there is no response when a button is pressed check that the switch has been inserted into the PCB the correct way round. Note that a display showing '????' means that the wrong button has been pressed.

6.5 Front Panel LEDs

6.5.a Press PROGRAM to continue.

6.5.b The LEDs should light sequentially from top to bottom; first with the colour RED, followed by YELLOW, and finally GREEN. The alphanumeric display should display the name of the current colour.

6.5.c If two or more LEDs light simultaneously check for solder bridges on both PCBs especially in the vicinity of PLC and 2SK1.

If the colour of any LED does not match the current colour shown in the display check:-

(i) the orientation of the LED

(ii) the values of R1-R5 on PCB no.2.

6.6 Nicam Data output

6.6.a Press PROGRAM to continue

6.6.b The LEDs marked D0 - D7 on the test jig should light in sequence starting with D0.

6.6.c If one or more outputs fail, check that WRREQ pulses reach IC25 p11 and IC26 p11, and that these ICs are being enabled (pin 1). Check also IC27 and IC28.

Note that these outputs are open-collector outputs with pull-up resistors inside the test jig.

6.7 Fault output

6.7.a Press PROGRAM to continue

6.7.b Following the name of the test, the red FAULT LED on the test jig should light for approx. 3 sec.. During this time the front panel display should read 'F ON'. The LED should then go out with the message 'FOFF' displayed for a further 3 sec..

6.7.c If the FAULT output is not toggled suspect IC25 or IC27. Check that WRREQ pulses reach IC25 p11 and that enable pulses reach p1.

Note that this output is also open-collector with its pull-up resistor within the test jig.

6.8 Transmitter address input (8-bit)

6.8.a Press PROGRAM to continue.

6.8.b Each address bit will be toggled in turn, and if all eight bits are received correctly then 'OK' should be displayed.

Since the NICAM data output bits are used as a source of dummy addresses, the LEDs labelled D0-D7 on the test jig will show a burst of activity during the test.

6.8.c If 'FAIL' is displayed check that IC32-IC35 carry +5V on pins 1,4 and 8. In this condition not all of the LEDs D0-D7 are likely to be on. The LED which was last to come on corresponds to the failed address bit, and so indicates which of IC32-IC35 should be checked first. Interrupt the power suppy to remove the FAIL condition. Check that during this test there are RDREQ pulses on IC22 p19 and enable pulses on p1.

6.9 Transmitter Control data input (16-bit)

6.9.a Press PROGRAM to continue.

6.9.b Each data bit will be toggled in turn and if all sixteen bits are correctly received then 'OK' should be displayed.

Since the NICAM data output bits are used as a source of dummy TX control data (first inputing to one 8-bit port and then the other) the LEDs labelled D0-D7 on the test jig will again show a burst of activity during the test.

6.9.c If 'FAIL' is displayed check that IC36-IC43 carry +5V on pins 1,4,and 8. Again, the state of the LEDs D0-D7 indicates which of these ICs should be checked first. Note that dummy data is input to the low byte first (associated with IC36-IC39) followed by the high byte (IC40-IC43).

Interrupt the power supply to remove the FAIL condition and check that during this test there are RDREQ pulses on pin 19 of IC23 and IC24 and that enable pulses reach pin 1.

6.10 Hard handshake outputs

6.10.a Press PROGRAM to continue.

6.10.b The MAIN hard handshake LED on the test jig should light for approx. 2 secs. then switch off for a further 2 secs. Its current status should be described in the front panel display.

The AUX hard handshake LED will then be tested in the same way.

6.10.c If the LEDs do not respond check that the TTL level changes on IC21 p16 (MAIN) or IC21 p25 (AUX). Suspect IC29 (MAIN) or IC30 (AUX).

6.11 Serial data channels

6.11.a Press PROGRAM to continue.

6.11.b

Main channel:
The display should read 'OK'.

Press PROGRAM

Aux. channel:
The display should read 'OK'.

The end of the test sequence is marked by a flashing 'END' message in the display. If it is required to return to the beginning of the sequence, this can be done by pressing CLEAR.

6.11.c If 'FAIL' is displayed, restart the sequence by interrupting the power supply and check that during this test a burst of RS232 data reaches PLA2 (MAIN) or PLA8 (AUX) whilst the front panel display is blank. This should appear simultaneously on IC29 p2 (MAIN) or IC30 p2 (AUX). Check that IC21 is receiving positive going timing pulses from the CTC on pins 13,14, and 27. These should be 0.2microsec. +/- 0.05microsec. wide with a repetition rate of 6.5microsec. +/- 1microsec..

This completes the Test Procedure. Replace P4604 with P4602.

6.12 Software maintenance

You should read and understand the entire section on software, and study the program modules themselves before attempting any software modifications - despite its physical size, this is not a trivial system!

The master files are held on the same magtape volume as the DSR master for this handbook. The version history of each module must be updated with full details of any permanent changes, as must the descriptions in this handbook. Also remember that every source module has a correponding definition module which must be kept in agreement.

APPENDIX A

DISPLAY MESSAGES

Status message (displayed during normal operation):

xxxx	Ident code of this combiner (see menu IDNT options)

Fault messages (accompanied by open collector signal):

NVR	Non-Volatile RAM (unable to recover correct settings - defaults used)
MOFL	Main queue OverFLow (RDS source did not respond to handshake - some serial data lost)
AOFL	Aux queue OverFLow

Warning messages:

REPT	REPeaT (when using the PROGRAM key, settings were not copied successfully to non-volatile RAM - try again)

Menu messages:

Select	(Explanation)	Review/Program
BR 1	RDS BAUD RATE	300/ 600/1200/2400/4800/9600
BR 2	AUX BAUD RATE	300/ 600/1200/2400/4800/9600
LEDS	COLS FROM TOP	RRG+/RYG+/RGG+/YYG+/YGG+/ RRR-/YYY-/GGG- (+ means active on, - active off)
SDPY	MESS DISP TIME	INST/FHWI/HOLD (FHWI= Faults Hold, Warnings Inst)
IDNT	SRCE IDNT CODE	BH01/BH02/BH03/BH04/BH05/BH06/ BH07/BH08/BH09/BH10/BH11/NH12/ BH13/BH14/BH15/BH16/BH17/BH18/ BH19/BH20/BH21/BH22/BH23/BH24/ GEN1/GEN2/GEN3/GEN4
DEST	CTRL ADRS CODE	ALLS/ALLT/ENGD/WALS/SCOT/ULST/GW

APPENDIX B

PACKET FORMAT

Byte 1	<Packet data>	
...	...	
Byte N	<Packet data>	
Byte N+1	Bits 7..5	<Checksum bits 10..8>
	Bits 4..3	<Packet type>
	Bits 2..0	<Data length, N>
Byte N+2	<Checksum bits 7..0>	

Notes:

i) Checksum is the binary sum of the N data bytes and byte N+1, with the checksum field of the latter set to zero.

ii) Main Serial Data packets (type 0) have data length N in the range 1..7. Data from consecutive main serial packets constitute a transparent stream of bytes.

iii) Auxiliary Serial Data packets (type 1) are similar to Main serial packets.

iv) Transmitter Control Data packets (type 2) have N=4 and a fixed data byte format:

Byte 1	<Combiner Ident Code>
Byte 2	<Splitter Address Code>
Byte 3	<TXCTRL data high byte>
Byte 4	<TXCTRL data low byte>

Ident and Address codes start at zero, and are numbered in the same sequence as the options displayed in the setup menu.

v) Packet type 3 is not used.

INDEX

IC CIRCUIT REFERENCE	TYPE	SUPPLY CONNECTIONS		
		+5V	0V	-5V
IC 1	LS14	14	7	
IC 11	LS08	14	7	
IC 16	LS32	14	7	

PLD
SA test points
clock 1
clock 2
start stop
ground

PLB (see note)

D60153A1

IC1c IC1d IC1e IC1a IC1b

XL1 9-83MHz C1 60p C2 390p C3 100p C4 33p C5 33p C21 330nF C6–C19 100n C20 4.7

R1 12k R2 15k R3 1k R4 7·5k R5 220 R6 1·2k R7 22 R8 1k R9 330 R10 1k R11 1k R12 1k R13 4×330 R14 4×330 R15 8×1k R16 22k

TR1 BC109 TR2 2N3906

IC2a LS74A IC3 MC74HC4040 IC4 MC74HC4040 LK4 SEC 1/2 1/4 1/8

watchdog reset

PLC CPU normal LED output port LED outputs IC17 LS273 switch input port switch inputs IC18 LS541

IC5 Z80B CPU

Memory address decoder IC10a LS139 IC11a

IC6 27128N 0000–7FFF IC7 5565PL/15 8000–BFFF IC8 5565PL/15 C000–FFFF

LK3 LK2 10k LK1

port group decoder IC12 LS138 CO–DF AO–BF 80–9F 60–7F 40–5F 20–3F 00–1F

address buffer IC15 LS541

data bus buffer IC9 LS245

SKA RS232 IC19 NM232CD

data bus MSB LSB

write-only gate IC10b LS139 FC–FF F8–FB

internal port decoder IC13 LS138 F0–F3 EC–EF E8–EB E4–E7 E0–E3 port group decodes

IC16a IC16b IC16c IC16d mem RD mem WR 10 RD 10 WR

IC14 LS139 4 INT ACK 10 EXTL RD IC11b

E0–FF decode

WRREQ RDREQ A1 A0 MI NMI INT RESET CK WAIT WR RD IORQ

Parts list -D60154A4

SCALE :- 0

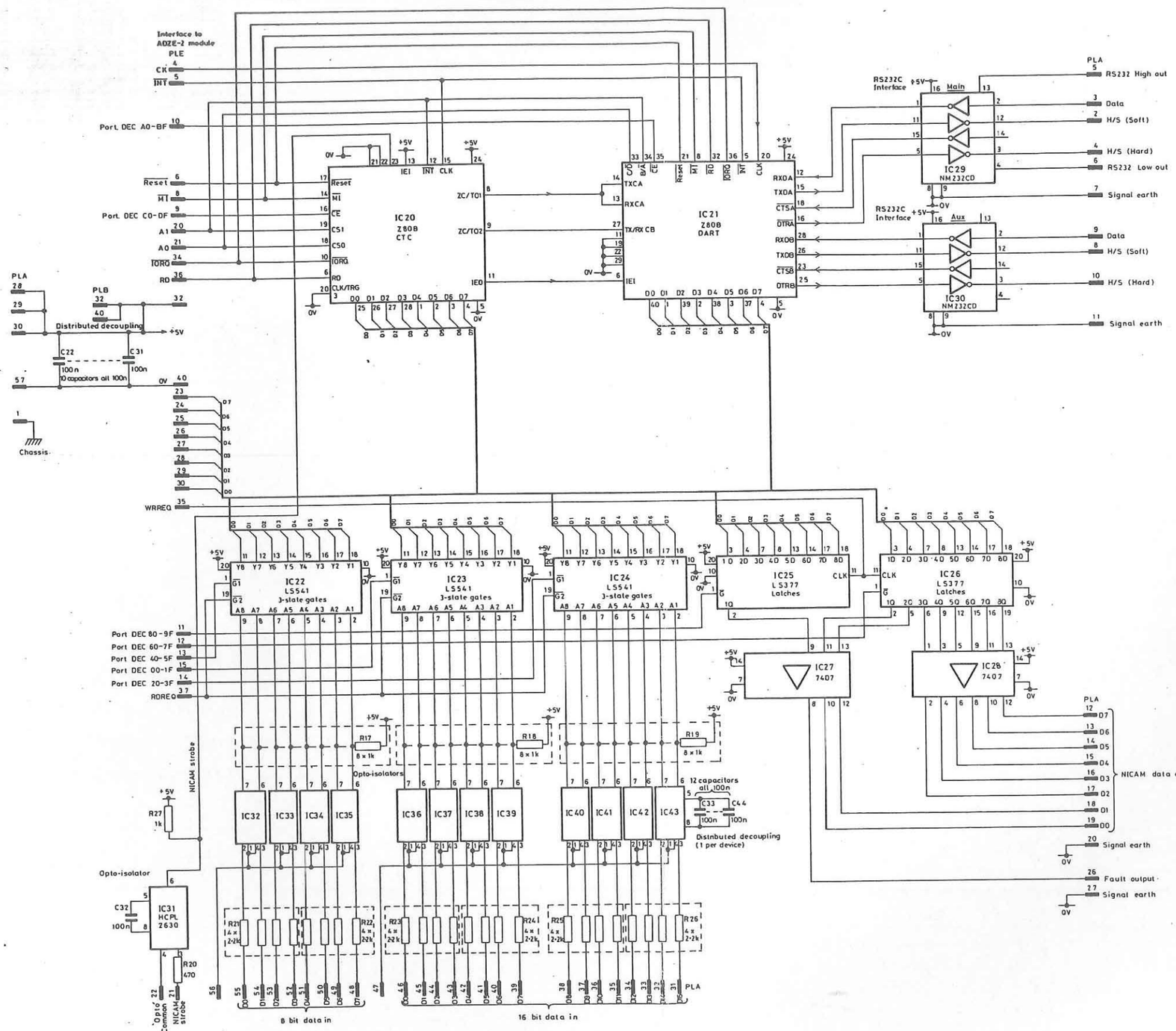
THIRD ANGLE PROJECTION | ORIGINAL FRAME SIZE 574mm x 821mm | CHANGE

(ADAPTABLE Z80 HALF CARD (ADZE) MK II)

CD4S/17
NICAM DATA COMBINER CIRCUIT

All dimensions in millimetres unless otherwise stated. Normal tolerances: no decimal places ± 1 mm unless; one decimal place ± 0·3 mm otherwise; two decimal places ± 0·1 mm stated

DRN	I.L.	DESIGNS DEPARTMENT
TCD		D60153A1
CKD		Sheet 1 of 2 sheets
APPD	JK	



IC ref	Type	Supply connection		
		+5V	0V	+5V
IC31	HCPL2630	8	5	
IC32-IC43	HCPL2731	8	5	

SCALE – 0

Parts List D60154A4

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE 574mm x 821mm

BBC

DS/A1/1

ISS	CHANGE
A	13-8-86 Date
B	17-11-86
C	4-2-87

NICAM DATA COMBINER

CD4S/17

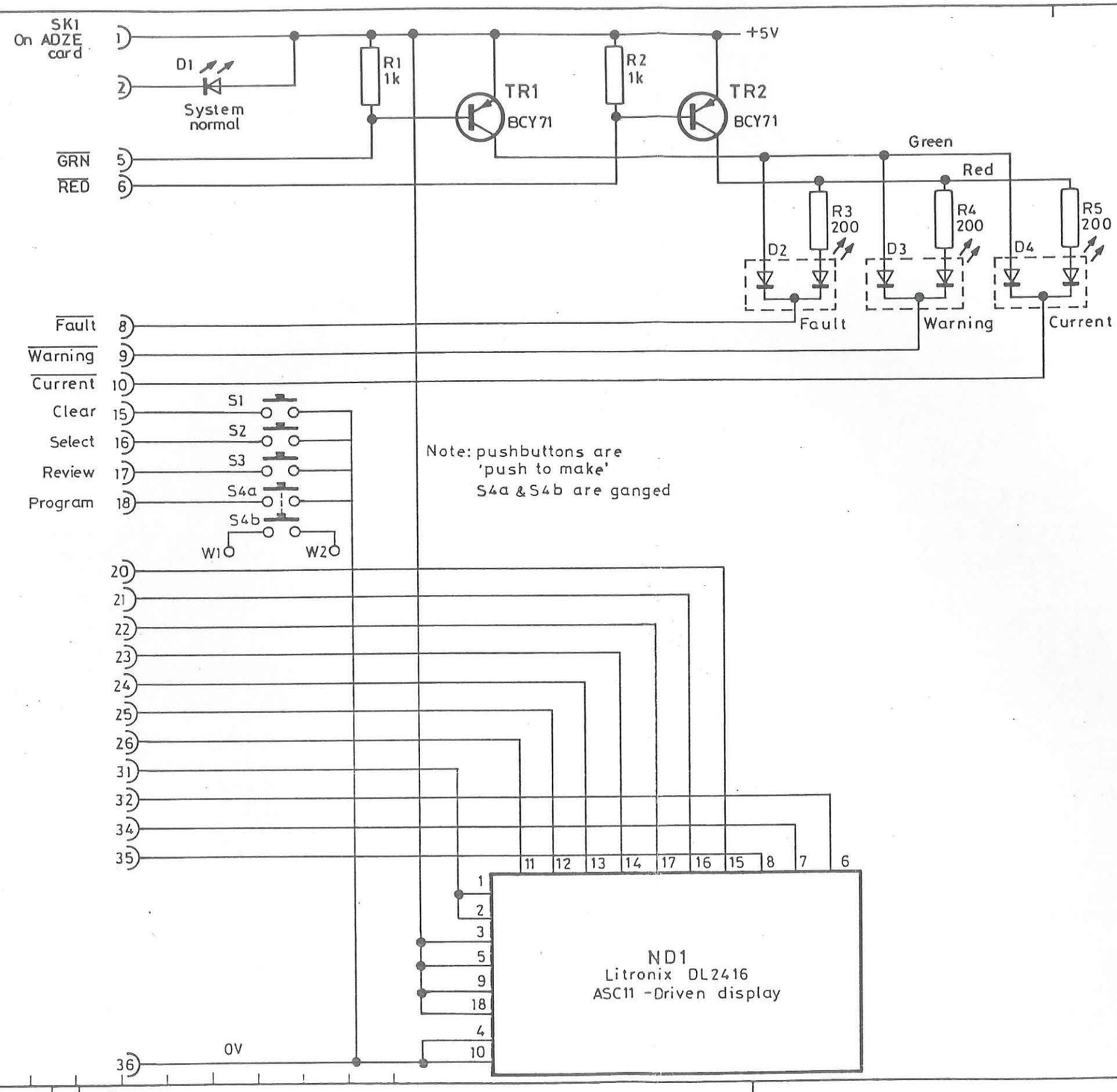
CIRCUIT

All dimensions in millimetres unless otherwise stated. Normal tolerances: no decimal place — ± 1 mm unless; one decimal place — ± 0·3 mm otherwise; two decimal places — ± 0·1 mm stated

DRN		DESIGN & EQUIPMENT DEPARTMENT
TCD	ART	D60153A1
CKD		Sheet 2 of 2 sheets
APPD	JK	

S & H LTD L6682A

D60153A1



THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE
277mm x 400mm

BBC

DS/A3/1

ISS	CHANGE
A	17-11-86

NICAM 3 DATA COMBINER / SPLITTER

CD4S/17 & 18

BOARD NO2

All dimensions in millimetres unless otherwise stated. Normal tolerances:
no decimal place — ± 1 mm unless
one decimal place — ± 0·3 mm otherwise
two decimal places — ± 0·1 mm stated

DRN.		DESIGN & EQUIPMENT DEPT.
TCD.	A.R.T.	D60170A3
CKD.		
APPD.	JR	

A3 F Royal Ltd

ISS	CHANGE
1	18-11-86
2	21-11-86

ITEM No	No. OFF		DESCRIPTION	C'C'T REF.	B B C REF. OR DRG. No.
			DRAWING NUMBERS		
			CIRCUIT (2 SHEETS) P.B.No1 D60153A1		
			PARTS LIST D60154A4		
			ASSEMBLY & WIRING D60155A2		
			DETAILS D60156A2		
			P.B. MASTERS No1 (PHOTO-PLOT) D60157A3S		
			P.B. DRILLING No1 D60158A3		
			ENHANCED COMP. LOC. No1 D3K26157A3		
			P.B. MASTER No2 (PHOTO-PLOT) D60306A3S		
			ENHANCED COMP. LOC. No2 D3K26235A3		
			P.B. DRILLING No2 D60307A3		
			FRONT PANEL LEGEND D60160A2		
			CIRCUIT P.B. No2 D60170A3		
			FURTHER INFORMATION REQUIRED FOR MANUFACTURE		
			UNIT WIRING INFORMATION EA10140		
			UNIT ASSEMBLY INFORMATION EA10484		
			SPEC ED/CD4S/17		
1	1	*+	CODING PLATE, 4U		0326593
			SLOT POSITIONS ARE 5, 9, & 25 MODIFIED BY		
			E.D. WORKSHOPS BEFORE ISSUE TO CONTRACTOR		D60156A2 DET.
2	1	*	CH1/64A FRONT PANEL		0326613
			MODIFIED BY CONTRACTOR TO:-		D60156A2 DET.
3	1	*	HANDLE		
			ENGRAVED BY CONTRACTOR TO:-		D60156A2
4	1	*	THUMBSCREW		0326656
5					
6	1	*+	EARTHING WASHER		0400310
7					
8	1	*+	NYLON BUSH		040102X
9					
10	2	*	MOUNTING BLOCK		0351590
11					
12	1	*	PRINTED BOARD No1		D60157A3
			TO SPEC. ED/PB/C043/17/1/P.T.H.		0608693
13					
14	1	*	PRINTED BOARD No2		D60306A3S
			TO SPEC. ED/PB/C043/17 & 18/2		0611358
15					
16					
17	3	*	SWITCH SPDT C&K 8121-S-H-C-7527-2		0610377
18	1	*	SWITCH DPDT C&K 8225-S-H-C-7527-3		0612398
19					
20	1	*	LIGHT EMITTING DIODE GREEN	D1	0465653
21	3	*	LIGHT EMITTING DIODE TRI-COLOUR CQX95	D2-4	0608930
22	1	Δ	DISPLAY FILTER 25X35 MADE FROM ITEM 23		
23	1	*+	POLARISED DISPLAY FILTER RS. No 586-548		0611461
24	1	*	ALPHANUMERIC DISPLAY LITRONIX DL2416		0525749

BBC

DS/PLA4/1

CD4S/17
NICAM DATA COMBINER
PARTS LIST

DRN.	J.H.
TPD.	
CKD.	
APPD.	AKL

DESIGN & EQUIPMENT DEPT

D60154 A4

SHEET 1 OF 6 SHEETS

CHANGE	ISS.
18-11-86	1

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
25	2	*+	SPACER, ROUND 5mm, M2.5 CLEAR		0207465
26	1	*+	SPACER, ROUND INSULATING 5mm LG. TAPPED M2.5		0325677
27					
28					
29					
30					
31	1	*	CABLE ASSEMBLY D60159A3		0610902
32					
33					
34					
35					
36					
37					
38					
39	17	*	I.C. SOCKET, TRANSMISSION 8 POLE		0445453
40	2	*	I.C. SOCKET, TRANSMISSION 14 POLE		0445461
41	2	*	I.C. SOCKET, TRANSMISSION 16 POLE		040704X
42	7	*	I.C. SOCKET, TRANSMISSION 20 POLE		0439423
43	4	*	I.C. SOCKET, TRANSMISSION 28 POLE		0445043
44	2	*	I.C. SOCKET, TRANSMISSION 40 POLE		0445488
45	4	*	SNAP-OFF SOCKET STRIP 20WAY HARWIN D01-997-01		0608949
46	1	*	NON VOLITILE RAM SOCKET DS1213		0611453
47					
48					
49					
50	4	*	DIL PIN HEADER 8 PIN		0446469
51					
52					
53					
54					
55					
56					
			CAPACITORS		
57	1	*	47nF 25V ELECT	IC20	037540X
58	37	*	100nF 50V CERAMIC FILM	IC6-IC19, IC22-IC44	0204648
59	2	*	33pF 100V SINGLE PLATE	IC4 IC5	0429820
60	1	*	100pF 63V P.C.B. MOUNTING	IC3	0449968
61	1	*	390pF 125V P.C.B. MOUNTING	IC2	0450104
62	1	*	330nF 50V MULTILAYER	IC21	038983X
63					
64					
65					
66					
67					
68					
69					
70					
71					
72					
73	1	*	60pF MAX, 250V VARIABLE	IC1	0333683
74					
75					

BBC

DS/PLA4/1

CD4S/17
NICAM DATA COMBINER
PARTS LIST

DRN.	J.H.
TPD.	
CKD.	
APPD.	ARL

DESIGN & EQUIPMENT DEPT.

D60154 A4

SHEET 2 OF 6 SHEETS

ISS	CHANGE
1	18-11-86

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
76					
77					
78					
79					
80					
			RESISTORS		
81	1	*	22Ω 2% 0·4W	1R7	0098976
82	1	*	220Ω 2% 0·4W	1R5	0099023
83	1	*	330Ω 2% 0·4W	1R9	0099031
84	8	*	1·0KΩ 2% 0·4W 2R1, 2R2, 1R3, 1R8, 1R10, 1R11	1R12, 1R27	0099082
85	1	*	1·2KΩ 2% 0·4W	1R6	0099102
86	1	*	7·5KΩ 2% 0·4W	1R4	0228027
87	1	*	12KΩ 2% 0·4W	1R1	0228043
88	1	*	15KΩ 2% 0·4W	1R2	0099370
89	1	*	22KΩ 2% 0·4W	1R16	0228078
90	4	*	8X 1·0KΩ S.I.L. RESISTOR NETWORK 1R15, 1R17-	1R19	0427980
91	6	*	4X 2·2KΩ S.I.L. RESISTOR NETWORK 1R21-	1R26	0428192
92	2	*	4X 330Ω S.I.L RESISTOR NETWORK 1R13	1R14	0428141
93	1	*	470Ω 2% 0·4W	1R20	0099047
94	3	*	200Ω 2% 0·4W 2R3-	2R5	0099015
95	1	*	10KΩ 2% 0·4W		0099224
96					
97					
98					
99					
100					
101					
102					
103					
104					
105					
106					
107					
108					
109					
110					
			TRANSISTORS		
111	1	*	2N3906	1TR2	0122804
112	1	*	BC109	1TR1	0112282
113	2	*	BCY71	2TR1-2	0112798
114					
115					
116					
117					
118					
119					
120					
121					
122					
123					
124					
125					

BBC

CD45/17
PARTS LIST

DRN.	J.H.
TPD.	
CKD.	
APPD.	ARC

DESIGN & EQUIPMENT DEPT.

D60154A4

SHEET 3 OF 6 SHEETS

A&F Royal Ltd

ISS 1

CHANGE 18-11-86

ITEM No.	No. OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
			INTEGRATED CIRCUITS		
			CAUTION STATIC SENSITIVE DEVICES		
			HANDLE WITH CARE		
126					
127	1	*	DIC 74LS08N	1IC11	0178362
128	2	*	DIC 74LS138N 1IC12	1IC13	0184526
129	2	*	DIC 74LS139N 1IC10	1IC14	0173926
130	1	*	DIC 74LS14N	1IC1	0188604
131	1	*	DIC 74LS245N	1IC9	0196698
132	1	*	DIC 74LS273N	1IC17	0191151
133	1	*	DIC 74LS32N	1IC16	0178843
134	5	*	DIC 74LS541N 1IC15,1IC18,1IC22,1IC23	1IC24	0508019
135	1	*	DIC 74LS74AN	1IC2	018212X
136	2	*	SSD/MC 74HC4040 1IC3	1IC4	0521269
137	1	*	Z80B-CPU	1IC5	0519585
138	1	*	Z80B-DART	1IC21	0525757
139	1	*	Z80B-CTC	1IC20	0506913
140	3	*	NM232CD RS232 CONVERTER 1IC19,1IC29	1IC30	0523070
141	2	*	DIC 74LS377N 1IC25	1IC26	0182111
142	2	*	DIC 7407N 1IC27	1IC28	0153497
143	1	*	HCPL2630 OPTO ISOLATOR	1IC31	0502188
144	12	*	HCPL 2731 OPTO ISOLATOR 1IC32-	1IC43	0505443
145	1	*+	SSD/27128N-250NS	1IC6	0516366
146	2	*	DIC TC556SPL/15 1IC7	1IC8	0526230
147					
148					
149					
150					
151					
			CRYSTALS		
152	1	*	3.83MHz: INTERFACE QUARTZ DEVICES HC18-U		0485861
153					
154					
155					
156					
157					
			PLUGS		
158	2	*	SINGLE ROW, 36 PIN SHROUDLESS HEADER		0457322
159	2	*	FIXED I.D.C. 40 WAY		0491343
160					
161					
162					
			SOCKETS		
163	1	*	6 POLE RIGHT ANGLE MOLEX TYPE A38-00-1306		0494022
164	1	*	36 POLE HARWIN M20-989-36-05		0609047
165					
166					
167					
168					
169					
170					

BBC

DS/PLA4/1

CD43/17
PARTS LIST

DRN.	J.H.	DESIGN & EQUIPMENT DEPT.
TPD.		D60154 A4
CKD.		
APPD.	ARL	SHEET 4 OF 6 SHEETS

ISS.	CHANGE
1	18-11-86

ITEM No.	No OFF		DESCRIPTION	C'C'T REF.	BBC REF. OR DRG. No.
171					
172					
173					
174					
175					
176					
			SCREWS		
177	8		M2·5 x 6LG. PAN HD. M.S. ZN. PL.		
178	1		M2·5 x 5LG. CSK HD. M.S. ZN. PL.		
179	2		M2·5 x 10LG. CSK HD. M.S. ZN. PL.		
180	2		M3 x 6 LG. INST. HD M.S. CR. PL.		
181	2		M3 x 10 LG. INST. HD. M.S. CR. PL.		
182					
183					
184					
185					
186					
187					
188					
			NUTS		
189	2		M2·5, HEX. FULL. M.S. ZN. PL.		
190	4		M3, HEX. FULL. M.S. ZN. PL.		
191					
192					
193					
194					
195					
			WASHERS		
196	10		M2·5 PLAIN M.S. ZN. PL.		
197	4		M3 SHK. PROOF. M.S. ZN. PL.		
198					
199					
200					
201	A/R	*+	WIRE PUFI/3M WHITE		0201524
202	A/R	*+	WIRE PUFI/3M BLUE		020147X
203	A/R		WIRE 1MM B.T.C.		
204	A/R		WIRE 0·6MM B.T.C.		
205	1	*	FOAM PACK		0342743

* Denotes items supplied to the contractor on embodiment loan.
*+ Denotes items supplied to the contractor on embodiment loan, requiring special costing or supply action by B.B.C.
θ* Denotes components supplied and fitted by B.B.C. on test.
θ+ Denotes coded plug in units supplied and fitted by B.B.C. on test.
Ø Denotes items supplied and fitted by B.B.C. on installation.

BBC

CD45/17
PARTS LIST

DRN.	J.H.	DESIGN & EQUIPMENT DEPT.
TPD.		D60154A4
CKD.		
APPD.	ARL	SHEET 5 OF 6 SHEETS

DS/PLA4/1

A & F Royal Ltd

SHT	ISS	DETAILS OF CHANGE	SHT	ISS	DETAILS OF CHANGE
1	2	ITEM 17 DESCRIPTION REVISED. ITEM 18 C/M No. WAS 0610385 J.H. 21-11-86			

DESIGN & EQUIPMENT DEPARTMENT

CODE CD45/17 21-11-86

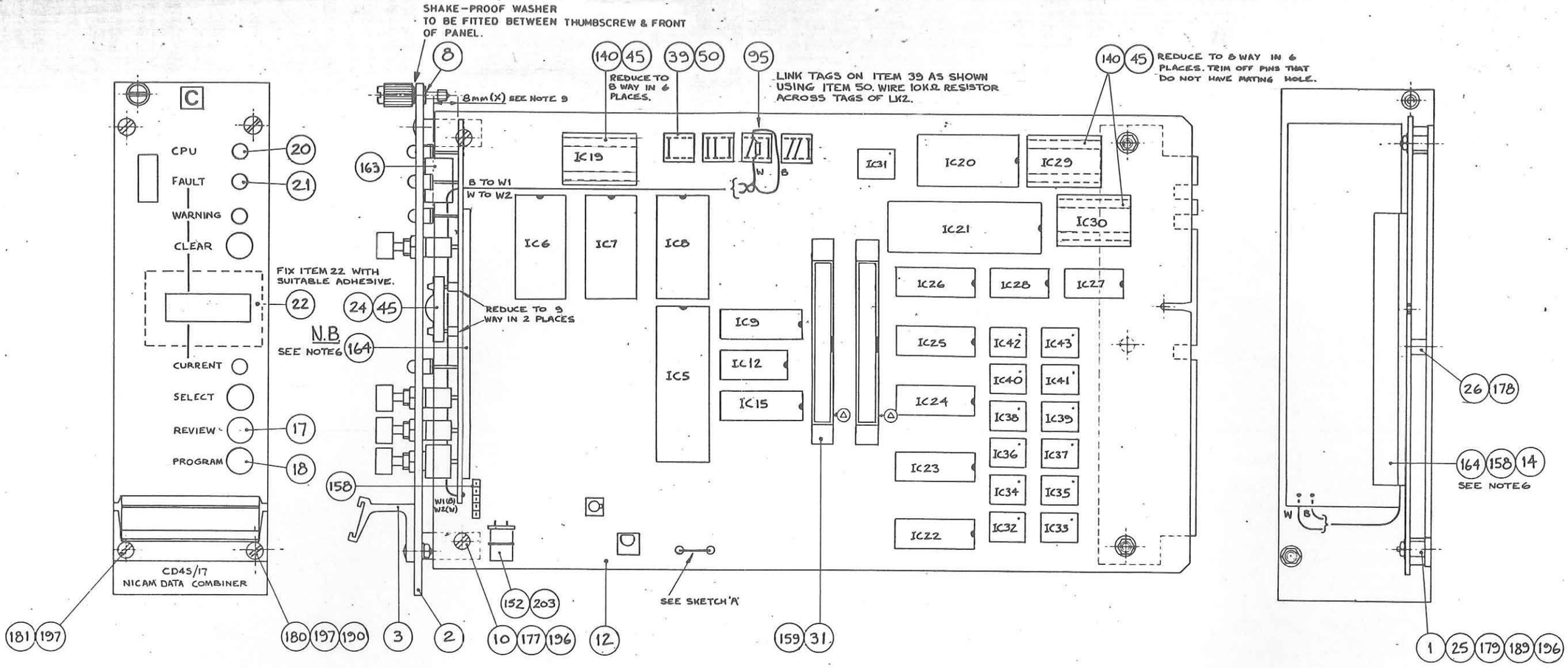
D60154 A4

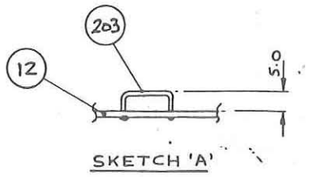
BBC

DS/SPA4

PARTS LIST CHANGE RECORD ISSUE:- 2

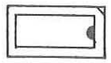
SHEET 6 OF 6 SHEETS





SKETCH 'A'

10. I.C'S NOT SHOWN ARE FITTED DIRECTLY INTO BOARD WITH OUT I.C. SOCKETS. ORIENTATED AS SHOWN:



NOTES:

1. ASSEMBLY TO BE IN ACCORDANCE WITH EA10484 NOTES 1,7.
2. COMPONENTS TO BE WIRED TO PRINTED BOARD IN ACCORDANCE WITH EA10140 NOTES 1,7,9&16
3. I.C.S. SHOWN NUMBERED TO HAVE I.C. SOCKETS FITTED (ITEM Nos 35-45)
4. I.C. No7 TO BE FITTED INTO ITEMS 43 & 46
5. MAXIMUM SOLDERING TIME OF 201-204 260°C-5 SECONDS
6. ITEM 164 TO BE FITTED TO WIRING SIDE OF BOARD 2
7. SI-S4 (P.B. No2) NC NO C CORNER LINE TO INDICATE PIN MARKED 'C'
8. DI-D4 (P.B. No2) CORNER LINE TO INDICATE FLAT ON DIODE
9. DIMENSION 'X' TO BE 8mm (DISTANCE BETWEEN BACK FACE OF DIODES & P.B. No2.)

CIRCUIT – D60153A1
PARTS LIST:- D60154A4

PN1/29J SCALE:-1:1 0 150

THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE 400mm x 574mm

BMM184A2/2

ISS	CHANGE
1	18-11-86
2	26-11-86

CD4S/17 ASSEMBLY & WIRING

All dimensions in millimetres unless otherwise stated
Normal tolerances:
no decimal place — ±1 mm unless
one decimal place — ±0·3 mm otherwise
two decimal places — ±0·1 mm stated

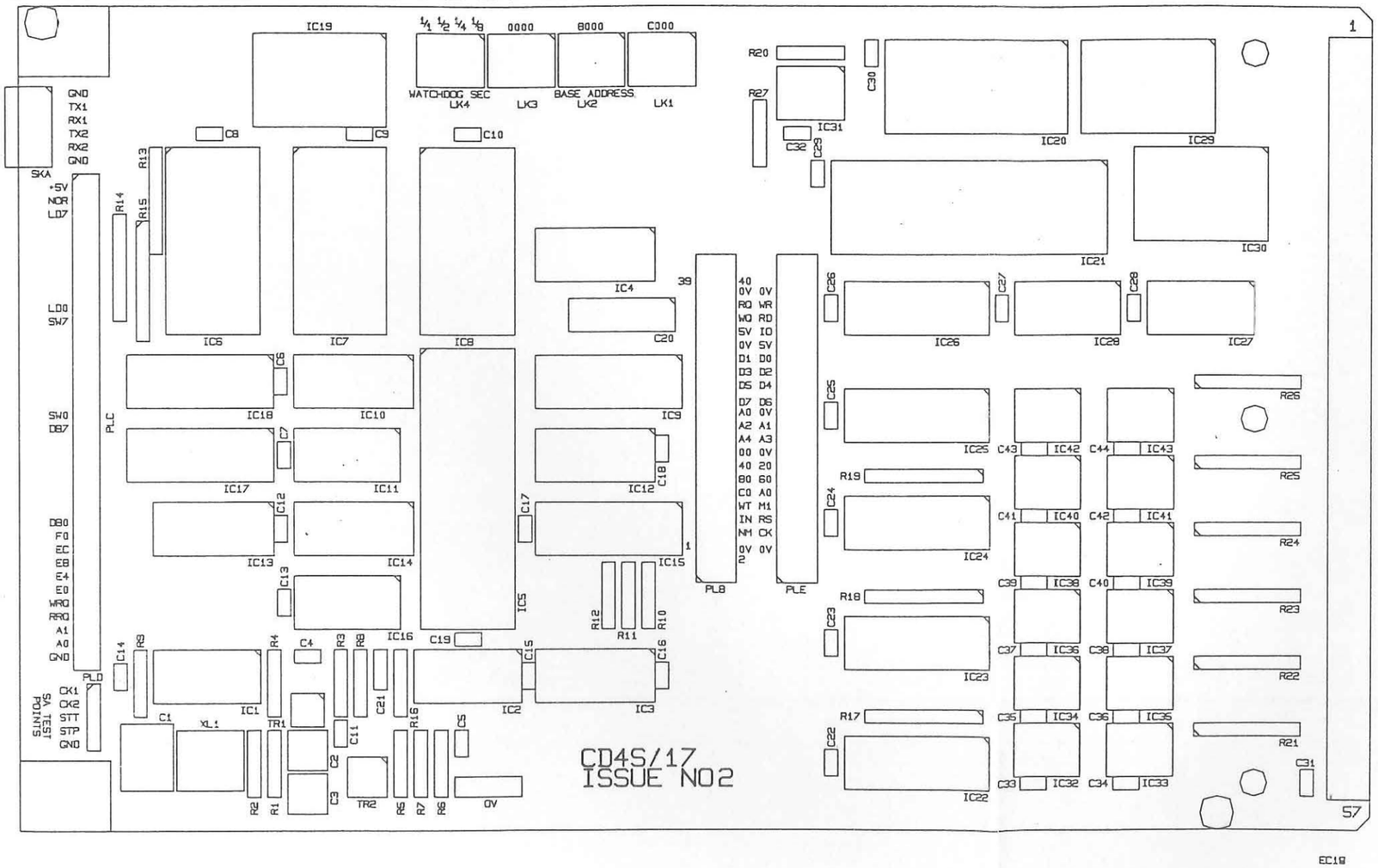
DRN	J.K.
TCD	
CKD	
APPD	ARL

DESIGN & EQUIPMENT DEPT.

D60155A2

S&H LTD L5064

CD4S/17
ISSUE NO2
PTH BOARD 01 3456789



01 3456789

SCALE:- 1:1

Original Frame Size	BBC
VM552A3 277mm x 400mm	DS/A3

CHANGE	ISS.
5-11-86	2

Issue no. of this drawing must be the same as the photo-master issue.

ENHANCED COPY OF COMP. LOC. PHOTO PLOT

CD4S/17

P.B. Nº1

DRN.	TCD.	CKD.	APPD.
J.H.			ARL

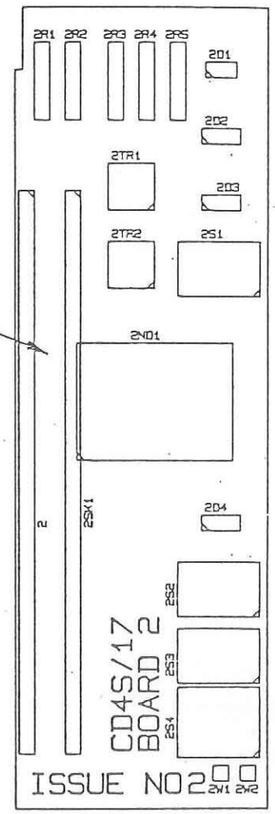
DESIGN & EQUIPMENT DEPT.

DSK26157A3

CD4S/17
BOARD 2
ISSUE NO2
PTH BOARD

N.B.

2 SK1 ITEM 164 ON PARTS LIST TO BE FITTED TO WIRING SIDE OF BOARD.



01 3459867

SCALE:- 1:1

Original Frame Size

VM552A3 277mm x 400mm

CHANGE

24-10-86

Issue no. of this drawin must be the same as t photo-master issue.

ENHANCED COPY O
COMP. LOC. PHOTO PL

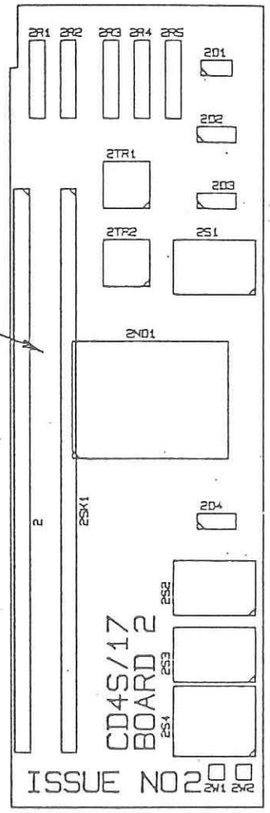
CD4S/17
P.B.Nº2

DRN.	TCD.	CKD.	A
J.H.			

DESIGN & EQUIPMENT DEP

DSK26235A

CD4S/17
BOARD 2
ISSUE NO2
PTH BOARD



N.B.

2 SK1 ITEM 164 ON PARTS LIST TO BE FITTED TO WIRING SIDE OF BOARD.

01 3459867

SCALE:- 1:1

	Original Frame Size		B
V.M552A3	277mm x 400mm		DS
CHANGE			
24-10-86			

Issue no. of this drawing must be the same as th photo-master issue.

ENHANCED COPY OF
COMP. LOC. PHOTO PLO

CD4S/17
P.B. Nº2

DRN.	TCD.	CKD.	APP
J.H.			AK

DESIGN & EQUIPMENT DEPT

DSK26235A

Pin no.*		Pin no.		Pin no.	
1.	Chassis earth	20.	Signal earth	39.	16-bit data in D7
2.	Soft handshake o/p (MAIN)	21.	NICAM strobe in	40.	· · · D6
3.	Data i/p (MAIN)	22.	Opto-iso. common	41.	· · · D5
4.	Hard handshake o/p (MAIN)	23.	N.C.	42.	· · · D4
5.	RS232 high o/p (MAIN)	24.	—	43.	· · · D3
6.	RS.232 low o/p (MAIN)	25.	N.C.	44.	· · · D2
7.	Signal earth (MAIN)	26.	Fault out	45.	· · · D1
8.	Soft handshake o/p (AUX)	27.	Signal earth	46.	· · · DØ
9.	Data i/p (AUX)	28.	+5V	47.	Opto. iso. common.
10.	Hard handshake o/p (AUX)	29.	+5V	48.	8-bit address in D7
11.	Signal earth (AUX)	30.	+5V	49.	· · · D6
12.	NICAM data out D7	31.	16-bit data in D15	50.	· · · D5
13.	· · · D6	32.	· · · D14	51.	· · · D4
14.	· · · D5	33.	· · · D13	52.	· · · D3
15.	· · · D4	34.	· · · D12	53.	· · · D2
16.	· · · D3	35.	· · · D11	54.	· · · D1
17.	· · · D2	36.	· · · D10	55.	· · · DØ
18.	· · · D1	37.	· · · D9	56.	Opto. iso. common.
19.	· · · DØ	38.	· · · D8	57.	OV

*Wiring side is connected to component side.

ORIGINAL FRAME SIZE 190mm x 277mm

THIRD ANGLE PROJECTION

All dimensions in millimetres unless otherwise stated:
Normal tolerances:
no decimal place — ± 1 mm unless
one decimal place — ± 0·3 mm otherwise
two decimal places — ± 0·1 mm stated

SCALE 0

CHANGE 17-8-87

ISS

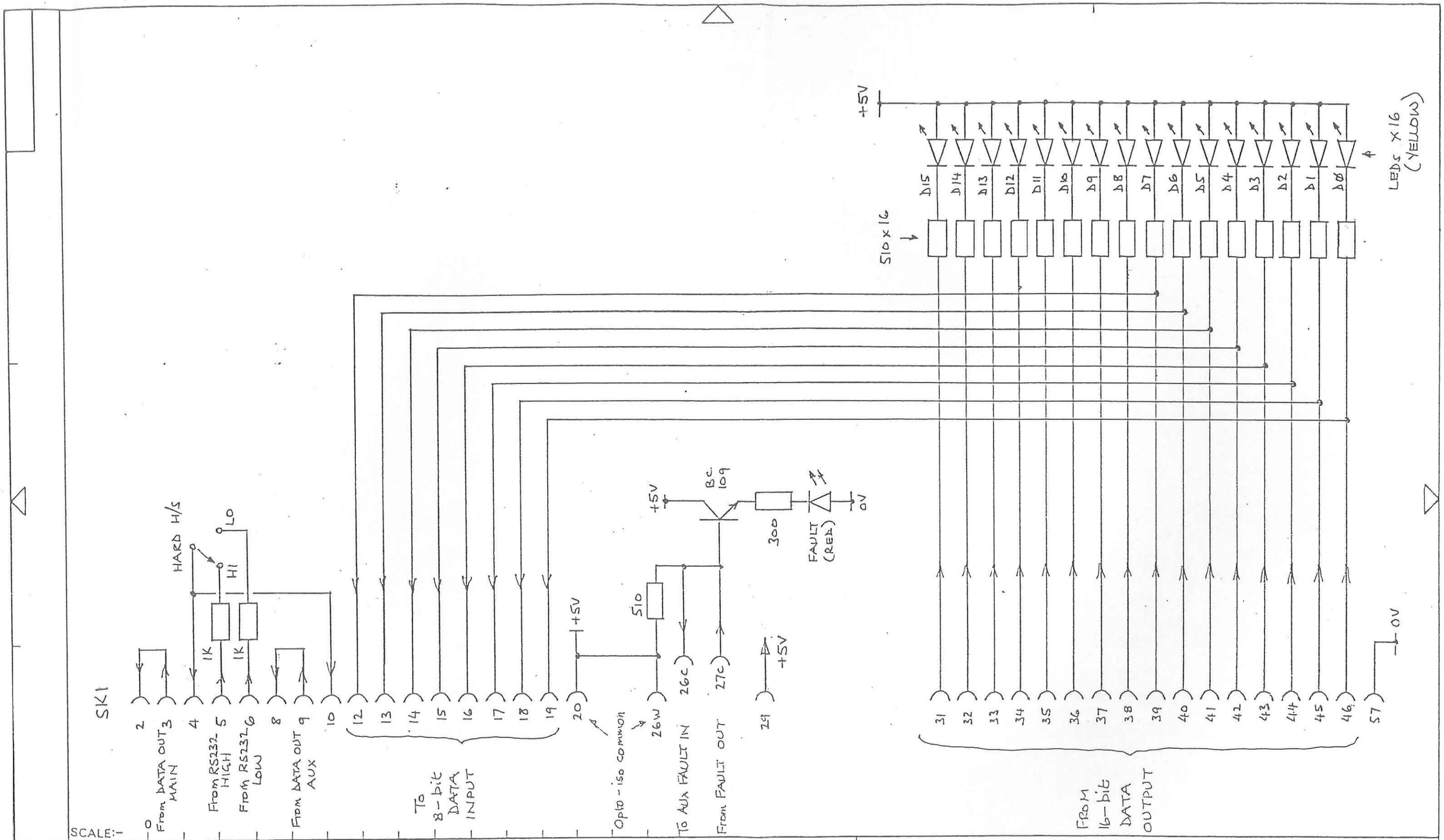
CD45/17 NICAM DATA COMBINER

CONNECTOR PIN-OUT

DRN.	DND	D & ED
TCD.		DSK 26737 A4
CKD.		
APPD	DND	

BBC

DS/A4



THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE
277mm x 400mm

ISS | CHANGE | 17-8-87

TEST. BOX FOR NICAM DATA SPLITTER.

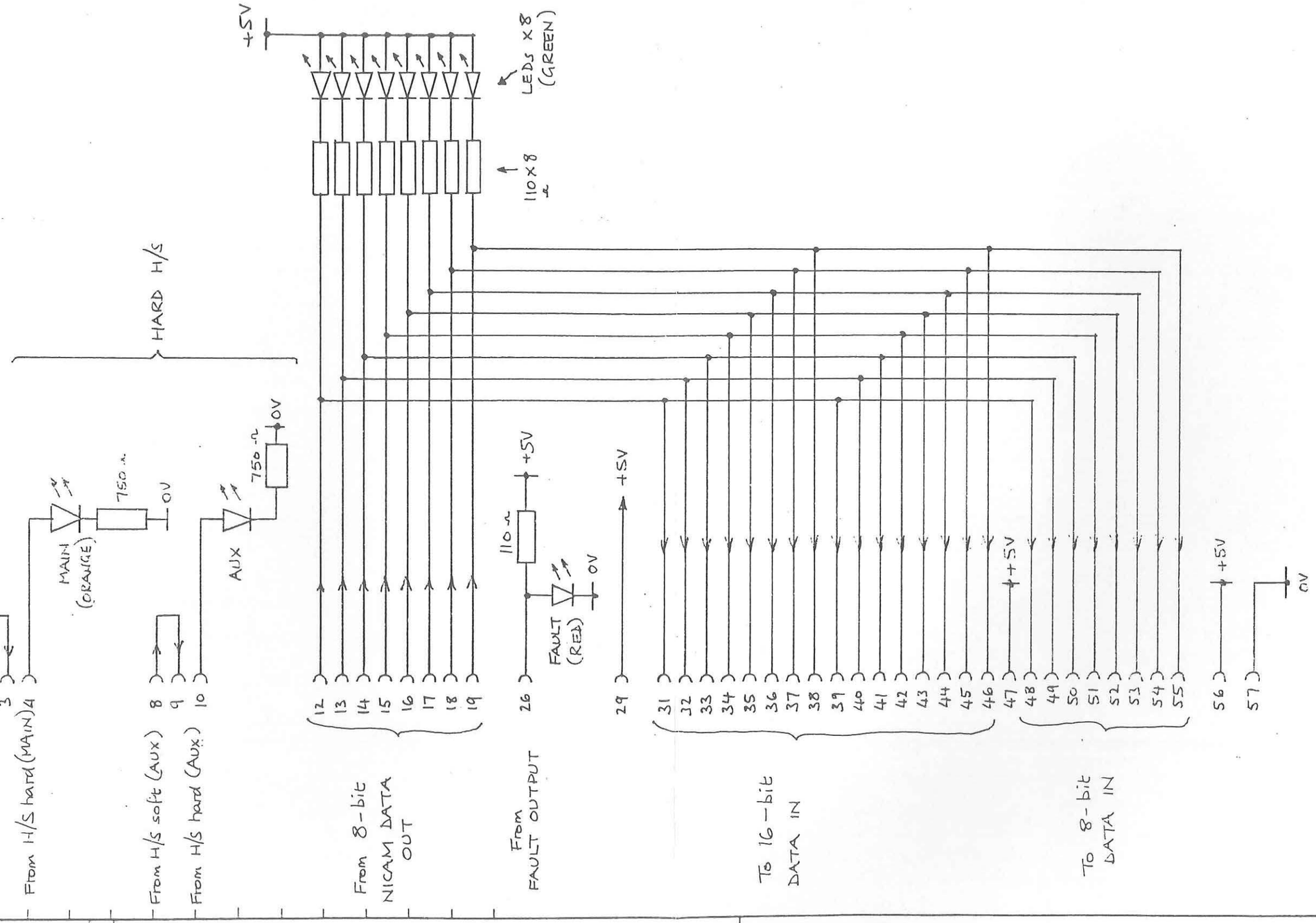
All dimensions in millimetres unless otherwise stated: Normal tolerances:
no decimal place — ± 1 mm unless
one decimal place — ± 0·3 mm otherwise
two decimal places — ± 0·1 mm stated

DRN.	DND
TCD.	
CKD.	
APPD	DND

D & ED

DSK 26740 A3

S & H L7308A



THIRD ANGLE PROJECTION

ORIGINAL FRAME SIZE
277mm x 400mm

CHANGE ISS 17 - 8 - 87

TEST BOX FOR NICAM DATA COMBINER.

All dimensions in millimetres unless otherwise stated Normal tolerances:
no decimal place — ± 1 mm unless
one decimal place — ± 0·3 mm otherwise
two decimal places — ± 0·1 mm stated

DRN.	DNA	D & ED
TCD.		DSK 26739A3
CKD.		
APPD	DNA	

DS/A3/1

S & H L7308A