SYNC PULSE GENERATION

INTRODUCTION

This information sheet describes the generation of pulse waveforms required to produce the 625-line (System I) television signal. These pulse waveforms are themselves generated by a 'Television Waveform Generator' (which is its official BBC title), but it is called a 'sync pulse generator', or S.P.G., by most broadcast engineers and throughout this information sheet.

Broadcast sync pulse generators use medium- and small-scale integrated circuits, although a single chip s.p.g. is available and, at the time of writing, is used for C.C.T.V. and Domestic Video.

This information sheet therefore provides an outline of the common techniques used in current broadcast s.p.g.'s.

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1. PULSE GENERATION PRINCIPLES - THE BISTABLE METHOD.

The pulse outputs of an s.p.g. are binary signals, having only two voltage levels for each signal. An S.R. bistable can be used to generate each required waveform, as follows:-

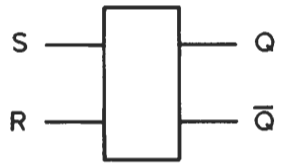

Fig. 1.1. S-R Bistable.

A pulse on the 'Set' input causes Q to assume logic '1'. Q will remain at logic '1' until a pulse is applied to the Reset i/p, when it changes to logic '0'. Using +ve logic, the waveforms are as shown in Fig. 1.2.

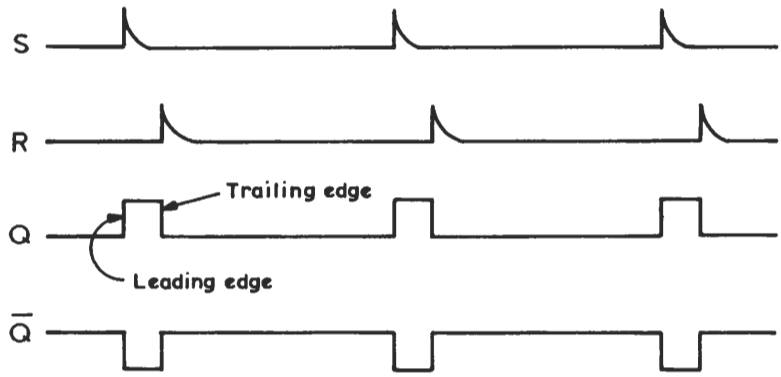

Fig. 1.2. Typical Signals for the S.R. Bistable.

The important fact from Fig. 1.2 is that the short pulses fed to S and R define transitions, or edges, in the output waveform from Q, and are therefore called 'edge timing pulses'.

Pulses fed to the 'Set" input define the leading edge timing, and pulses fed to 'Reset' define the trailing edge timing of the Q output waveform.

Sync pulses are conventionally distributed as low-active signals, and it is useful to note that the inverse of the Q output is always available from $\overline{Q}$.

2. EDGE TIMING PULSE GENERATION.

The highest repetition rate contained in the s.p.g. outputs occurs when equalising and broad pulses are being generated at 2H rate. (H is the horizontal scan frequency).

An Edge Timing Generator is therefore clocked at 2 x H rate, its outputs being a number of pulses, of suitable timing relative to each other, which can be used as leading and trailing edge triggers for the s.p.g. outputs.

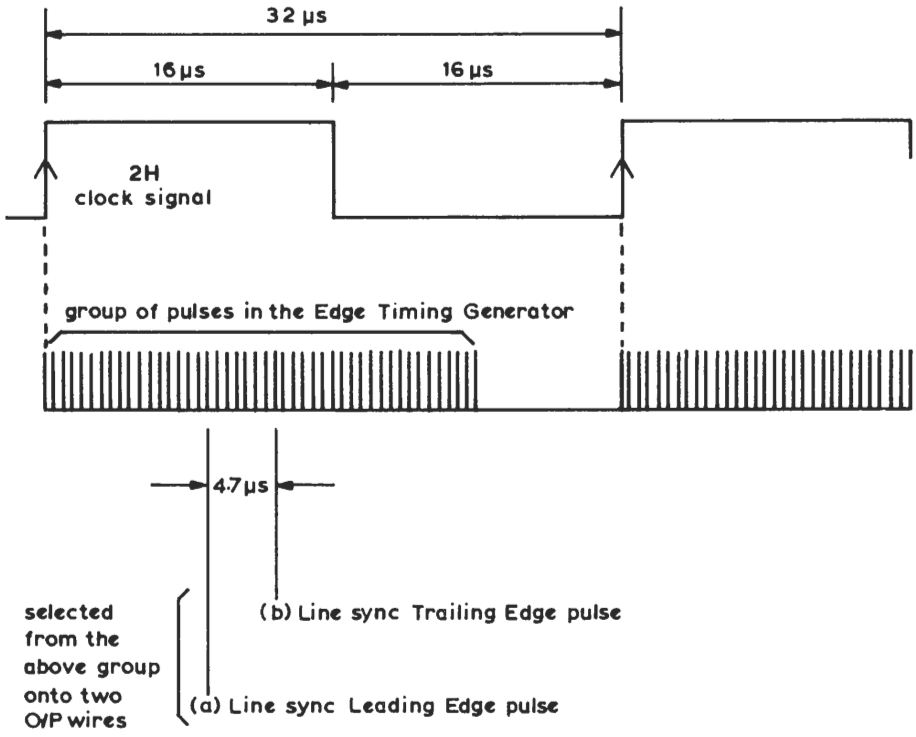

Fig. 2.1. Generation Principles for Edge Timing Pulses.

By a selection process within the Edge Timing Generator, a pulse at time (a) is routed out to be the leading edge trigger for line syncs. A pulse 4.7µs later (b) is selected and routed out as trailing edge trigger for line syncs.

The other outputs of the Edge Timing Generator supply start (leading edge) and finish (trailing edge) pulses for the other components of the sync waveforms.

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As a simple example, take line drive, which has a start pulse 1.7μs early on line sync start, and a finish pulse 4.8μs late on line sync start. (Note that line sync leading edge is used as a reference for time measurement across a television line. It is often referred to as t = 0.)

3. INHIBIT GATING.

The Edge Timing Generator produces all start and finish pulses at 2H rate. If they are required at a lower rate, e.g. to give line (H) or field (V) rate outputs, then they are gated with an inhibit waveform to remove unwanted edge timing pulses.

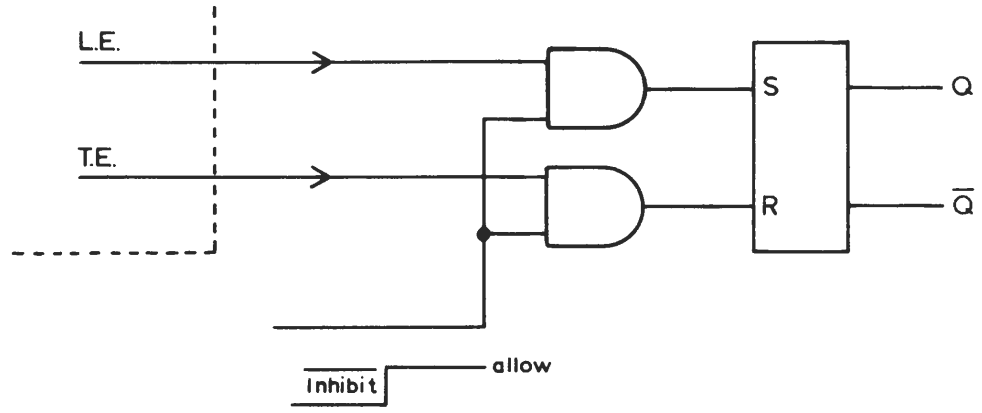

Fig. 3.1. Ideal Inhibit Gating for Line Drive.

For our example of line drive, every other set and reset trigger must have no affect; the inhibit waveform is therefore a line rate square wave.

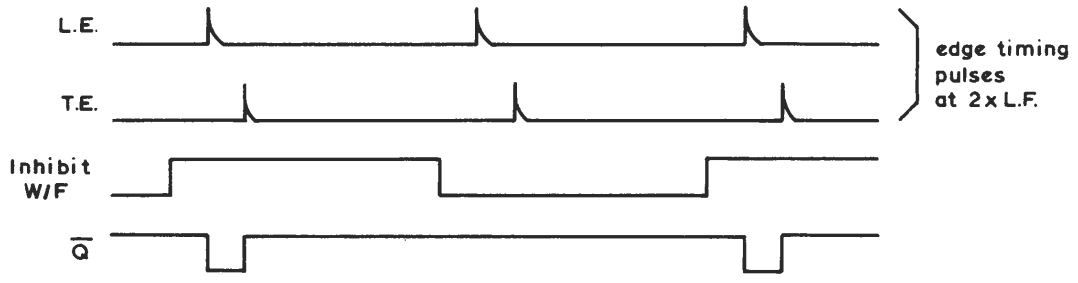

Fig. 3.2. Waveforms for L.D. Generation

Note that the timing of inhibit waveform is not critical, as long as the gates are open for one pair of pulses and closed for the next pair.
The circuit of Fig. 3.1 uses two 'And' gates, but it is possible to reduce the hardware by not inhibiting the reset input of the bistable.

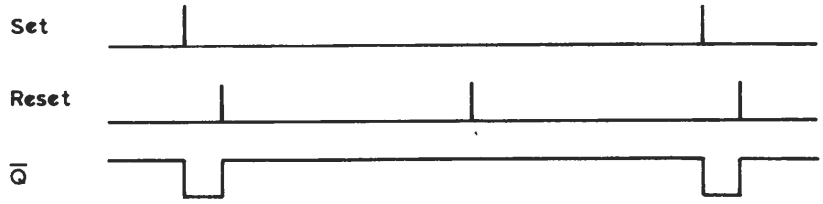

Fig. 3.3. Waveforms at the Bistable in Fig. 3.4.
The bistable ignores the second reset pulse since it is already reset. So, one gate is saved.

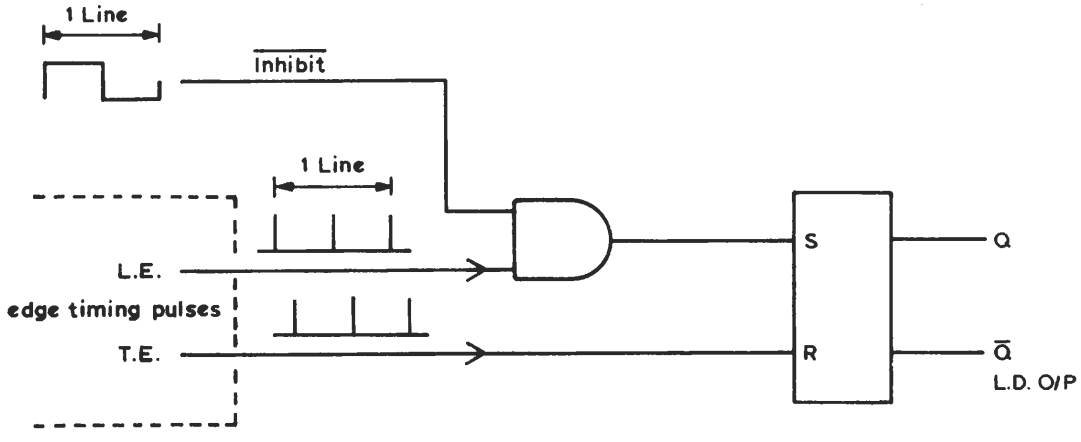

Fig. 3.4. Practical Line Drive Circuit.
For Mixed Syncs, the edge triggers used to set and reset the bistable must be changed to give different pulse widths and repetition rates during the field sync period. Field rate inhibit waveforms are produced in a Field Divider. This is clocked by the SAME 2H frequency which drives the edge timing generator, and is divided by 625 to give 50Hz inhibit waveforms.

4. BLOCK SCHEMATIC OF AN SPG

The separate components of the SPG form the block diagram of Figure 4.1.

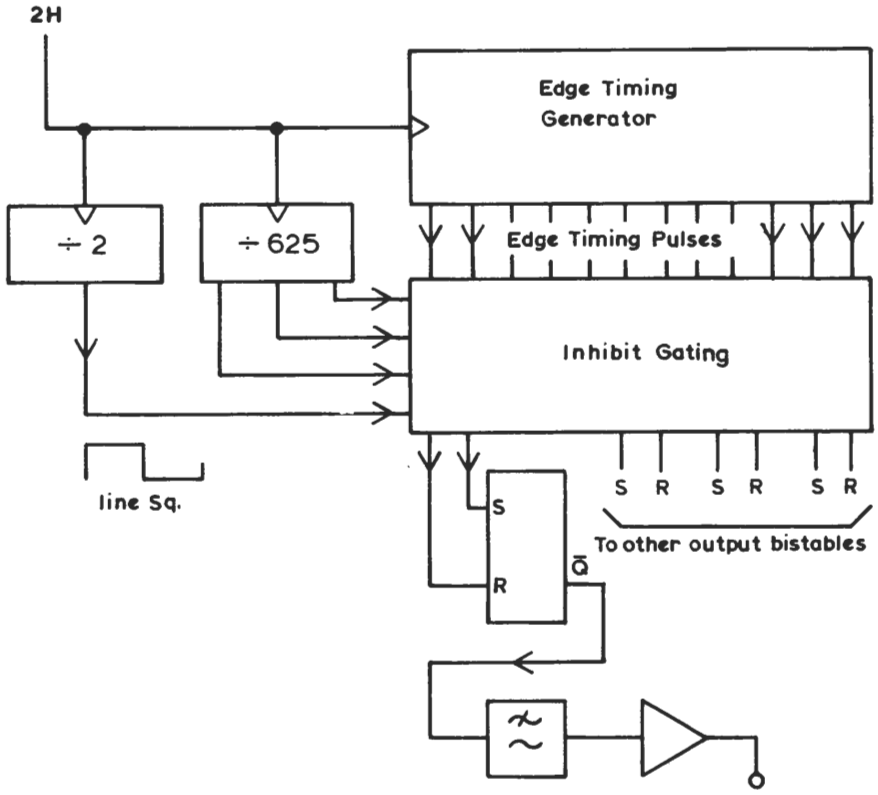

Figure 4.1. A General SPG Block Diagram

The 2 x H frequency drive may come from either an external drive source, or from a stable internal oscillator.

Most current sync pulse generators contain a high-frequency crystal oscillator, (from which PAL subcarrier frequency may also be derived,) which is divided down to generate the 2 x H frequency clock for the edge timing generator and the line and field dividers.

The majority of the sync pulse generator circuits are implemented using standard logic families, TTL, CMOS etc. The output pulses have to meet different specifications regarding level, impedance, rise-time etc., typical parameters are 2V pk-pk into 75Ω with a rise time of around 200-250ns. To meet these specifications the logic signals are filtered and buffered by the output stages.

The remainder of this information sheet takes a more detailed look at the circuitry of the sync pulse generator and gives examples of techniques in current use.

5. DERIVATION OF THE 2H SIGNAL

Having established a basic s.p.g. block diagram the next step is to derive the necessary input signals. Although this might appear to mean only the 2H signal required by the pulse generating circuits it is as well to remember the need for colour subcarrier (csc) as well. The reason for this is that the subcarrier and line frequencies produced by the s.p.g. must be related according to the PAL formula:

$$CSC = (283.75 + 1/625)H$$

The justification for which was explained in a previous lecture.

5.1 Establishing the CSC/H Relationship

Fixing a relationship is one thing, achieving it is another. As a first step however it is not difficult to suppose that for considerations of stability both should be derived from the same oscillator. Figure 5.1 shows this.

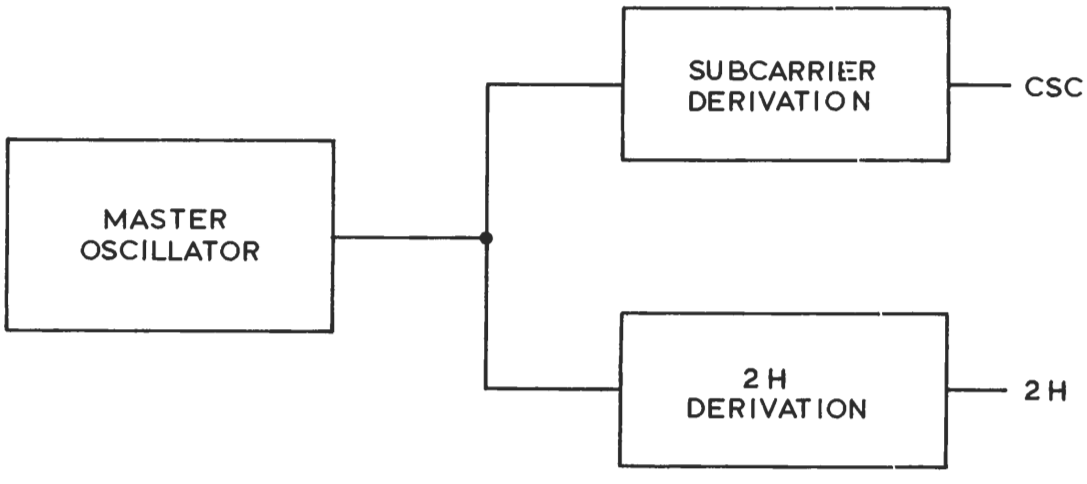

Fig. 5.1 Basic Technique for Deriving CSC and 2H

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Different manufacturers naturally vary as to just how they do it but most choose an oscillator frequency that is related to the colour subcarrier. In this handout two s.p.g.s in common use will be examined - manufactured by Philips and Seltech respectively.

5.2 The Philips Approach

The Philips LDK4215 s.p.g. is fairly common throughout the BBC, it takes up little bay space (only 1U high), has genlock facilities, inbuilt test signal and (optional) colour bar generators and is well suited to colour black installations. Its master oscillator runs at PAL subcarrier frequency, with 2H derived from it by means of a phase locked loop (PLL).

The problem with a PLL in this case is finding two signals correctly related which can be compared in order to produce an error signal for the VCO. Philips have produced a custom IC to carry out this function. Although it would be perfectly feasible to regard such a device as a "black box" some insight into its operation will be beneficial.

An important starting place however is to know that there is a second custom IC in the s.p.g. This one generates all the pulse waveforms, together with some signals for the PLL. It requires a drive frequency of 160H.

Basically the Philips PLL manipulates a few aspects of the relationship between csc and line frequencies to obtain two identical frequencies for comparison. Consider:

$$CSC = (283.75 + 1/625)H \quad \text{or}$$
$$= (283.7516)H \quad \text{or}$$
$$= (70.9379) \times 4H$$

The number (709379) is familiar in another context, however what Philips do is derive from the subcarrier a frequency of 10H. This is then compared with a 10H signal derived directly from the 160H oscillator which drives the pulse generating IC. The process is shown in figure 5.2 below. (Note that in practice there is a lot more to the IC than that - all multi-standard switching has been omitted for example).

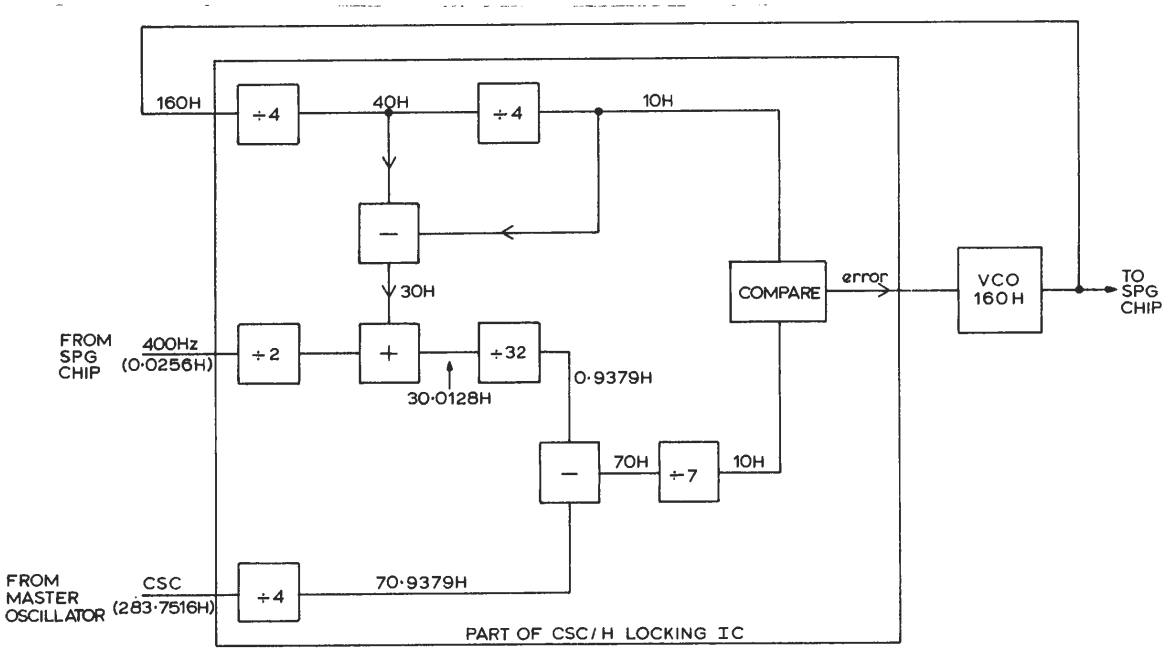

Fig. 5.2 Philips CSC/H Locking

5.3 The Seltech Approach

The Seltech s.p.g. is also used in quite large numbers, but there are probably fewer of these than the Philips. It is a 2U s.p.g., has genlock and colour bar generation facilities and although conscious of the PAL eight field sequence is not quite so well equipped to cope with it as the Philips.

Seltech use an oscillator at 4 times csc. This modifies the relationship to line frequency as follows :

CSC = (283.75 + 1/625)H or
= (283.75)H + 25Hz thus
CSC X 4 = 1135H + 100Hz

This means that there is no longer a problem associated with the quarter cycle per line as with csc, however the question of what to do about the PAL offset (now 100Hz) still remains. The Seltech solution to the problem is to capitalise on one of those Trigonometric relationships that you've long since forgotten! Figure 5.3 below shows the basic arrangement used to remove the 100Hz offset.

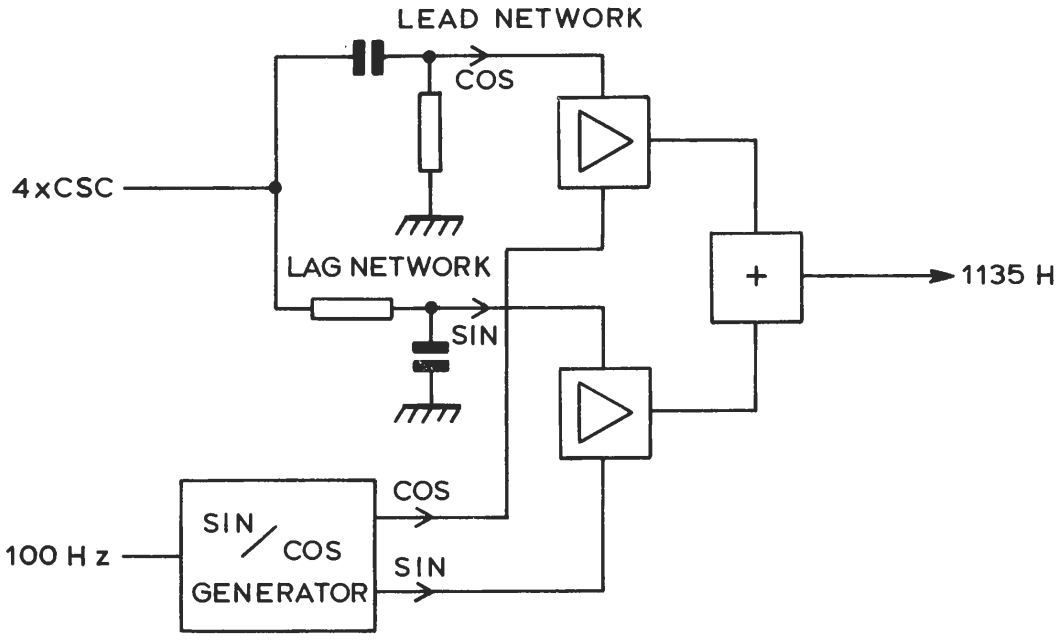

Fig. 5.3 Seltech Removal of 100Hz Offset

4 x CSC is processed by RC networks to derive two feeds having a sin/cos relationship. These provide one of the inputs to each of two balanced modulators. The other modulator inputs are at 100Hz, and also have a sin/cos relationship. If one remembers that a modulator is basically a multiplier and assuming the two signals to be simply A and B then the relationship is :

$$\text{OUTPUT} = \text{SinA} \times \text{SinB} + \text{CosA} \times \text{CosB}$$
$$= \text{Cos}\ (A-B)$$

which if we regard the 4 x CSC as A and the 100Hz as B becomes:

$$\text{OUTPUT} = 4 \times \text{CSC} - 100\text{Hz} = 1135\text{H}$$

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The 1135H is divided by 5 to 227H (about 3.55MHz), at which point a VCO is provided in a relatively long time constant PLL in order to reject any phase jitter introduced by the offset removal process. The VCO output is divided by 113.5 to derive 2H. This process involves a programmable counter dividing by 113, however the input clock frequency is inverted on completion of each count cycle, thus contributing the half. Figure 5.4 below shows this together with some other details.

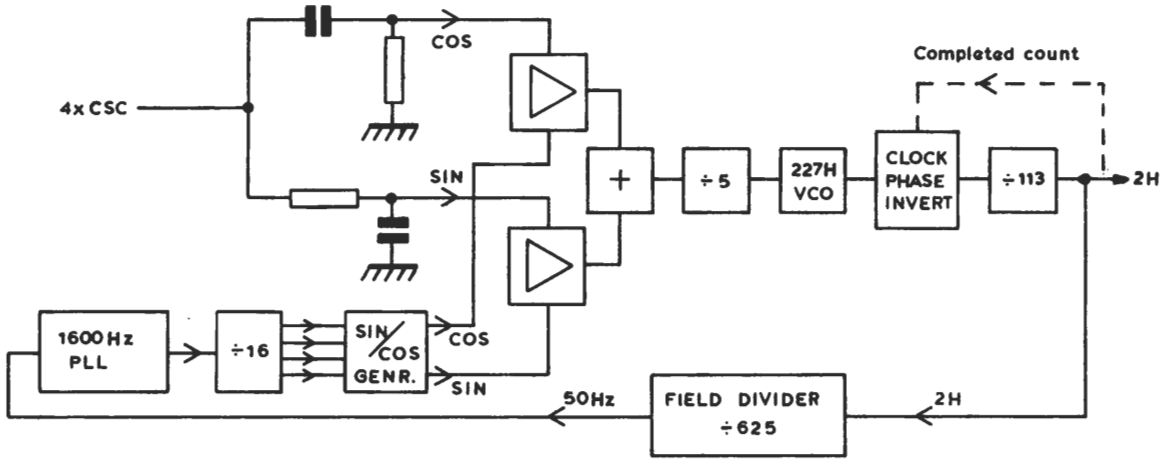

Fig. 5.4 Seltech Derivation of 2H

Notice that the 100Hz is derived from the 50Hz output of the field divider, which in turn is clocked by 2H. The offset generator output is forced to be 100Hz by virtue of the hardware "numbers" in the loop:

$$\text{OFFSET} = 1135H / (5 \times 113.5 \times 625 \times 0.5)$$
$$= 100Hz$$

The field divider output is actually used to lock an oscillator at 1600Hz. This is divided to 100Hz in a four stage counter, the outputs of which derive 100Hz sin/cos "look-alikes" via 4 bit A-D converters. When genlocking (see information sheet no. 12B "The Genlock SPG") the digital lock mode changes the horizontal timing by altering the division ratio of this counter. In the AFC genlock mode the horizontal timing is locked via the 227H PLL.

5.3.1 Subcarrier Derivation

This might seem so simple as to not require consideration however it's not quite a simple divide by 4. The reason is again genlock, where it will almost certainly be necessary to adjust the phase of the output subcarrier relative to the genlock reference. The method used is shown in figure 5.5.

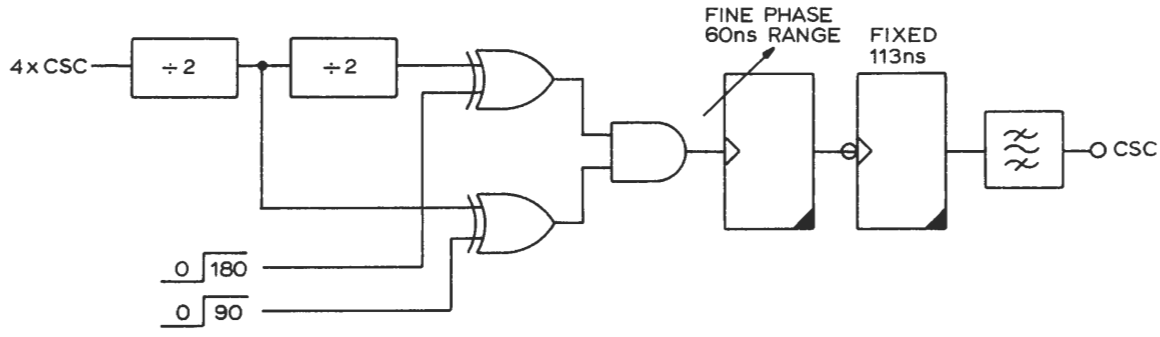

Fig. 5.5 Subcarrier Phase Adjustment

The divide by four counter outputs are gated to produce a subcarrier rate output pulse. By selectively inverting the counter outputs the pulse can be shifted in 90^0 steps over a full 360^0 range. A variable monostable of 60ns range (not 0 - 60ns, why not?) provides fine phasing adjustment.

The output of this monostable is therefore an edge which can be continuously varied over a full 360^0 range. By using this edge to trigger a fixed, 113ns, duration monostable a subcarrier square-wave "look-alike" is formed. It is a relatively simple matter to filter this square-wave to derive the necessary sine-wave output.

5.4 Oscillator Stability

One final point to consider is that of oscillator stability. The stability specified for the transmitted signal is that the subcarrier should be maintained to within 1Hz. This could be expressed as a maximum drift of 1 part in 4,433,618.75 parts, or approximately 1 in 5 million. Drift is :

1 in 5×10^6 or

2 in 10^7

which is the more usual way of expressing it.

In practice the broadcaster will maintain a much higher level of stability, apart from any other considerations there is a big advantage to video recording in keeping the subcarrier frequency constant over a relatively long period. Oscillator stabilities of better than 1 in 10^8 are relatively common, many BBC master oscillators achieve short term (over a few hours) figures of 2 in 10^{10}.

2 in 10^{10} is a drift, relative to a "perfect" oscillator, of 200ps a second. Remembering that one cycle of subcarrier is approximately 200ns this is equivalent to a drift of 1/1000th of a cycle, or 0.3^0 per second. In practical terms this means once round the vectorscope in 20 minutes. Television Centre and many NPC recording and network operations generally use a rubidium vapour sourcehaving an absolute stability of 5 in 10^{11}. This is a drift of 50ps/s, or around the vectorscope in eighty minutes.

5.4.1 Adjusting the Oscillator

Although the oscillator may have excellent short term stability its performance over weeks or months may not be as good. The figure for the 2 in 10^{10} oscillator is only 2 in 10^{8} per month. Fortunately an easy method of keeping it up to scratch exists. All that is necessary is to display network video, preferably during non outside broadcast conditions, on a vectorscope locked to local subcarrier. Tweak the local oscillator for minimum rotation (0.3^{0} per second) and the job's done.

6. COMMON SPG TECHNIQUES

This section extends the basic principles embodied in the general block diagram of figure 4.1 to examine in more detail some aspects of the s.p.g. operation. Of particular interest are the edge timing generator and field divider.

6.1 Programmable Counters

The programmable, or presettable, counter is a common building block in s.p.g.s, and enables counters having non "power of two" division to be produced easily. Figure 6.1 shows such a counter, which typically has four stages.

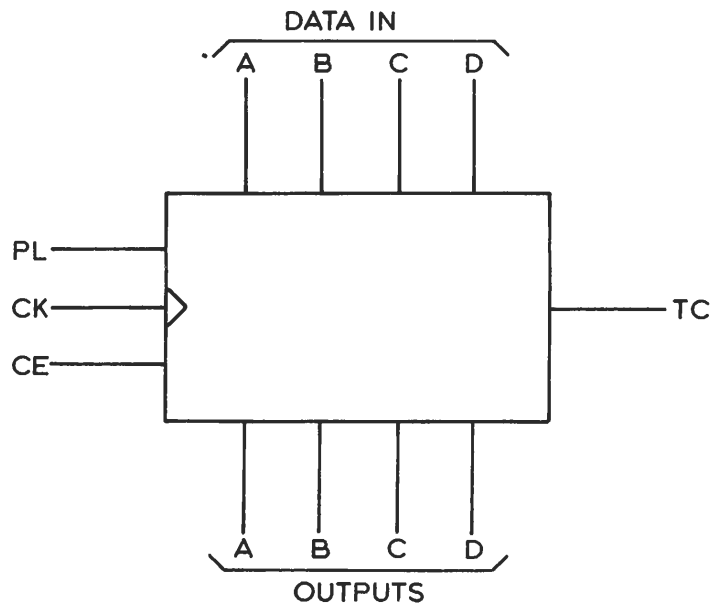

Fig. 6.1 4 Stage Programmable Counter

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In addition to the usual clock and reset inputs and counter outputs a number of other connections are provided. These are the Count Enable (CE) and Parallel Load (PL) inputs and Terminal Count (TC) output.

CE must be high and PL low for normal counting to proceed. When the maximum count value (all outputs high) is reached TC goes high. This output can be connected to the CE input of a following stage, to enable a multi-stage synchronous counter to be constructed. If PL is taken high a different state of affairs exists. Normal counting is suspended and the next clock pulse sets the counter outputs to the number programmed on the four preset count, or "jam" inputs. Figure 6.2 shows a typical 8 stage presettable counter constructed in this way.

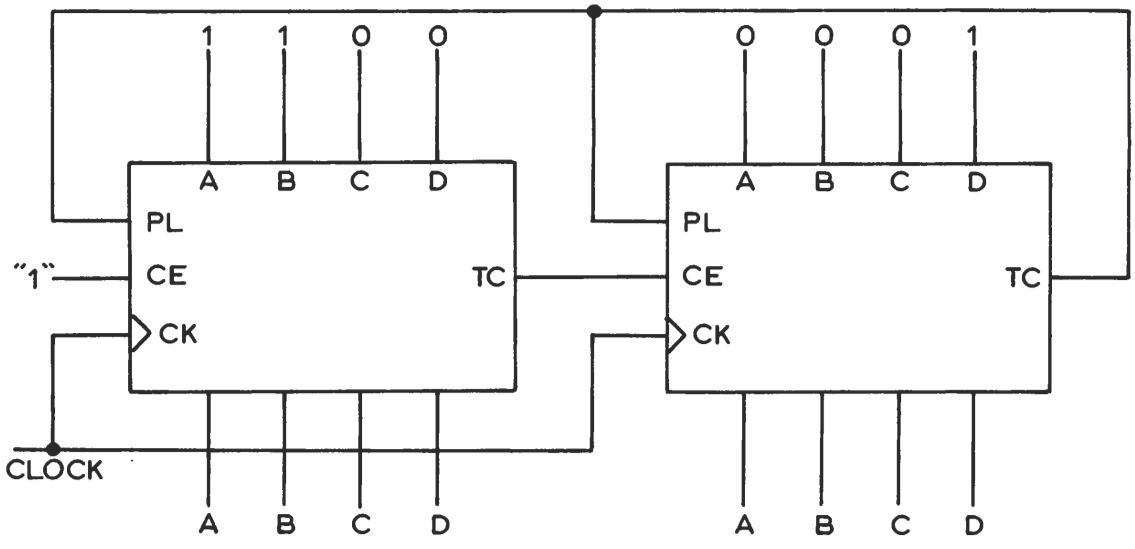

Fig. 6.2 8 Stage Presettable Counter

The TC output from the second counter is gated internally with its CE input so that it only goes high when all 8 stages are high. TC is used to enable the parallel load. Now the next clock pulse, instead of advancing the counter from maximum to zero count, loads in the preset value, in this case 131. The counter thus counts from 131 to maximum count, 255, and so on. Consequently its overall division ratio is 125, a figure that could well find application in an s.p.g.

6.2 Edge Timing Generators

Most current s.p.g.s use the same method of edge timing generation and make use of the counter which divides down the master oscillator to 2H. The division cycle of this counter therefore repeats at 2H rate, and the counter Q outputs can be gated to derive the necessary edges during each 32μs period, as described in the next section.

6.3 Counter Method of Edge Timing Generation

Consider the simple, 3 stage counter, in figure 6.3 below.

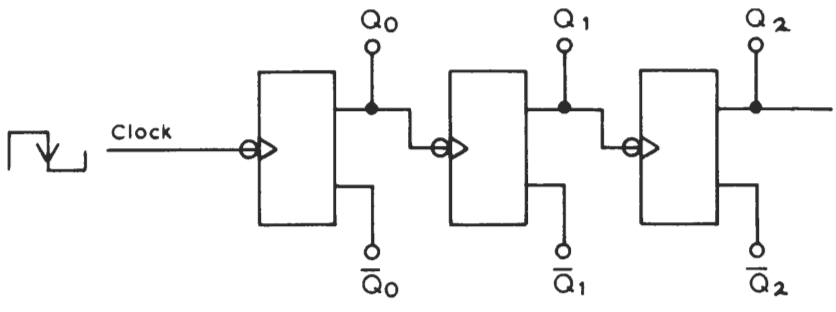

Fig. 6.3 Simple Counter divided by 8

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The up-counter Q and $\overline{Q}$ outputs from each stage, and the clock waveforms, are taken to gating, which can select a particular part of the count cycle.

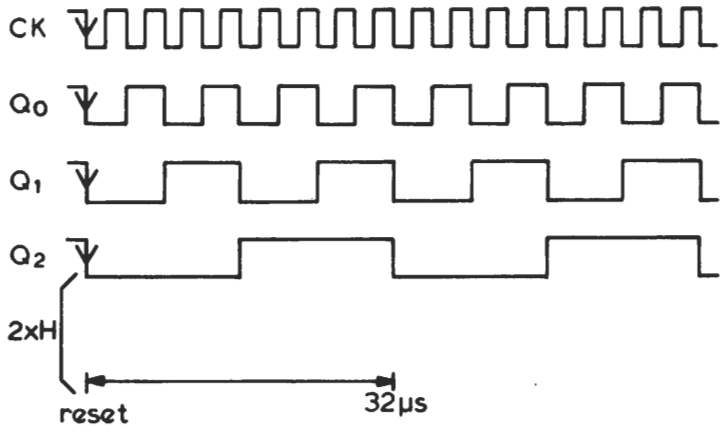

Fig. 6.4. Counter o/ps from divide by 8-up-counter.

The Q2 output must be 2 x H frequency, therefore, the input clock frequency needed is 250KHz, i.e. 4µs period. As an example, let us derive the gating required to produce edge timing pulses to suit the following output waveform.

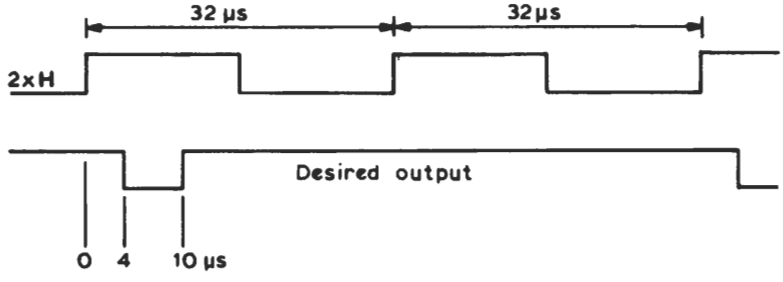

Fig. 6.5. Desired Simple s.p.g. Output Waveform.

This requires a set edge trigger for the output SR at 4µs after a rising edge of 2H, and a reset edge trigger at 10µs after the rising edge of 2H.

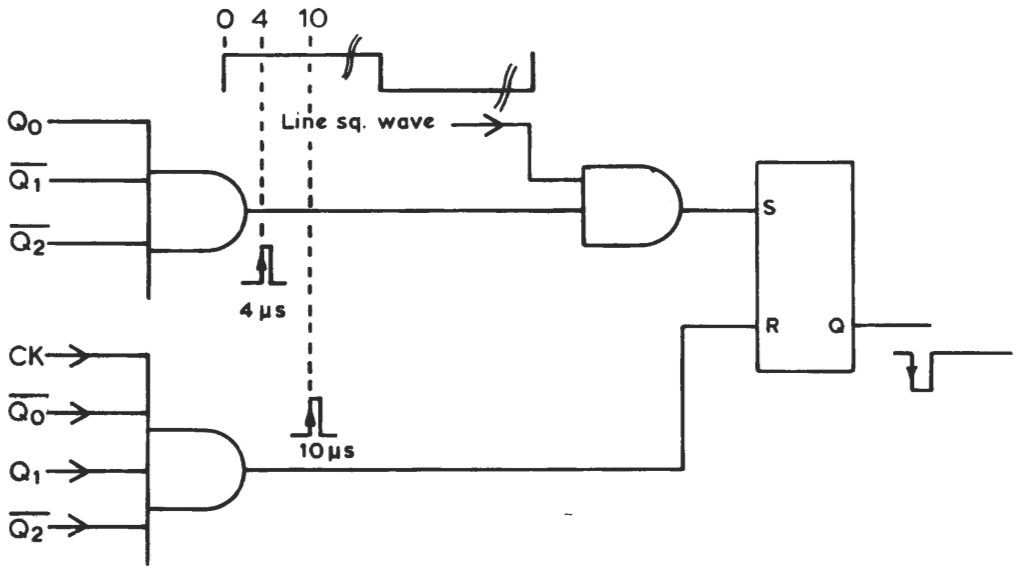

Fig. 6.6. Gating for the Required Edge Trigger.

An extra divide-by-2 must be used to produce a line-rate inhibit waveform (for the set input), from the 2H output at Q2.

The minimum separation between edge timing pulses, using a symmetrical clock at 250 KHz, is 2µs. For a practical s.p.g., clock frequencies of 1-4 MHz are used with 6 to 8 stage counters giving minimum edge separation of 500 - 125ns.

6.4 Other Edge Timing Techniques

Although nowadays the counter technique is almost universal other methods may be encountered, particularly in older generators. All other methods are based on the concept of a delay line.

The reference 2H signal is fed to a tapped delay line. The total delay available must cover the range of edge timings required, typically 15-20µs. The individual edge timings (0µs, 4.7µs, etc.) are derived directly from the delay taps.

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Analogue delays, whilst being reliable and accurate, are both bulky and expensive. Consequently this method is no longer used. Alternative approaches will be found however, one of which uses a shorter delay line with its output fed back to the input in a re-circulation technique. A parallel output shift register may also be used as a digital equivalent to the analogue delay line.

6.5 The Field Divider

The division from 2H to 50 Hz to produce field rate inhibit waveforms requires division by 625, which is not a power of 2. This is typically achieved by means of a presettable counter as described in section 6.1.

6.6. Field Divider Outputs

For mixed syncs, the finish pulses must be changed to give 'equalising', then 'broad' pulses, then equalising pulses once per field. In this period, the start pulses must occur at twice-H rate, to give the 15 field-group pulses in 7.5 lines. (See Information Sheet 44E). Once per field, the field divider produces a 7.5 line long waveform to allow the twice-line start pulses. The inverse is used to block (inhibit) line sync finish during the 7.5 lines. What are the other two waveforms in figure 6.7 used for?

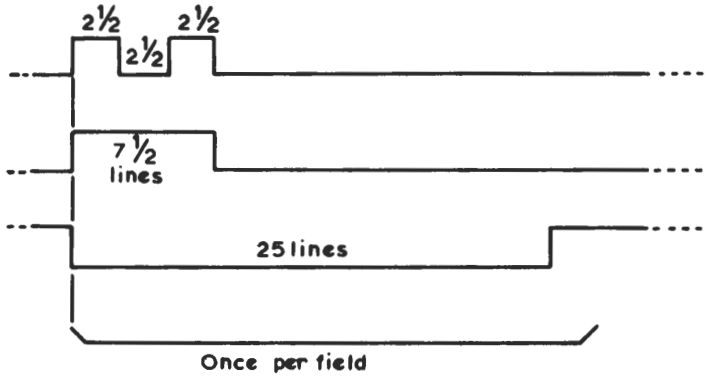

Fig. 6.7. Typical Field Rate inhibit waveforms

A combination of line and field inhibits may thus be needed to generate many of the s.p.g. outputs, as illustrated by the mixed syncs output.

6.7 Generation of Mixed Syncs

Mixed syncs is basically a line-rate signal except for a period of seven and a half lines during the field sync interval. In the field sync interval, output pulses are generated every 32μs for this period of seven and a half lines. The first five intervals contain equalising pulses 2.3μs long; the next five contain broad pulses, 27.3μs long; and the last five contain equalising pulses again, all with leading edges at t = 0 and t = +32μs.

Figure 6.8 illustrates the generation of mixed sync pulses.

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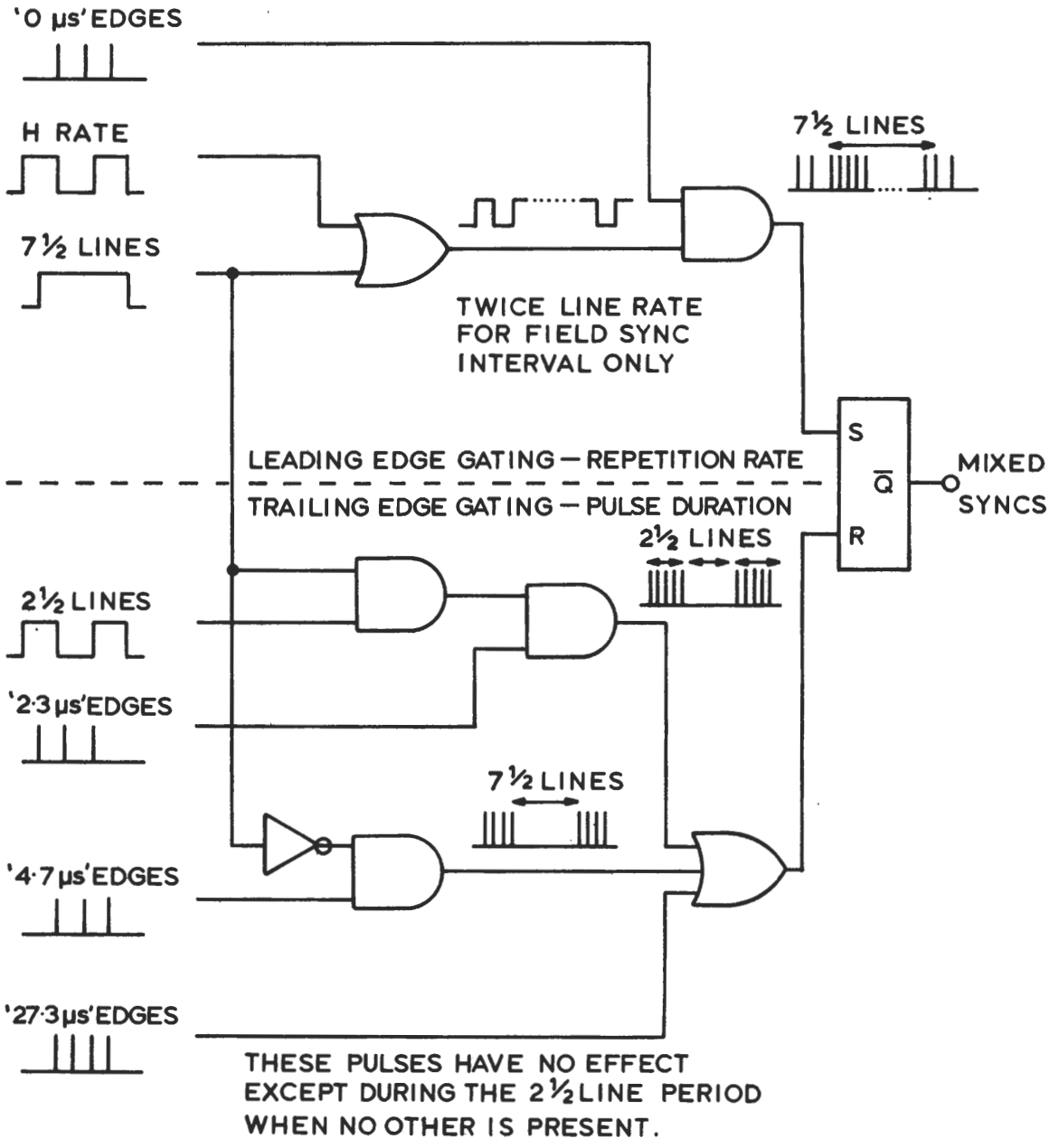

Fig. 6.8 Mixed Sync Generation, showing line and field rate Inhibit

7. PAL V-AXIS SWITCH AND BURST GATE

With the exception of Burst Gate the other synchronising waveforms are obtained in a similar but simpler fashion. (Fewer components). Burst gate generation is fundamentally straightforward but is complicated by the Bruch Blanking Sequence. The colour burst is blanked for 9 lines each field, however the blanking is related to the polarity of the VAS waveform. First and last bursts always correspond to positive VAS. Burst blanking is achieved by not generating burst gate pulses. Inhibit waveforms are therefore needed to do this, waveforms which must relate to the polarity of VAS.

7.1 V-Axis Switch (V.A.S.)

To alternate the polarity of the V signal in the coder on a line-by-line basis, the V.A.S. waveform is a square-wave at half-line frequency (7.8kHz.) The transitions should occur at the leading edge of line sync. Leading edge triggers from the edge timing generator are inhibited to line frequency and fed to the clock input of a ÷2 circuit. The circuit and waveforms are shown in fig. 7.1.

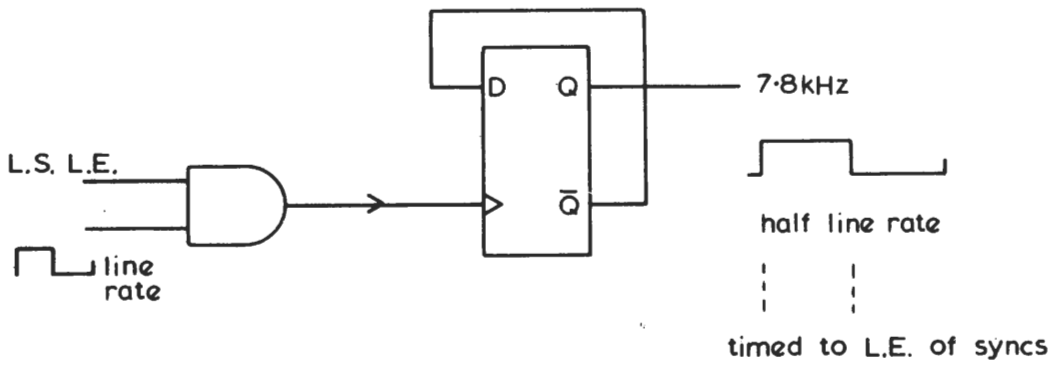

Fig. 7.1 V.A.S Generation

SYNC PULSE GENERATION

7.2 Burst Blanking

A look at the field interval of fields 1-4 (information sheet 44E) shows that burst blanking may be started as much as one and a half lines before the start of the normal mixed blanking field component. (The last burst must occur on a complete line, not a half-line). A further waveform is generated from the field divider, to start one and a half lines before the seven and a half and twenty five line components, and last for nine lines. This is then combined with V.A.S. to set a bistable to produce a Bruch Blanking pulse of 9-lines timed correctly on each field. Figure 7.2 illustrates this.

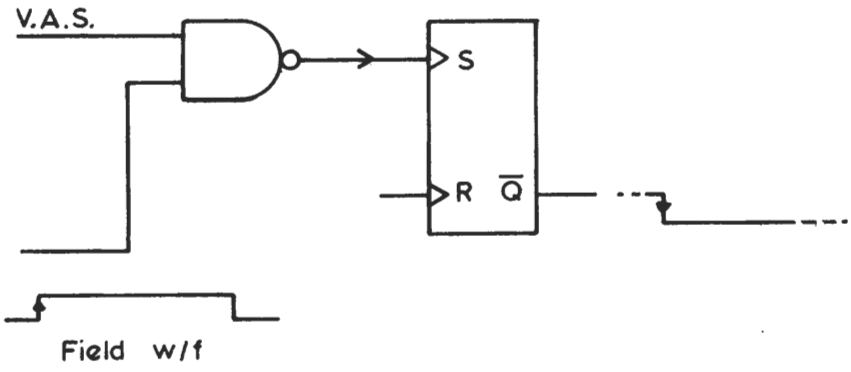

Fig. 7.2 Generation of Burst Blanking Start

The use of a NAND gate means that its output is held high, until the field waveform goes high, gating through the VAS, but inverting it. The bistable is positive-edge triggered. At the end of the first line with VAS high and field w/f active, a +ve edge will set the bistable, the output of which will be used to inhibit B.G.L.E. pulses. When the 9-line field w/f goes low, the next line of +ve VAS polarity can have a burst, so the blanking bistable must be reset.

This is achieved by gating the inverse of VAS with the inverse of the field w/f using a NAND to feed the +ve edge-triggered reset, as shown in figure 7.3.

To recap, a 9-line field waveform is produced by the field divider, having a fixed relationship to the state of field pulses. This is re timed by a VAS so that a 9-line waveform is produced, such that the line before it and the line after it have positive VAS.

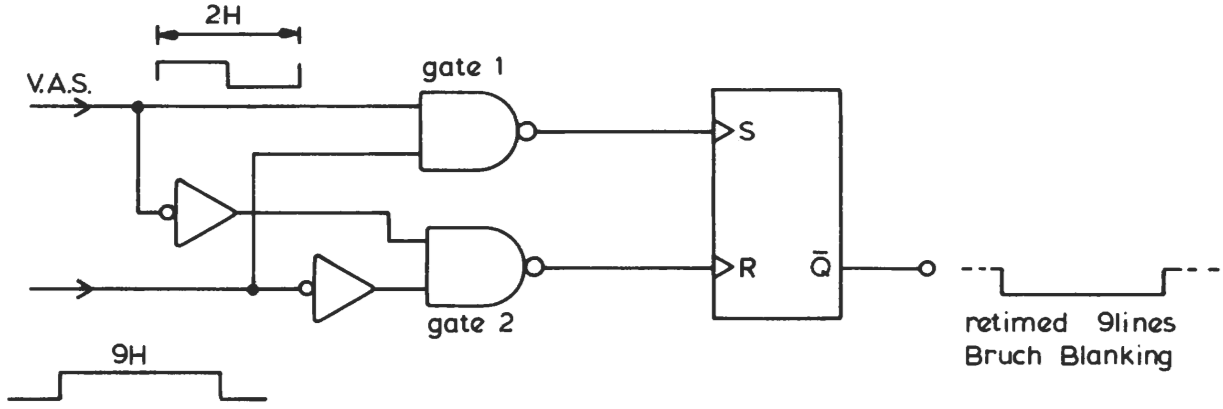

Fig. 7.3 Complete 9-line Inhibit Generator

Figures 7.4 and 7.5 below show the sequence of waveforms for the start of fields 1 and 3 respectively.

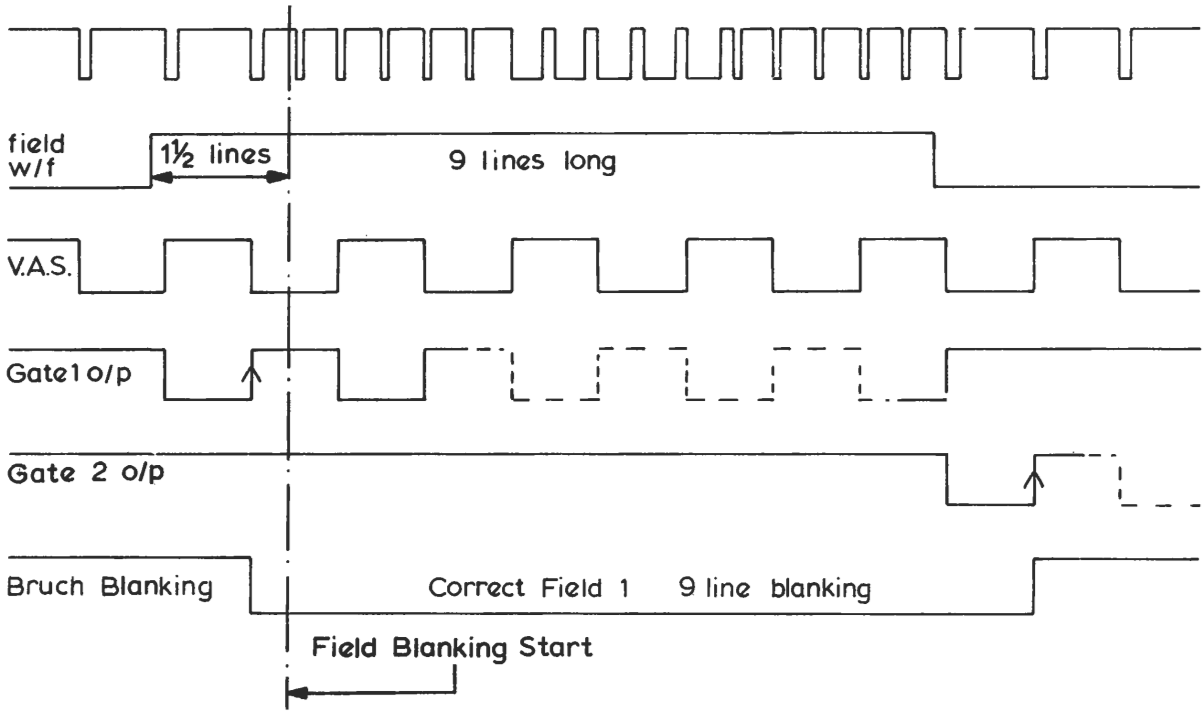

Fig. 7.4 Derivation of Bruch Blanking, Field 1

SYNC PULSE GENERATION

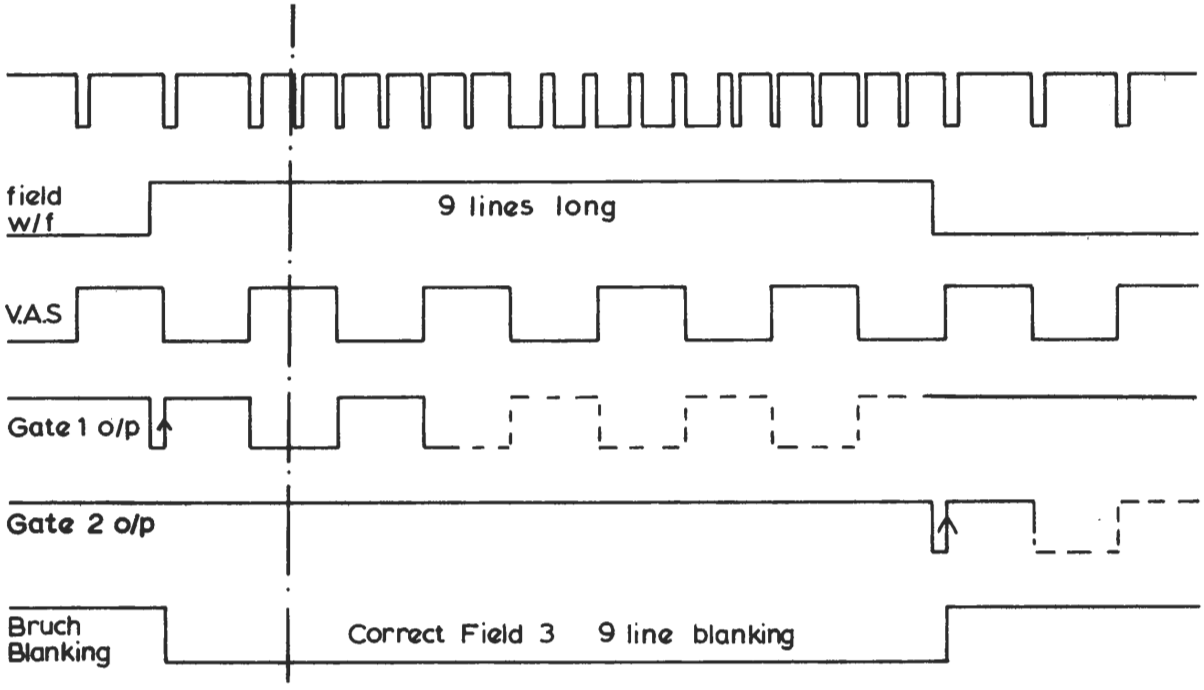

Fig. 7.5 Derivation of Bruch Blanking, Field 3

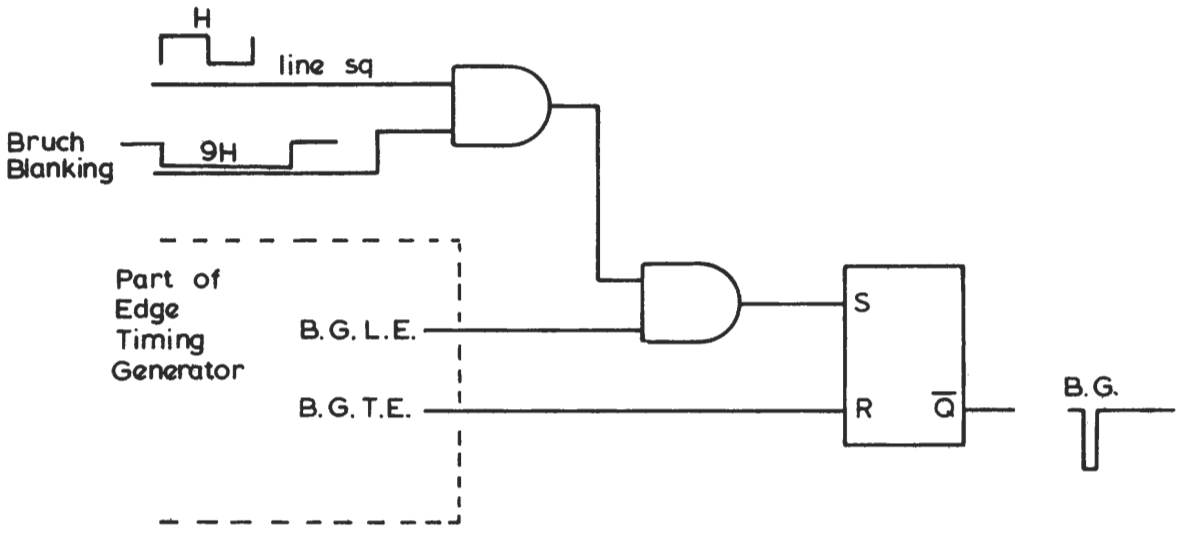

Fig. 7.6 Burst Gate Waveform

The Bruch Blanking is combined with the line frequency square wave to give the combined inhibit for burst gate leading edge pulses, as in fig. 7.6.

It is worth noting that the process is reversible - VAS can be obtained from burst gate and mixed syncs. Most current equipment requiring VAS (coders etc) generally derives it in this way, thus saving on distribution.

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9.5.86
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