SYNC PULSE GENERATION 1.

INTRODUCTION

This information sheet describes the generation of pulse waveforms required to produce the 625-line (System I) television signal. These pulse waveforms are themselves generated by a 'Television Waveform Generator' (which is its official BBC title), but it is called a 'sync pulse generator', or S.P.G., by most broadcast engineers and throughout this information sheet.

Broadcast sync pulse generators use medium- and small-scale integrated circuits, although a single chip s.p.g. is available and, at the time of writing, is used for C.C.T.V. and Domestic Video.

This information sheet therefore provides an outline of the common techniques used in current broadcast s.p.g.'s.

1. WHAT ARE PULSE WAVEFORMS USED FOR?

There are six pulse waveforms, plus colour sub-carrier, used to originate the broadcast television signal. (See information Sheet 44E).

In the camera, the scan generators cause motion of the electron beam horizontally (Line scan) and vertically (Field scan) over the light image. Flyback, to start a new scan, is initiated by the drive waveforms, line drive and field drive.

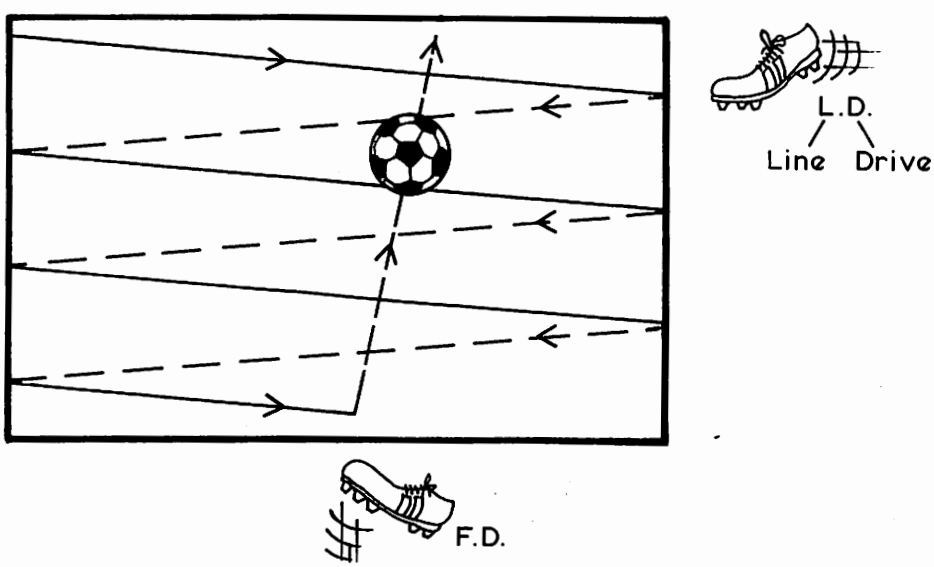


Figure 1.1. Scan Drive Waveforms

SYNC PULSE GENERATION

The drive waveforms can be supplied from the sync pulse generator, although most recent cameras have circuitry to derive these within the camera from the mixed syncs waveform.

The video waveform from the head amp. has suppression periods, where the beam was turned off (beam blanking) during flyback. In the camera, flyback can be achieved more quickly than the flyback in a monitor or receiver, where a much wider angle of deflecton is used.

MIXED BLANKING is therefore used to widen line and field blanking intervals to give sufficient time for the monitor to flyback; and to give the same blanking widths on all sources (also called "system blanking").

MIXED SYNCS is added to the final output signal to provide line and field synchronising signals to the display scans.

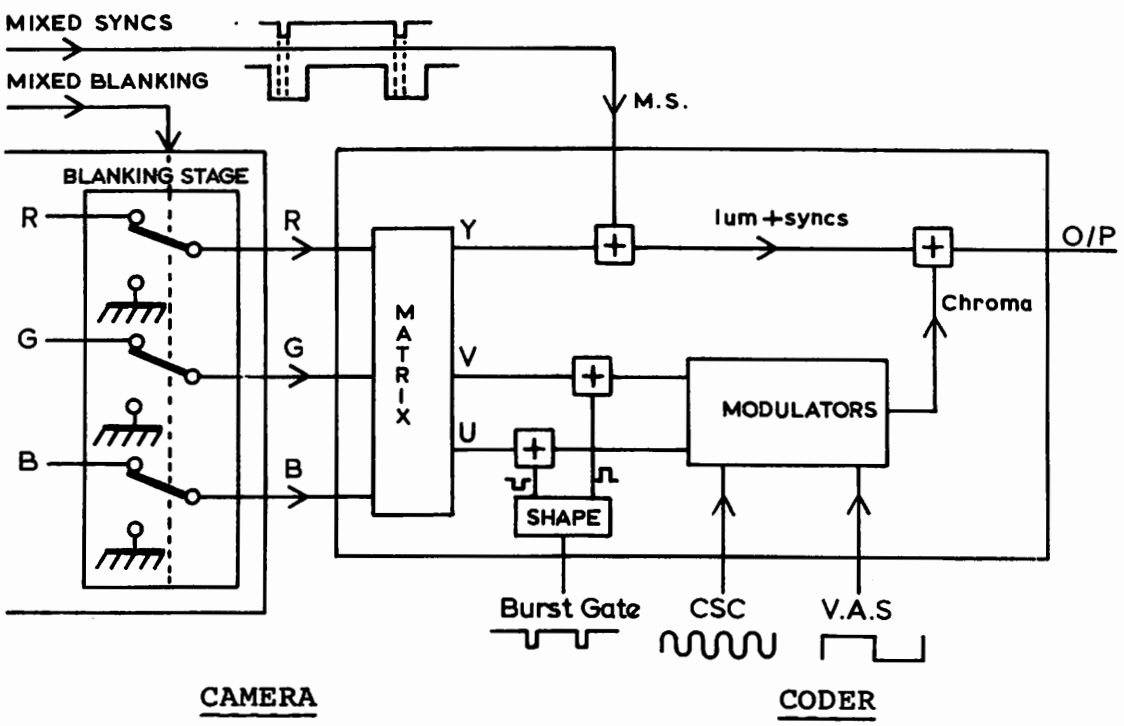


Fig. 1.2. Use of Synchronising Waveforms.

For PAL colour-coded signals, the polarity of the V-axis colour subcarrier is alternated by the V-Axis Switch waveform at half-line rate (7.8 KHz).

BURST GATE is used to introduce the colour burst into the correct part of the back porch of the video signal.

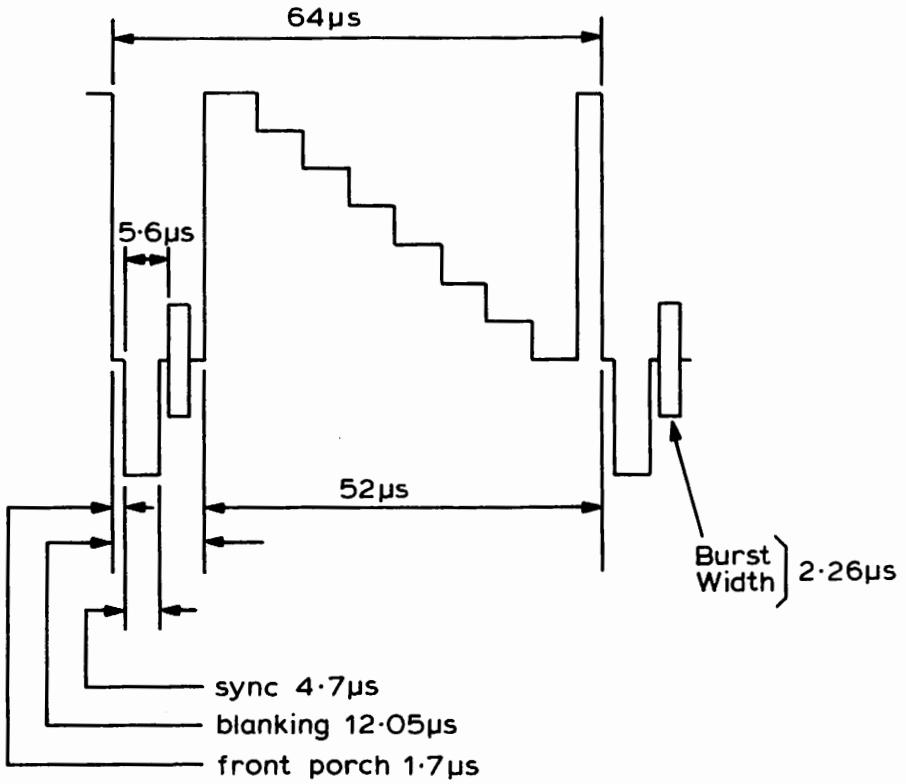


Fig. 1.3. Line Rate Video Waveforms.

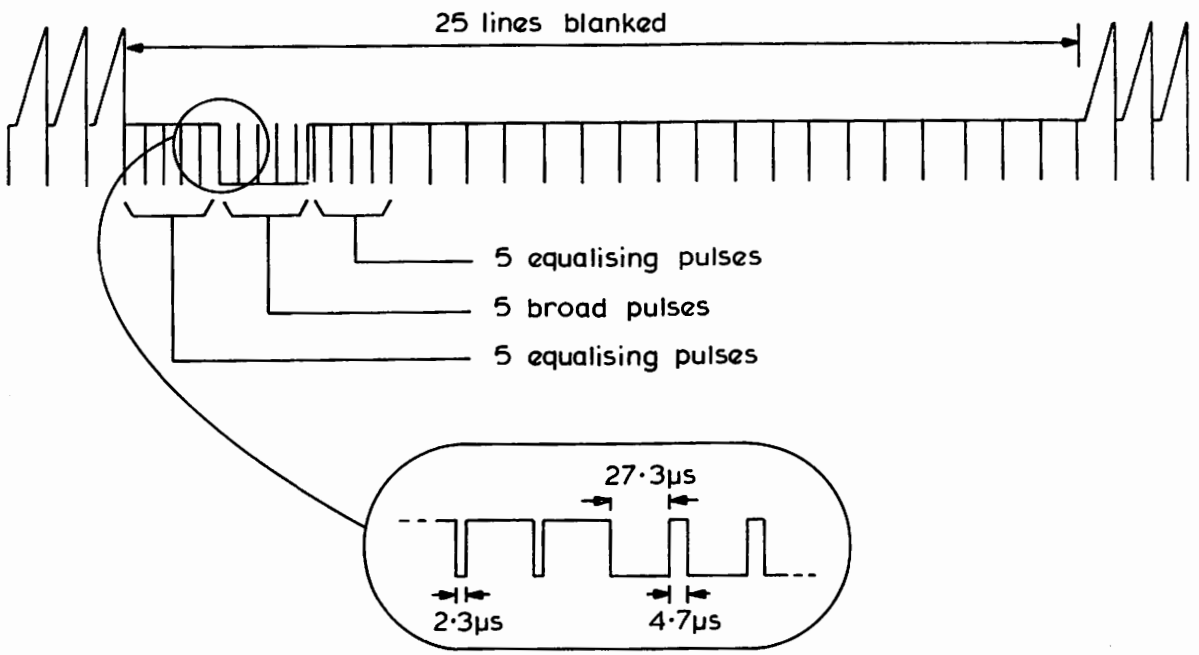


Figure 1.4. Field Rate Video Waveforms

SYNC PULSE GENERATION

These waveforms have timings corresponding to the International Specification of P.A.L. System I.

2 PULSE GENERATION PRINCIPLES - THE BISTABLE METHOD.

The pulse outputs of an s.p.g. are binary signals, having only two voltage levels for each signal. An S.R. bistable can be used to generate each required waveform, as follows:-

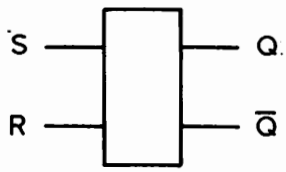


Fig. 2.1. S-R Bistable.

A pulse on the 'Set' input causes Q to assume logic '1'. Q will remain at logic '1' until a pulse is applied to the Reset i/p, when it changes to logic '0'. Using +ve logic, the waveforms are as shown in Fig. 2.2.

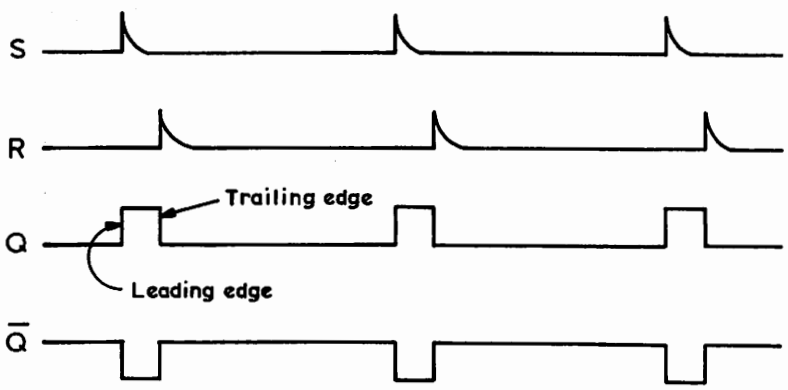


Fig. 2.2. Typical Signals for the S.R. Bistable.

The important fact from Fig. 2.2 is that the short pulses fed to S and R define transitions, or edges, in the output waveform from Q, and are therefore called 'edge timing pulses'.

Pulses fed to the 'Set" input define the leading edge timing, and pulses fed to 'Reset' define the trailing edge timing of the Q output waveform.

SYNC PULSE GENERATION

Sync pulses are conventionally distributed as low-active signals, and it is useful to note that the inverse of the Q output is always available from $\overline{Q}$.

3. EDGE TIMING PULSE GENERATION.

The highest repetition rate contained in the s.p.g. outputs occurs when equalising and broad pulses are being generated at 2H rate. (H is the horizontal scan frequency).

An Edge Timing Generator is therefore clocked at 2 x H rate, its outputs being a number of pulses, of suitable timing relative to each other, which can be used as leading and trailing edge triggers for the s.p.g. outputs.

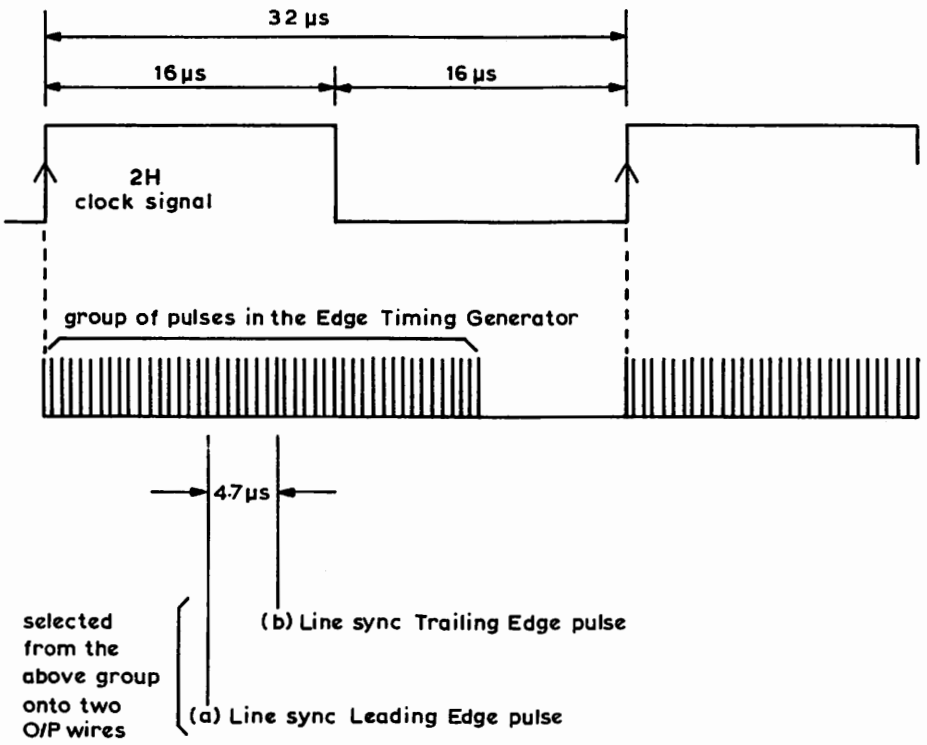


Fig. 3.1. Generation Principles for Edge Timing Pulses.

By a selection process within the Edge Timing Generator, a pulse at time (a) is routed out to be the leading edge trigger for line syncs. A pulse 4.7µs later (b) is selected and routed out as trailing edge trigger for line syncs.

SYNC PULSE GENERATION

The other outputs of the Edge Timing Generator supply start (leading edge) and finish (trailing edge) pulses for the other components of the sync waveforms.

As a simple example, take line drive, which has a start pulse 1.7μs early on line sync start, and a finish pulse 4.8μs late on line sync start. (Note that line sync leading edge is used as a reference for time measurement across a television line. It is often referred to as t = 0.)

4. INHIBIT GATING.

The Edge Timing Generator produces all start and finish pulses at 2H rate. If they are required at a lower rate, e.g. to give line (H) or field (V) rate outputs, then they are gated with an inhibit waveform to remove unwanted edge timing pulses.

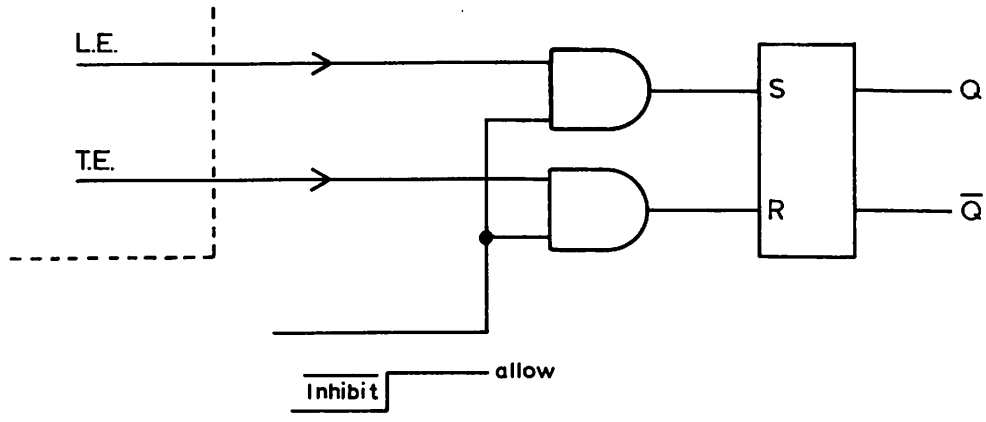


Fig. 4.1. Ideal Inhibit Gating for Line Drive.

For our example of line drive, every other set and reset trigger must have no affect; the inhibit waveform is therefore a line rate square wave.

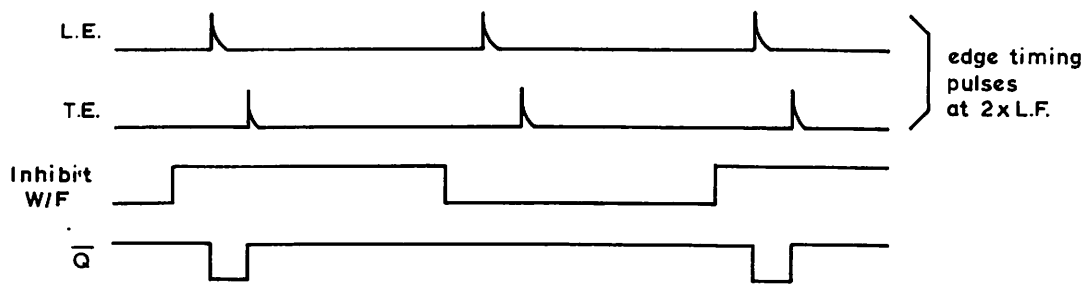


Fig. 4.2. Waveforms for L.D. Generation

Note that the timing of inhibit waveform is not critical, as long as the gates are open for one pair of pulses and closed for the next pair.

The circuit of Fig. 4.1 uses two 'And' gates, but it is possible to reduce the hardware by not inhibiting the reset input of the bistable.

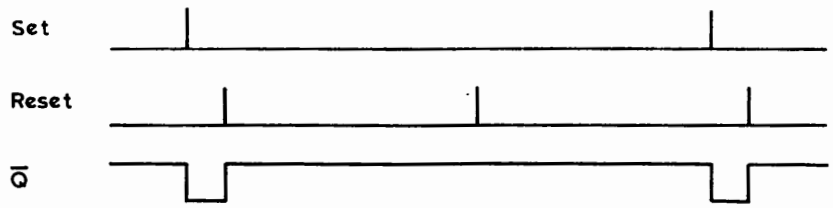


Fig. 4.3. Waveforms at the Bistable in Fig. 4.4.

The bistable ignores the second reset pulse since it is already reset. So, one gate is saved.

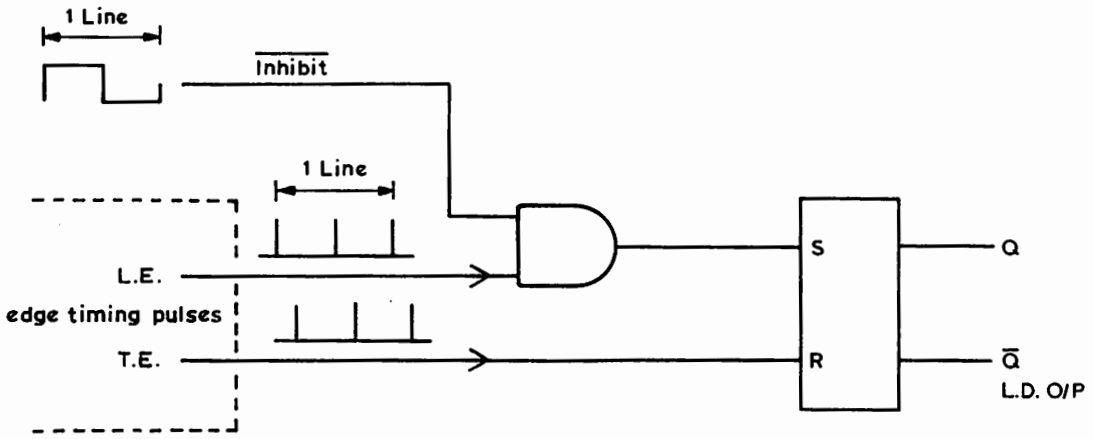


Fig. 4.4. Practical Line Drive Circuit.

For Mixed Syncs, the edge triggers used to set and reset the bistable must be changed to give different pulse widths and repetition rates during the field sync period. Field rate inhibit waveforms are produced in the Field Divider. This is clocked by the SAME 2H frequency which drives the edge timing generator, and is divided by 625 to give 50Hz inhibit waveforms.

SYNC PULSE GENERATION

5. BLOCK SCHEMATIC OF AN SPG

The separate components of the SPG form the block diagram of Figure 5.1.

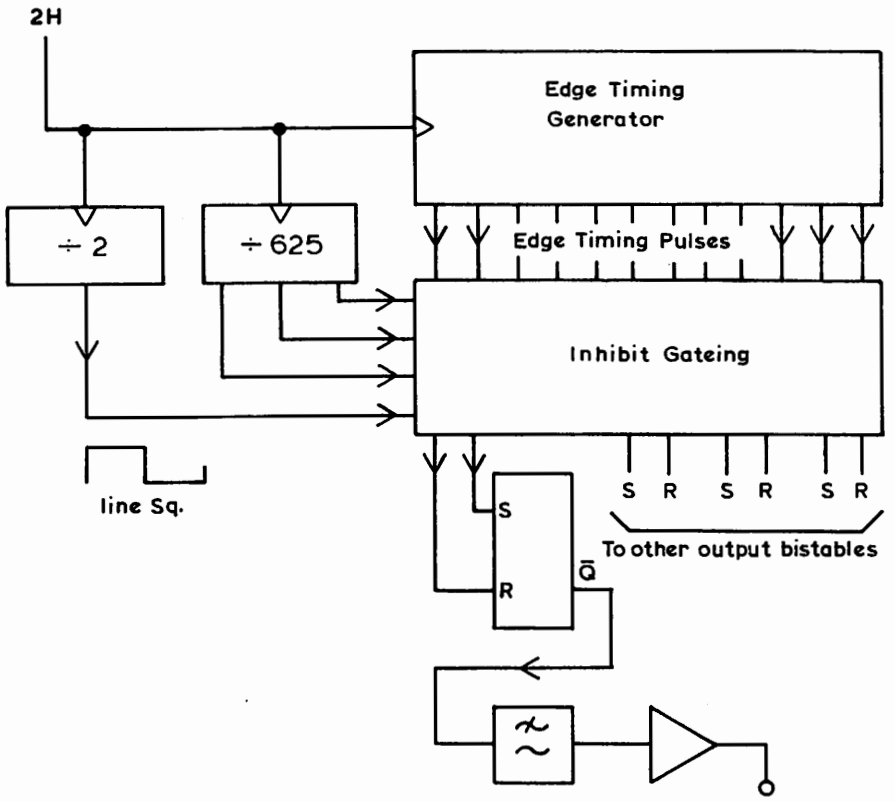


Figure 5.1. A General SPG Block Diagram

The 2 x H frequency drive may come from either an external drive source, or from a stable internal oscillator.

Most current sync pulse generators contain a high-frequency crystal oscillator, (from which PAL subcarrier frequency may also be derived,) which is divided down to generate the 2 x H frequency clock for the edge timing generator and the line and field dividers.

6. CURRENT TECHNIQUES USED IN EDGE TIMING GENERATORS.

There are two basic techniques used to produce edge timing pulses correctly time-related to each other.

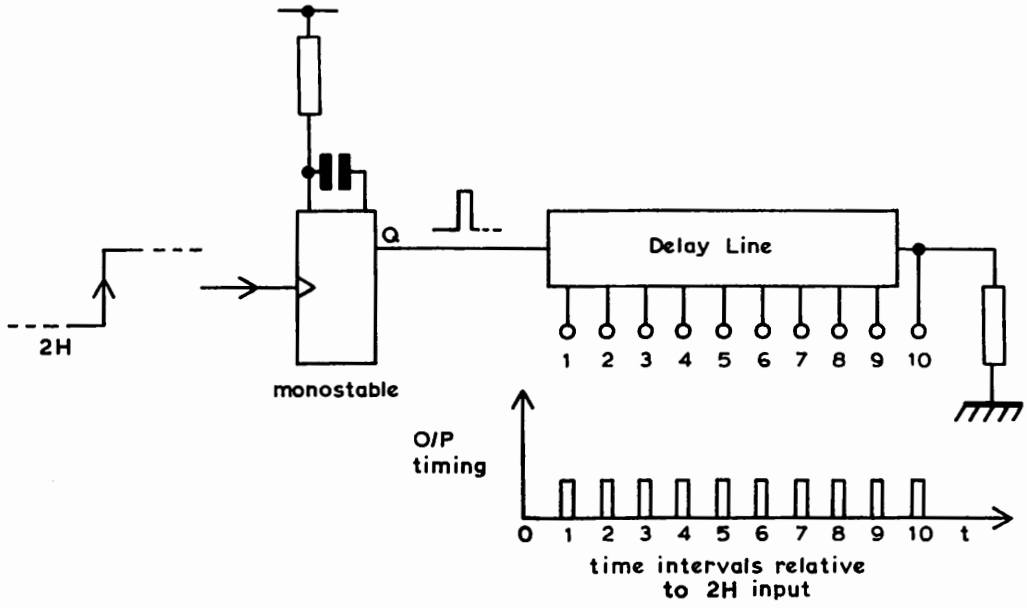
In the first technique, the 2 x H clock fires a short pulse into a delay- line. The delay line has taps at the required timing intervals.

In the second method, a divider divides down from a high frequency to 2 x H frequency. By gating, it is possible to select time intervals from the count sequence which will give the correct edge timing.

6.1. SIMPLE DELAY LINE (OBSOLETE)

One edge of the 2H generates a fixed width pulse which is injected into the delay line, producing a range of edge timing pulses from the taps.

Large delay line lengths are both expensive and bulky, and this has made this technique obsolete.



Fig, 6.1. Simple Delay Line.

6.2. BBC S.P.G.: - DELAY LINE- WITH RE-CIRCULATION.

To reduce the bulk of the delay line, only 4us of delay is used, but the pulse is re-circulated four times to give edge timing pulses over a 20us period following the twice-line clock edge.

SYNC PULSE GENERATION

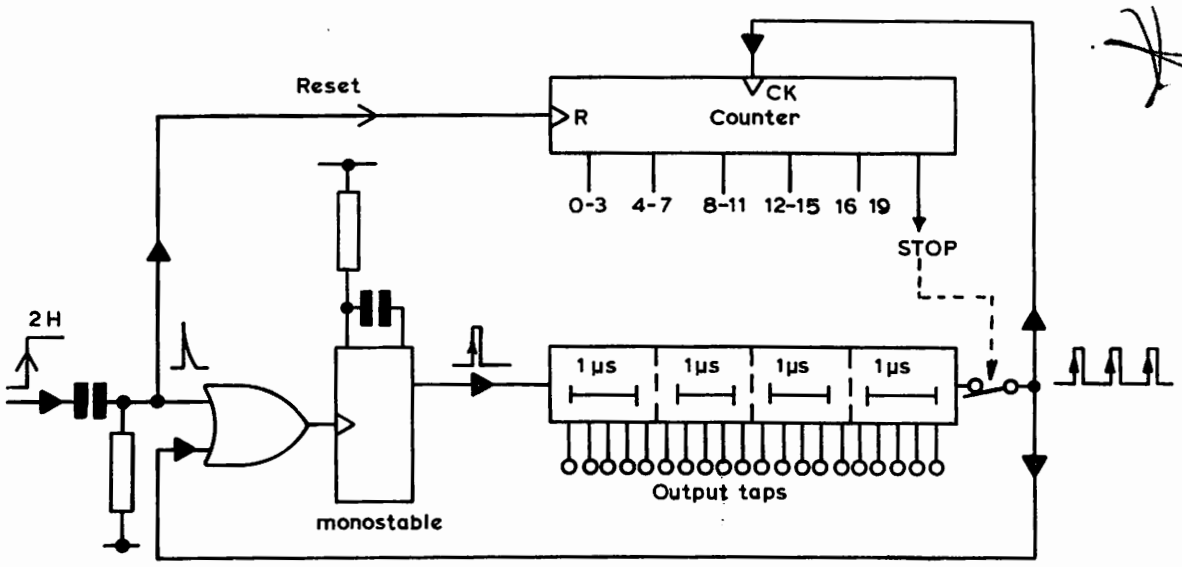


Fig. 6.2 Short Delay with Re-circulation.

A counter is clocked to keep count of how many times the re-circulation has occurred, so that the time periods 0-3us, 4-7us, 8-11, 12-15 and 16-19, may be identified.

Re-circulation is stopped after 20us and the circuit initialised for the next 2H input.

6.3. SHIFT REGISTER USED AS DELAY LINE.

In the Link 250 s.p.g., a shift register is used in place of an expensive analogue delay- line.

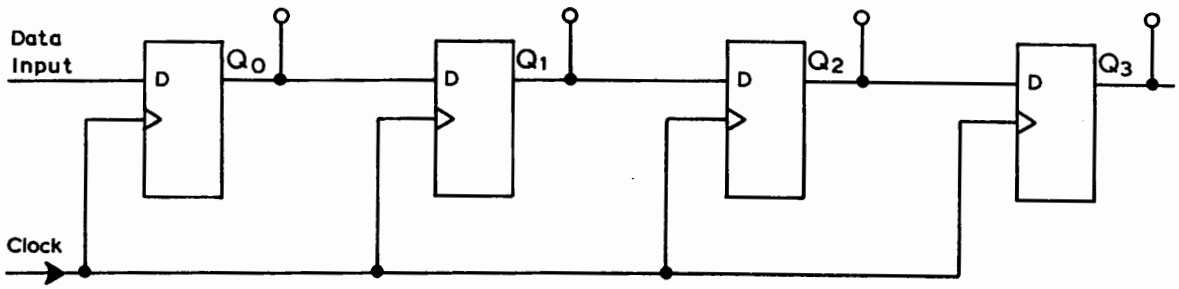


Fig. 6.3. Shift Register - Data Clocked to the Right.

SYNC PULSE GENERATION

Fig. 6.3 shows a 4-bit shift register made from D-type bistables. If all are first cleared, and then logic '1' presented on the data Input, this logic will appear at Qo after 1 clock pulse, at Q1 after 2 clock pulses, Q2 after 3 clock pulses, etc.

The Link s.p.g. divides down from high frequency to produce a 2 x H frequency signal which loads a single logic '1' as 'data in'. The high frequency is used to clock the logic '1' along a 24-bit shift register.

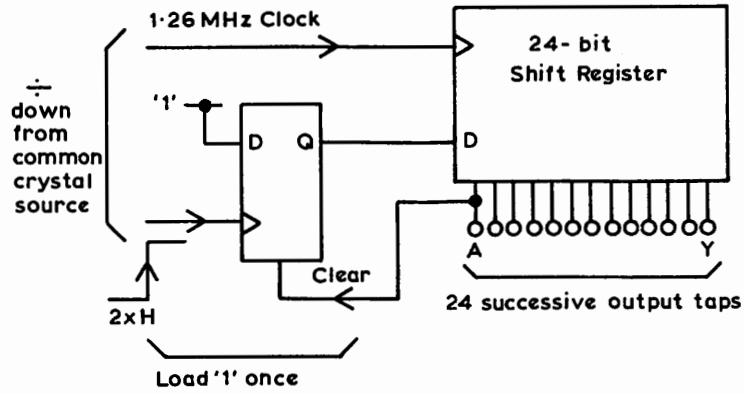


Fig. 6.4. Link 250 Edge Timing Generator.

Once per cycle of 2H the data given to the 24-bit Shift Register changes to logic 1. The first 1.26MHz clock edge then loads this 1 into the A output of the register and clears the load circuit back to '0'. Further 1.26MHz clock pulses chase the logic '1' along the outputs A to Y, i.e. a pulse of approximately 800ns appears at each output in turn.

The 8th output, H, is used as line sync start; the 14th, 0, is used as line sync finish, the 6th output, F, is used as line drive start, etc.

6.4. COUNTER METHOD OF EDGE TIMING, e.g. Seltech 110.

A high-frequency oscillator is used to clock a counter whose final output is the 2 x H frequency.

To show the principle, an example using a 3-stage up-counter is given below.

SYNC PULSE GENERATION

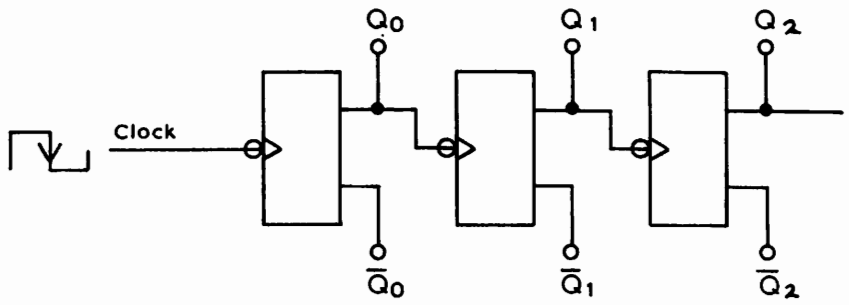


Fig. 6.5. Simple Counter divided by 8.

The up-counter Q and Q outputs from each stage, and the clock waveforms, are taken to gating, which can select a particular part of the count cycle.

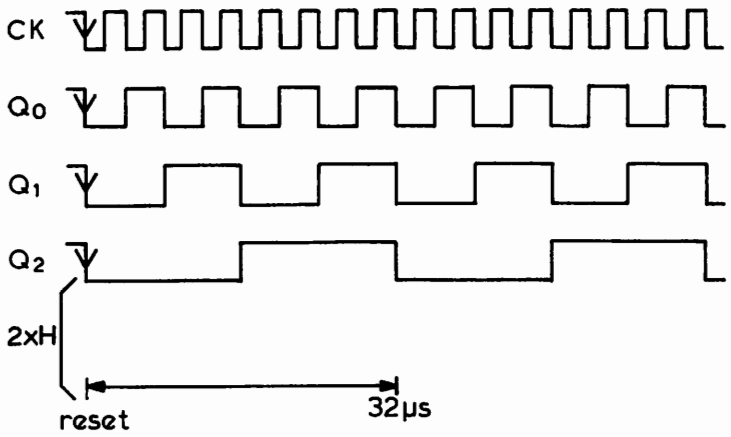


Fig. 6.6. Counter o/ps from divide by 8-up-counter.

The Q2 output must be 2 x H frequency, therefore, the input clock frequency needed is 250KHz, i.e. 4us period.
As an example, let us derive the gating required to produce edge timing pulses to suit the following output waveform.

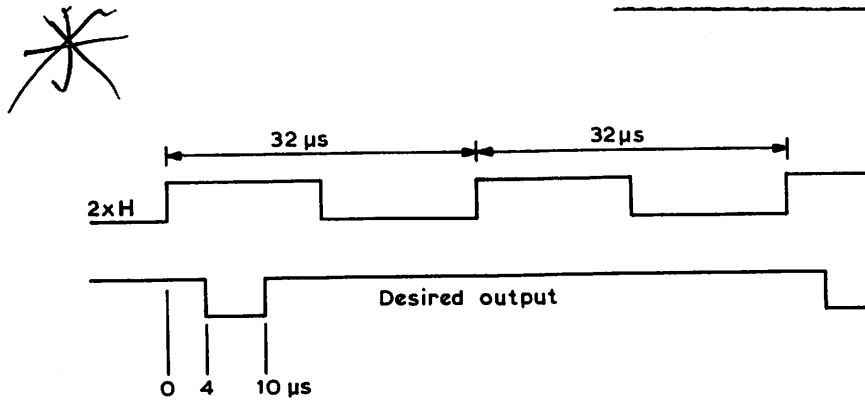


Fig. 6.7. Desired Simple s.p.g. Output Waveform.

This requires a set edge trigger for the output SR at 4us after a rising edge of 2LF, and a reset edge trigger at 10µs after the rising edge of 2LF.

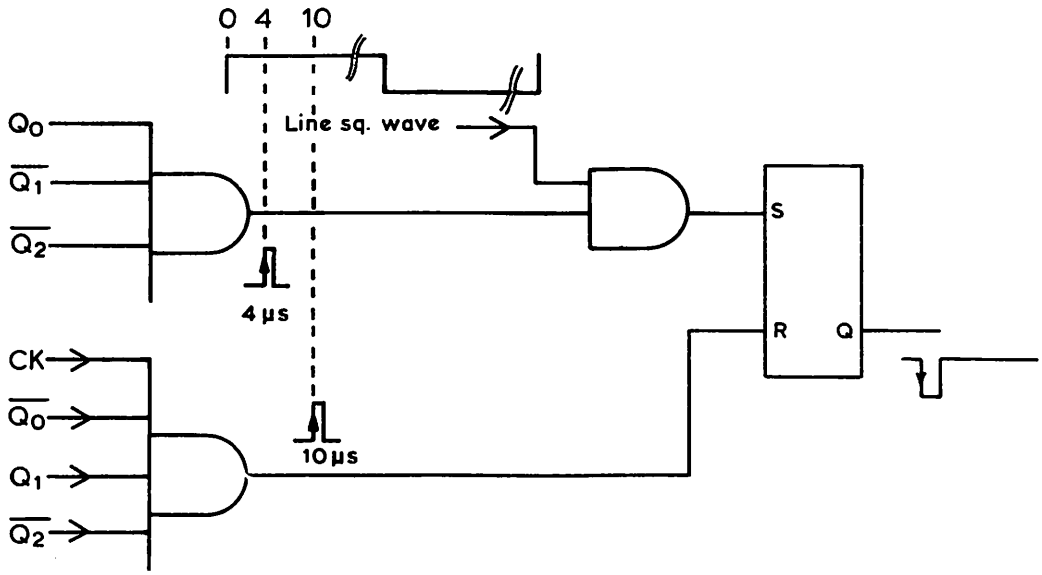


Fig. 6.8. Gating for the Required Edge Trigger.

An extra divide-by-2 must be used to produce a line-rate inhibit waveform (for the set input), from the 2H output at Q2.

The minimum separation between edge timing pulses, using a symmetrical clock at 250 KHz, is 2us.

For a practical s.p.g., clock frequencies of 1-4 MHz are used with 6 to 8 stage counters giving minimum edge separation of 500 - 125ns.

The Seltech 110 uses a 3.55 MHz clock giving a clock period of 280ns, i.e. 140ns and its multiples between edge timing pulses.

SYNC PULSE GENERATION

7. THE FIELD DIVIDER.

The division from 2H to 50 Hz to produce field rate inhibit waveforms requires division by 625, which is not a power of 2. There are two common ways of modifying the division ratio of a binary divider.

7.1 GATED RESET

We have seen earlier how to gate out a particular count from a counter division cycle. If the gated 'count 5' is used to clear all stages of a divide by 8 counter, the count cycle will begin again after only 5 clock pulses.

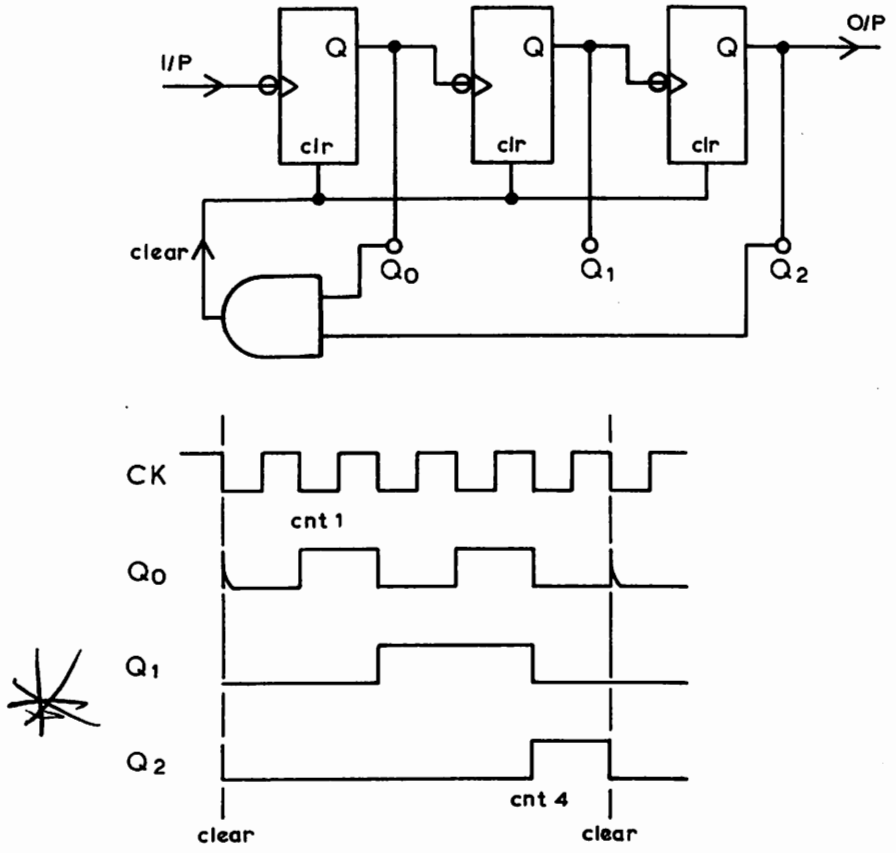


Fig. 7.1. Divide-by-5 counter using gating:- Circuit and Waveforms

Each clock pulse causes a count-up cycle until both Q2 and Qo become active, on the fifth clock pulse. The And gate detects this condition and clears down the bistables. When these have been cleared, the And gate output goes low, enabling a further count cycle.

A divide-by-625 counter can be made from four divide-by-5 circuits in series.

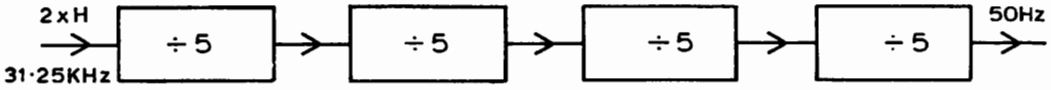


Fig. 7.2.

7.2 PRESETTABLE COUNTER.

The divide-by-625 could be done by a ten stage counter, whose binary count is normally 1024, and reset, as above, when gates detect the condition 625 on its output.

This would involve a lot of gates to detect binary 625. Some counters, however, have the capacity of loading a number into the counter, and the counter can then run, not from zero, but from the loaded count up to the maximum value. Each time the maximum count is reached (all '1's) internal gating produces a signal called terminal count, TC, which can be used to re-load the starting number at the next clock pulse.

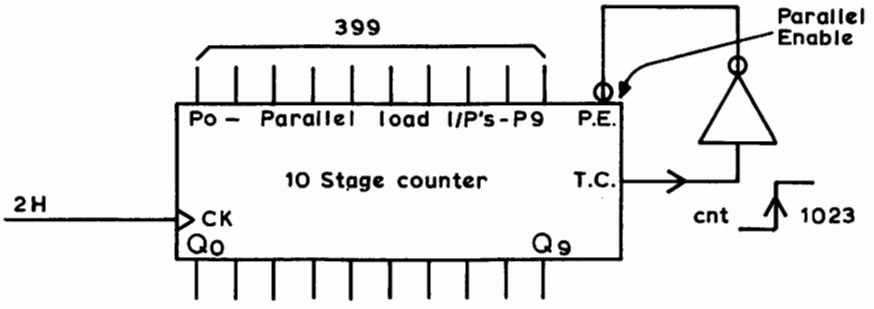


Fig. 7.3. Presettable Counter as ÷625 Field Divider.

The Q outputs are taken to gating which decodes the correct duration field rate inhibit waveforms.

SYNC PULSE GENERATION

7.3. FIELD DIVIDER OUTPUTS.

For mixed syncs, the finish pulses must be changed to give 'equalising', then 'broad' pulses, then equalising pulses once per field. In this period, the start pulses must occur at twice-H rate, to give the 15 field-group pulses in 7.5 lines. (See Information Sheet 44E). Once per field, the field divider produces a 7.5 line long waveform to allow the twice-line start pulses. The inverse is used to block (inhibit) line sync finish during the 7.5 lines. What are the other two waveforms in fig. 7.4 used for?

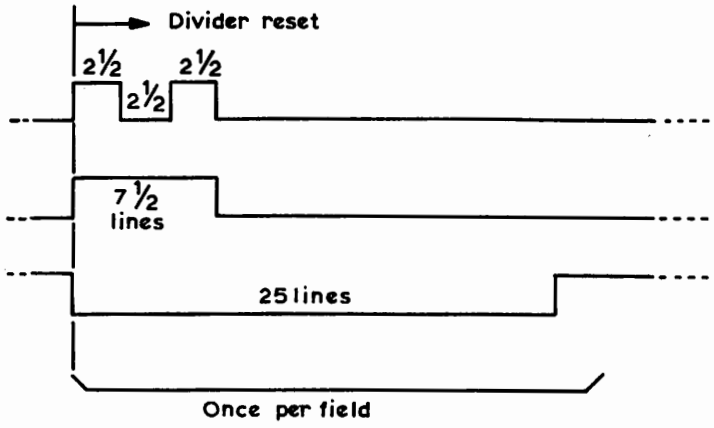


Fig. 7.4. Typical Field Rate inhibit waveforms

A combination of line and field inhibits may thus be needed to generate many of the s.p.g. outputs.

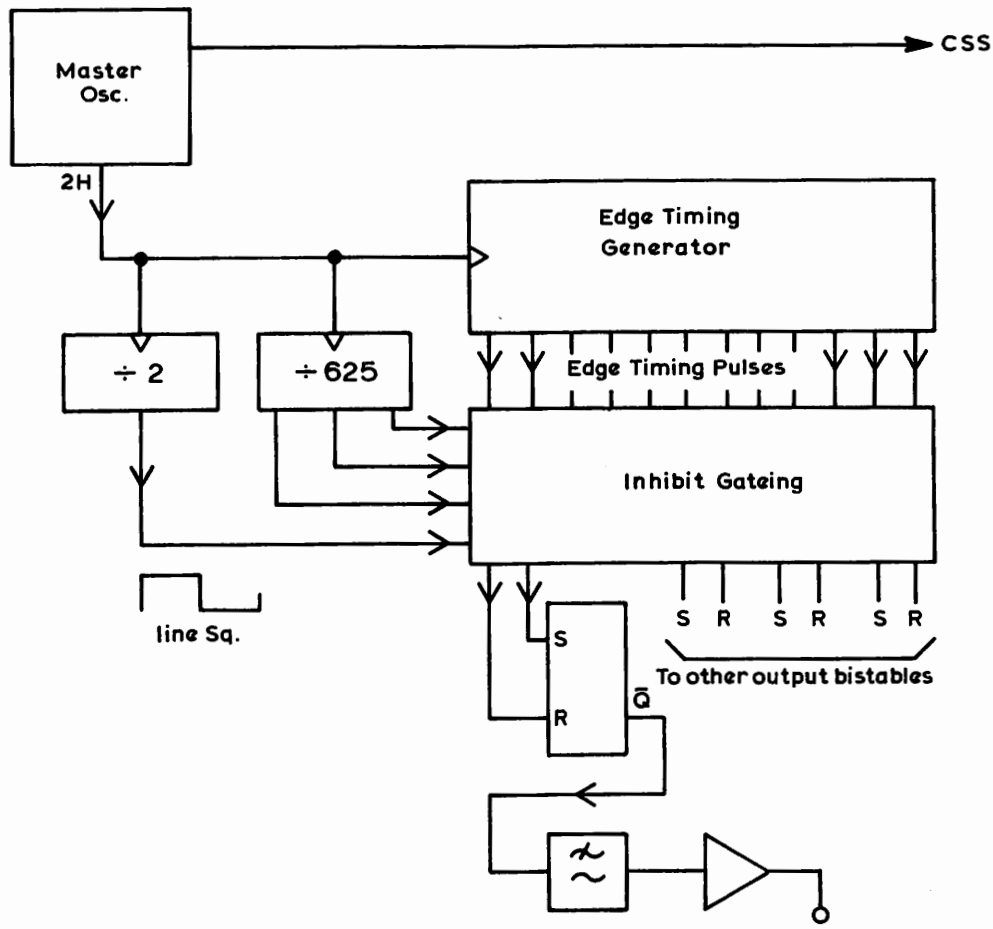


Fig. 8.1 Block diagram of S.P.G. (See 5.1)

8. SUMMARY OF SYNC PULSE GENERATION.

The sync pulse generator consists of:-

An edge timing generator, which is kicked, at 2H rate, into a burst of activity. The edge timing generator produces along its output wires every 32μs, all the pulses required to define each transition which may be made by any of the s.p.g. output waveforms.

The inhibit gating is used to reduce the frequency of these edge timing pulses down to line and field rate. To use a railway analogy, the inhibit waveforms open or close the points along the lines which feed trains of edge timing pulses to the individual set and reset inputs of the final S-R bistable elements.

SYNC PULSE GENERATION

The S-R bistables change state at the supplied edge timing to generate the output binary waveforms with the correct duration and relative timing.

The output filters and buffers are used to give the desired rise-time (usually much lower than that of the logic-level signals encountered earlier) and deliver each output to the outside world at the correct voltage level - usually 2V into a 75R load (except for V.A.S. and C.S.C. which are usually 1 volt into 75R for historical reasons).

9. MASTER CLOCK SOURCE

In section 5, it was mentioned that a complete colour sync pulse generator normally contains its own master clock source, from which correctly related subcarrier and twice-line frequency drive are obtained.

9.1 PAL CSC-Line Frequency Relationship

$F_{CSC} = 283.3/4 \times F_H + 25Hz$ ...(1/625 x FH)

It is difficult to synthesise F_H from F_{CSC}, (or vice versa), because of the 25Hz offset, and the non-whole number relationship between the two frequencies.

The colour subcarrier frequency has a frequency tolerance of ±1Hz, ie one part in approx. 4.5×10^6, (or 2 in 10^7 stability). This necessitates a stable crystal oscillator to achieve the PAL stability tolerance.

Most master clock circuits therefore use a high frequency crystal from which colour subcarrier may be derived (eg 4 x CSC - Seltech; 5MHz - BBC spg) and divide down to generate the related 2 x H rate drive for the edge timing circuits.

The use of a master 2H source and multiplying up to achieve F_{CSC} would have problems in achieving an accurate output subcarrier frequency, and a good enough tolerance, including short term jitter from the frequency multiplication process.

9.2 Non-standard Colour Subcarrier to Line Frequency Relationship

The precise relationships quoted in 9.1 was originally proposed to reduce the visibility of CSC on a monochrome display tube. If this relationship is lost, the CSC will produce a pattern which moves relative to the line structure of the scanning process. The eye finds rapid movements produce a greater stimulus than static patterns, and the subcarrier visibility increases.

However, more important to the production of television programmes is the effect on video tape replay.

Due to the mechanical write-read process of VT, the off-tape signal has timing variations which must be smoothed out before the signal will satisfactorily lock a monitor. The Timebase Corrector of a VT compares the tape signal timing with a local reference syncs and burst, of stable timing, from the station spg. The TBC then dynamically adjusts the delay applied to the off-tape signal, each line, to make the output timing match the stable reference.

At the output of the TBC, the signal's line and field components are the same frequency as the reference syncs supplied to the TBC. Also the phase and frequency of the off-tape colour subcarrier is the same as that of the reference subcarrier.

If the reference spg has a correct CSC-H frequency relation, but the recording source was wrong, then either:

1. The TBC can match the line timing, and the colour subcarrier timing will drift out due to the frequency difference.

OR 2. The TBC can correctly match the colour subcarrier off-tape to the reference, in which case the line timing will drift out!

In practice it tries to do both and a conflict occurs which results in colour dumping - correction of colour phase until the line timing error is beginning to be serious, when it corrects the line timing:- to do which it must temporarily lose color correction, or dump, causing a flash on the output picture.
The greater the loss of CSC-H, the more often it must dump colour correction to hold line timing somewhere near correct.

10. GENLOCK SPG

'Genlock' is the name which is given to the process of an spg locking its output timing to a supplied video feed, in colour, line and field phase. (Generator Lock).
To do this it must contain timing comparators to assess the error between the input signal colour, line and field timing and the generator's output signal timing.

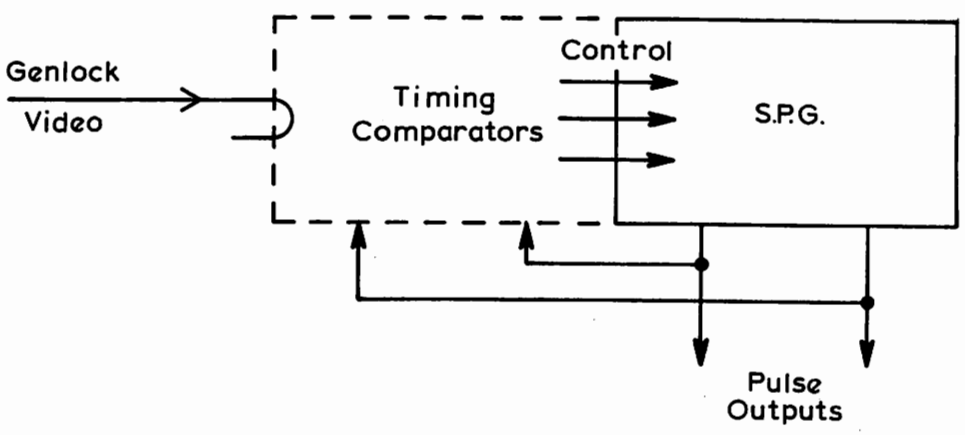


Fig. 10.1 Genlock modification to an SPG

One use of Genlock SPG is given below.

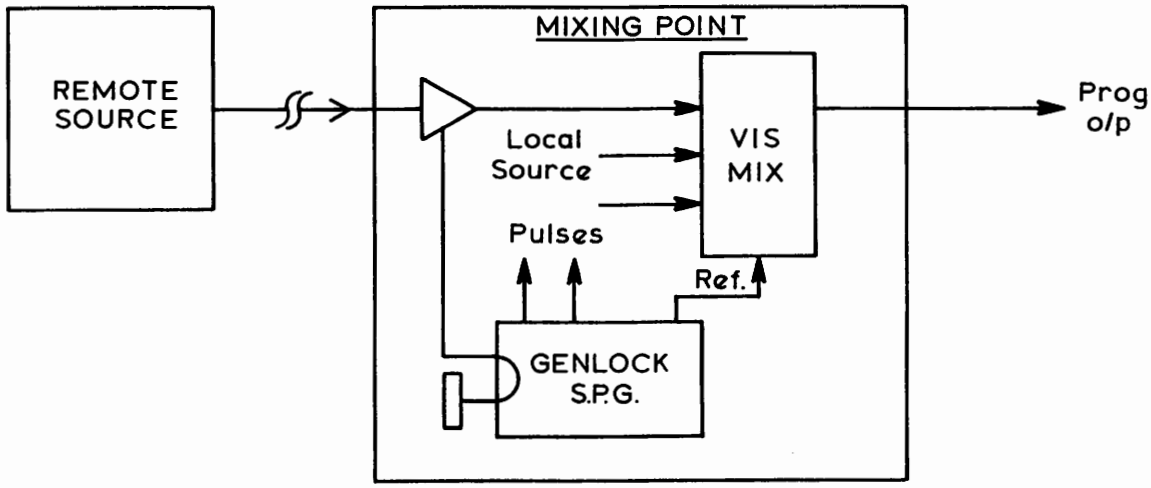


Fig. 10.2 Typical use of Genlock SPG

The mixing point studio is taking a contribution from a Remote Studio. By locking the mixing point pulses to the incoming video, the timing of the local sources to the mixer, generated from the SPG waveforms, matches the remote contribution timing, enabling synchronous operation of the vision mixer with the Outside Source.

10.1 Operation of the Genlock SPG

The requirement is for locking the colour subcarrier, line and field output timing to the relevant components of the genlock video signal.

10.1.1 Colour Subcarrier Lock

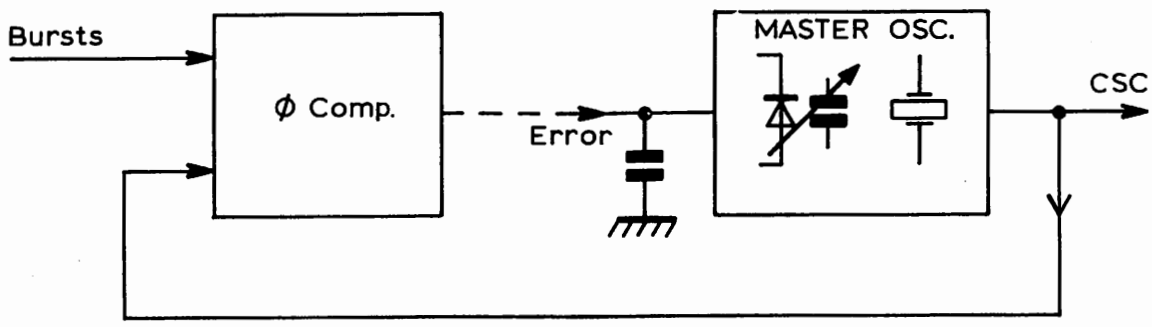


Fig. 10.3: Colour Phase Lock

SYNC PULSE GENERATION

The bursts separated from the genlock video are phase compared with the genlock S.P.G.'s subcarrier oscillator and a lock achieved with a long time constant to reject the burst 90° phase change on alternate lines; (as in a PAL colour decoder).
As with the decoder, a shorter time constant output is used to regenerate the VAS sequence of the remote bursts.

10.2 Line Lock

Line and field rate spg outputs are derived from a 2H clock. This can be supplied by a phase-locked loop, which is used to lock the spg line rate outputs to the incoming H syncs on the genlock video.

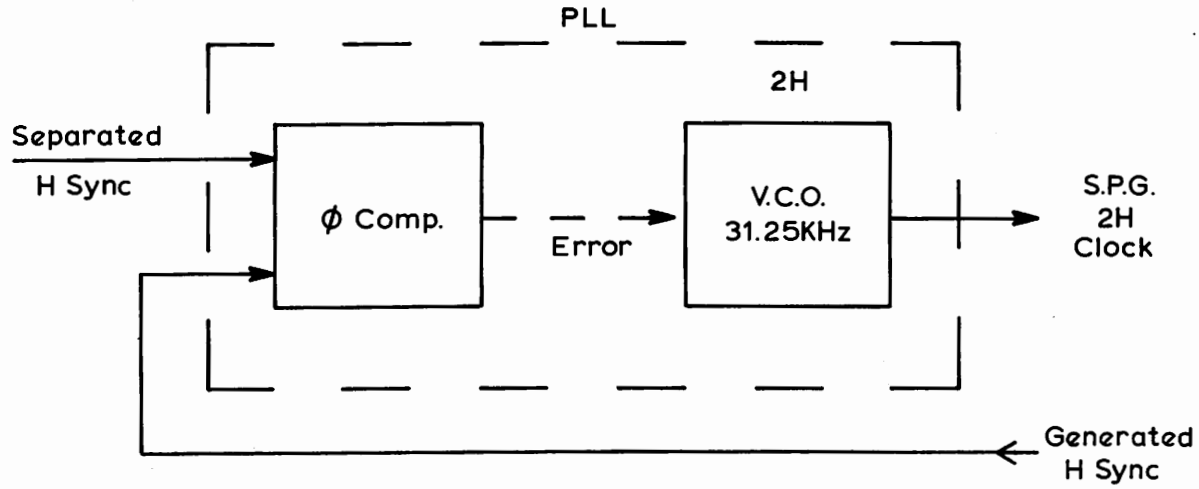
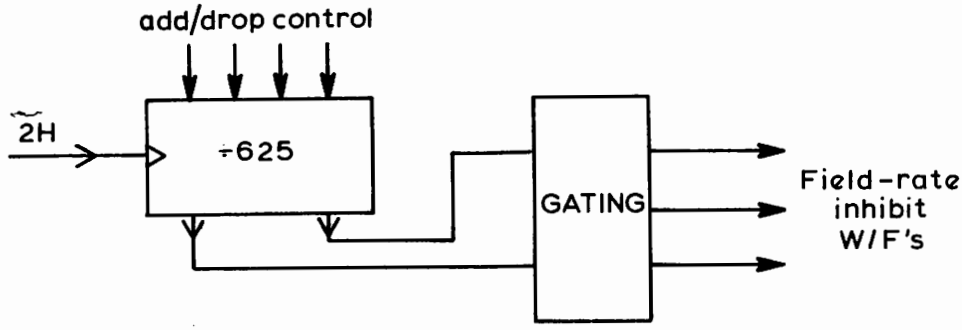


Fig. 10.4 Phase-Locked Loop for Line Timing

Once this loop is locked, the line phase and frequency is matched to the remote video, and therefore the field frequency is matched. (Generated by the same 2H clock) Since there is no telling which line number of the remote video is locked to a particular line of the generator o/p, the field phase still needs correcting.

10.1.3 Field Timing Correction



If the field divider count ratio is changed to ÷627, the time to the next generated field interval will increase by one line. The generated field interval will retard by one line/field relative to the field period on the input video.

Change to ÷623, and the generator field period advances by 1 line per field.

The field timing comparator causes a change in division ratio if an error of field phasing exists when the line timing has been locked.

10.1.4 Speed of Timing Correction

The Time constant of lock for both the CSC and Line timing locked oscillators can be of the order of a few lines, or tens of lines, so that both lock very quickly after a non-sync cut in the genlock video.

The rate of field lock should be slowed down to an acceptable rate for the following reasons:-

a. Monitor and receiver field timbases are often driven by a crudely synchronised oscillator. If the input signal suffers a sudden large change in field sync timing, the oscillator will free-run at its natural frequency until its output phase is close to the new field sync phase, then lock will occur.

   The period of free running causes a 'field roll' which is disturbing to the receiver.

b. Mechanical devices such as TK and VT are usually servo-locked to the television field component. A jump change in field phase of the VT reference could cause older servos to to completely unlock, taking more time to re-phase and stabilise during which time the output was unuseable.

For both these reasons, a controlled slewing of the generator output field phase was desirable, at a rate which timebases and servos could follow without losing lock.

10.1.5 Practical Field Divider Division Changes

The rate of field correction depends on the number of lines/field by which the field divider is allowed to miscount.

a. ±1 count per field, (±½ line/field). The position of field syncs relative to line syncs is advanced or retarded by ½ a line per field, each field, until lock is achieved. Maximum error needing correction ±½ field, ie 150 lines at ½ line per field ≅ 6 seconds.

During correction each field length is an integral number of lines, ie 312 or 313, therefore interlace is lost.

b. ± 2 counts per field (± 1 line per field). Field sync stepped by ± 1 line per field until lock occurs. Maximum error 312 lines - correction time still 6 seconds.

Interlace is maintained since each field is still n + ½ lines long.

Both these methods do not take account of the 4 field PAL colour sequence involving VAS. Generators using this method apply a sudden reset to VAS to invert its phase if the four field sequence is 180° out when field lock is achieved. This may cause a colour flash under certain conditions.

c. ± 4 counts - ± 2 lines per field.
This method can be used so that the VAS sequence does not have to be disturbed - a field 1 is followed by a field 2 etc. - but therefore the maximum error may be up to 624 lines, still taking 6 seconds to correct.

A consequence of correcting by 2 lines/field is that the local and remote VAS must already be matched. The solution is to lock the line timing (section 10.2) using a comparison of local and remote VAS, thus giving a two-line lock before field correction occurs.

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13th September 1983