DIGITAL STORAGE - THE EFFECT OF PAL CSC - SYNC RELATIONSHIP IN STORING COMPOSITE PAL w/f's

INTRODUCTION

In many digital stores, only the active line-time of the television waveform is stored. This saves store capacity, since the blanking and sync periods are easy to regenerate at the output. The writing of information to the store is stopped for most of the input blanking period; as is the reading of data from the store during the output blanking period.

This information sheet outlines how to choose where to 'start' and 'stop' the store activity.

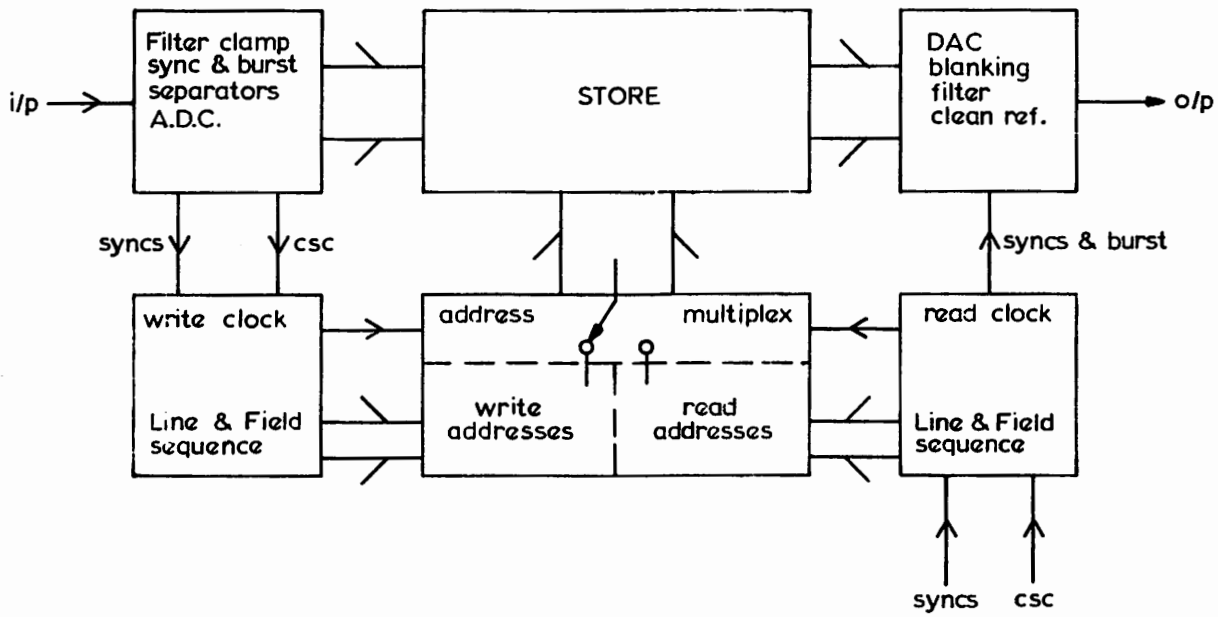

Fig. 0.1 Simple Store block diagram

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1. Monochrome signals

To clock the signal into store, the clock used will be a multiple of line frequency, ie line-locked. Stores are usually organised so that a new store area is selected at the start of the line, and each successive clock pulse puts a new digitally-encoded sample sequentially into the storage cells in this store area;

The selection of a new storage area will occur each line, but, if the clock were free-running the timing of the first clock pulse for storing data could vary by ∓0.5 clock period relative to syncs; and the line-by-line picture timing would be ragged.

Using a typical clock frequency (greater than 2.2 x F signal max.) of 852 x line, the clock is derived as in fig. 1.1, using a phase-locked loop.

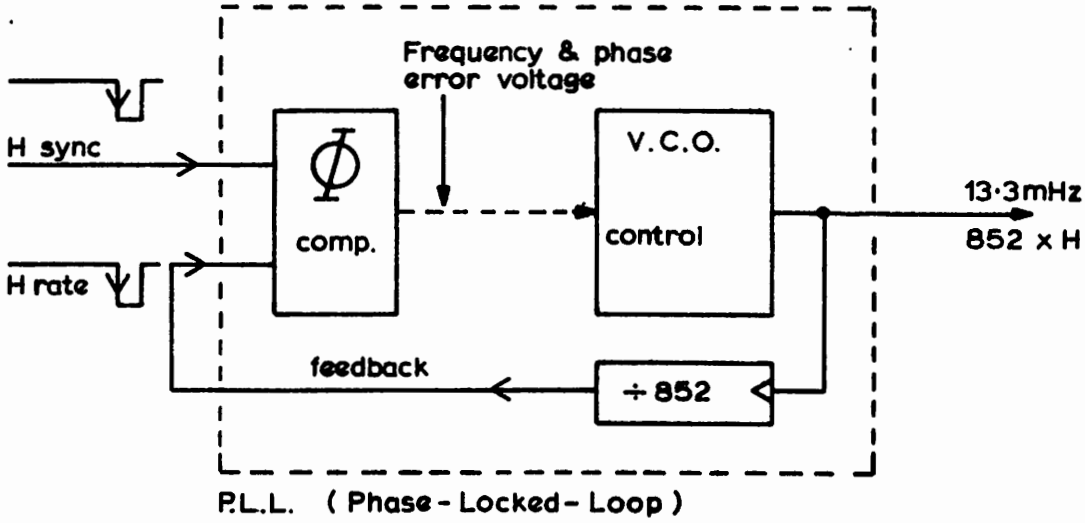

Fig. 1.1 Line-locked clock frequency

The voltage-controlled oscillator output is divided down to line rate and fed back to a phase-comparator with input line syncs. The error voltage steers the oscillator into frequency and phase lock.

1.1 Store Capacity per line

There are 852 clock pulses generated per line of television signal, but some of those occur during line blanking. If we only activate the store for 768 clock pulses, then 84 clock pulses are ignored, a time of about 6.3μs, which is less than the blanking period. All the active line plus some blanking will be stored.

The 768 clock pulses per line will cause the store to write successive digitally-encoded samples into 768 sequential address locations.

Why 768? It's a convenient multiple of 256, making the allocation of memory addresses easier.

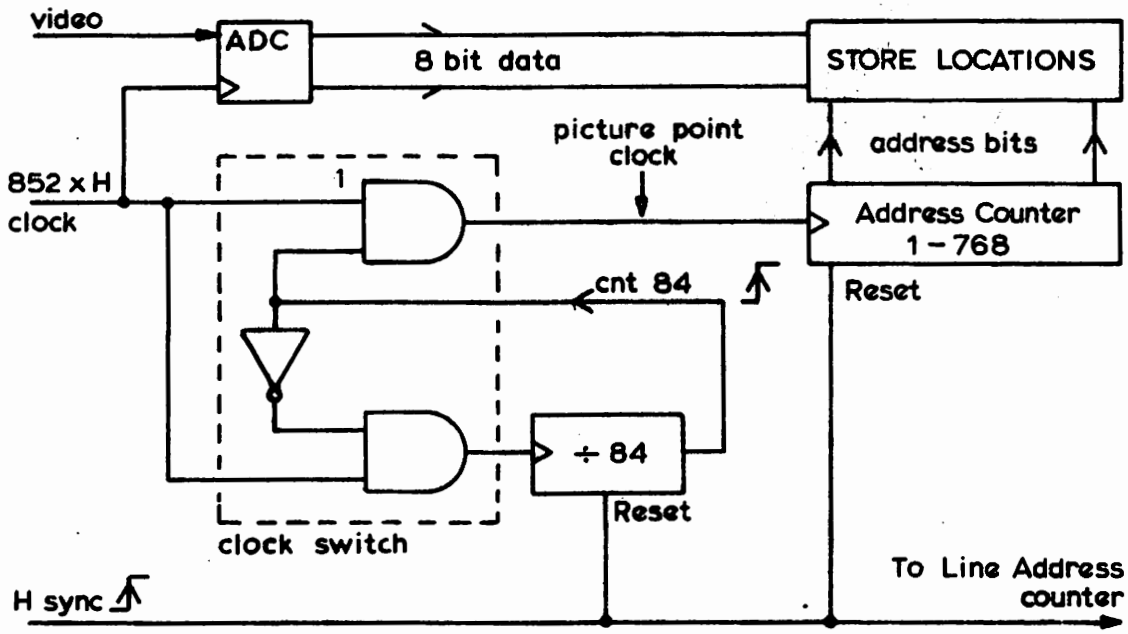

Fig. 1.2 Simple Store Addressing

The A.D.C. converts 852 samples per line. The store operation is held until 84 clock pulses after the line sync, when gate 1 opens allowing the address counter to count up from 1 to 768.

This gated clock is often called the Picture Point Clock since it causes the storage of picture elements; and the Address counter is called the Picture Point counter. Having reached 768 the counter is reset, ready to address store elements for the next line.

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Next Line? Yes, there must be a line counter as well, which directs the next 768 addresses to a new storage area.
This system of Picture Point clock generation is satisfactory for monochrome, or where separate stores are used for the component video waveforms of a colour signal; Y,U & V.

1.2 Store Reading

The reference line syncs are used in a similar circuit to figs. 1.1 and 1.2 to derive Read Clock and Read Picture Point addresses.
The output video will be correctly timed if the Read Picture Point Clock is gated 'on' 84 clock pulses after Read Sync, (but this can be altered to vary the output horizontal phase)

2. PAL Composite Colour Signal

If a PAL Composite colour signal is being stored, not only must the timing of the video luminance information be correct at the output, but the phase of subcarrier must be correct on each line at the output.
The elegant solution to this is to start the write (and read) process at the same point relative to a subcarrier cycle, say the +ve zero crossing. If the clock frequency is then a multiple of CSC, say 3x, then each store location will contain a known phase of C.S.C.
In practice, a burst-locked oscillator is locked to the mean phase of the burst. Its output is multiplied by 3 to give the A.D.C. and store clock signals.
The picture-point clock is gated on at a zero-crossing of the B.L.O. output, and 768 clock pulses allowed through. The P.P. clock is stopped for 84 pulses and then gated on for the next line.

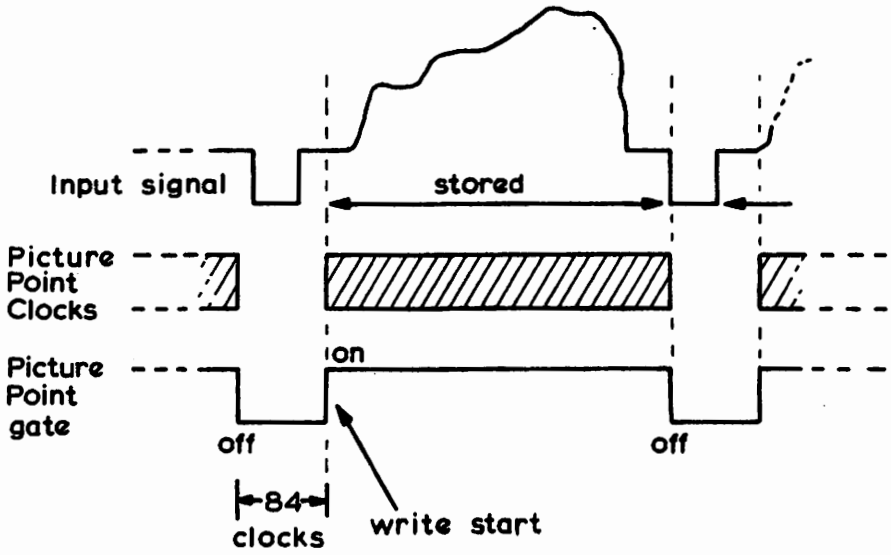

Fig. 2.1 Picture Point Clocks and Picture Point Gate

852 clocks per line at 3 x CSC, is 284 cycles of subcarrier per line. But in one exact line period there are only 283+0.75 cycles of subcarrier!

The picture point gate must occur at the same time, relative to CSC on each line, in order that the phase of subcarrier in each store location is predictable. It will therefore go 'on' at the 284th zero crossing of colour sub-carrier after it last went on.

Relative to line syncs, the picture point gate is 90° of CSC later along each line.

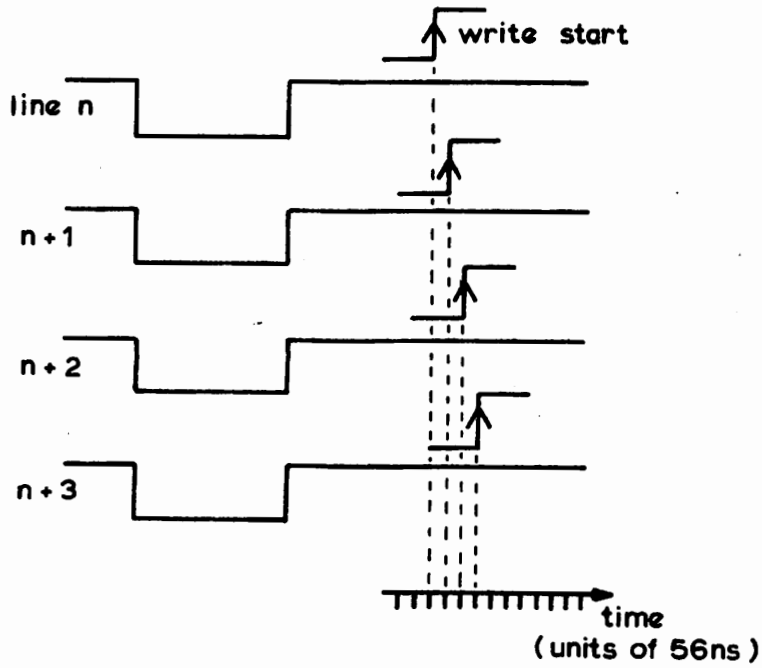

Fig. 2.2 'Write start' relative to line sync

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This can't be allowed to go on for long, since the gate would soon be opening in active line time!

After four lines, the write gate has been displaced by one cycle of subcarrier towards the active picture time. On the fifth line, the clocks are only stopped for 83 counts, to make the write gate open at the same time along the line as it did four lines ago, ie jump back by one cycle of subcarrier.

The average number of cycles of subcarrier per line in this four line period is:-

= (284 + 284 + 284 + 283)/4

= 283 + 0.75

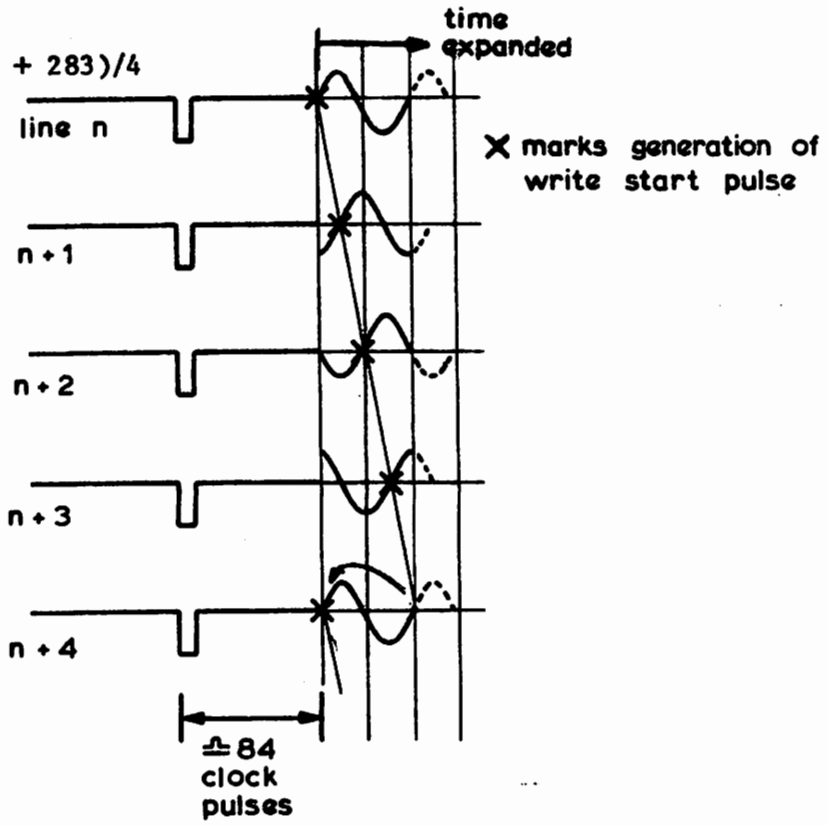

Fig. 2.3 CSC - Line Phase Relationship

BUT Fpal = 283.75 x FL + 1/625 of FL, (25 Hz)

Remember the 25Hz offset? That means that one extra cycle of sub-carrier occurs in each 2 field period, compared to the simple approximation we have used up to now:-

ie approximately 0.5 degree, advance, per line, of the selected zero crossing occurs over two fields.

If we want to be sure of getting a consistent write start pulse locked to colour-sub-carrier phase, but still storing nearly the same part of the television line waveform, a predictor must be built to enable us to follow a particular subcarrier zero-crossing through its 4-line and 2-field phase variations with respect to line sync.

2.1 Use of a Sync-Subcarrier Predictor

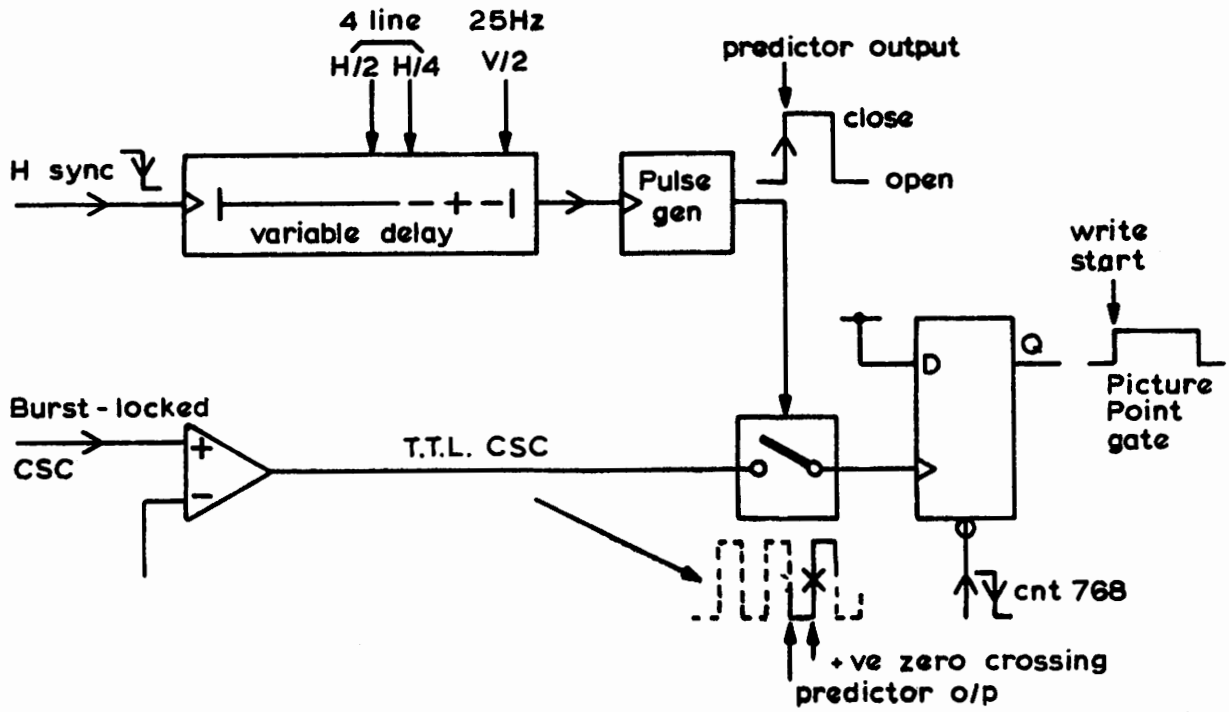

Fig. 2.4 Selection of a CSC zero-crossing

The output time of the variable delay is modulated by + 56ns/line in a 4 line sequence, and by -225ns over a two field sequence. The output should therefore occur accurately just before a +ve zero-crossing, and track the phase variations of CSC with respect to sync on each line of the picture.

You may have noticed that there is no absolute phase relationship in the PAL waveform between CSC and syncs, eg that on line 1 of field 1 a positive zero crossing of subcarrier will occur exactly at the mid-point of sync leading edge!

So when the predictor output occurs, it may find a zero crossing anywhere between 0ns and 225ns away, whose phase variation it must track. To enable it not to be thrown by the odd noisy signal, it would be healthier if the predictor output occured about 0.5 a cycle before the wanted zero crossing. Differential jitter between sync and subcarrier of up to 110ns could then be tolerated.

The time period between predictor output and selected crossing is measured, and the long-term delay in the predictor gently steered to give the required half subcarrier cycle between the two. Quantel call this circuit a 'BIT PICKER', possibly because it 'picks' the 'bit' of the waveform just before a subcarrier +ve zero-crossing!

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2.2 Read

The read process occurs in much the same way. Since each line is stored with the same phase relationship to mean burst in each location (although VAS affects alternate lines), the correct PAL output will be given using a 3 x Read subcarrier (station ref.) clock and a Read start pulse modulated by +56ns per line and -225ns over two fields.

The phase of the chroma coming out of the store will have a fixed relationship to station syncs and subcarrier independant of the source applied to the input.

3. Summary - Store Clock Generation

3.1 Storage of 625-line video requires a clock frequency ~2.2 x 5.5 MHz, and around 13.5MHz is convenient.

3.2 Mono or component video uses a line-locked clock, produced by a P.L.L. with a divider in the feedback path.

3.3 Blanking periods need not be stored, hence only a convenient number of pixels, or picture points need be stored eg 3 x 256 (768).

3.4 To store composite P.A.L. signals, these 768 pixels should have a simple relationship to colour subcarrier. This gives them a complex relationship to line sync, and makes it difficult to identify the precise point along the line to start the store process. A sync-subcarrier predictor must be used.

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4. Digital T.B.C.s FOR HELICAL SCAN eg TBC-2

The output of a helical scan v.t.r. demodulator has timing errors of typically ∓1.5μs at normal replay speed. The rate of change of timing is however very slow. Since the head drum has high inertia, timing errors are mainly caused by longitudinal "wow & flutter" type speed variations of the tape.

The digital T.B.C needs to write the time-varying input signal into a digital store, using a clock signal locked to the off-tape time variations. The signal is read out several lines later using a stable clock locked to replay reference pulses.

4.1 Store Clocks - Problems

The store holds 256 x 3 samples per line at 3Fsc, in a shift register store of 12 lines capacity.

The phase of subcarrier in each store location should be predictable, and the start of the write process should therefore be derived from the off-tape subcarrier.

A burst-locked oscillator used to follow the mean phase of a PAL burst has to have a long TC to reject the 7.8kHz VAS component of the burst phase. With the superimposed timing variations of the v.t.r. system, the b.l.o. would have difficulty following the timing error of ∓1.5μs (∓ 7 cycles at CSC).

If the time constant were low enough to enable rapid following, there would still be a following error and there would not be sufficient rejection of 7.8kHz burst phase alternation.

4.2 Derivation of Store Clocks

The clock signals for the store must be derived by a circuit able to respond to line-by-line variations in CSC phase.

We have seen a predictor designed to follow a particular zero-crossing of a stable subcarrier locked to the mean phase of burst. Similarly, the T.B.C. must pick out a particular zero-crossing of the burst of the off-tape signal, since this will give line-by-line timing variations.

If colour subcarrier is used to generate a PAL burst, what will be the phase variation of a selected +ve zero-crossing of the burst, relative to the sync leading edge?

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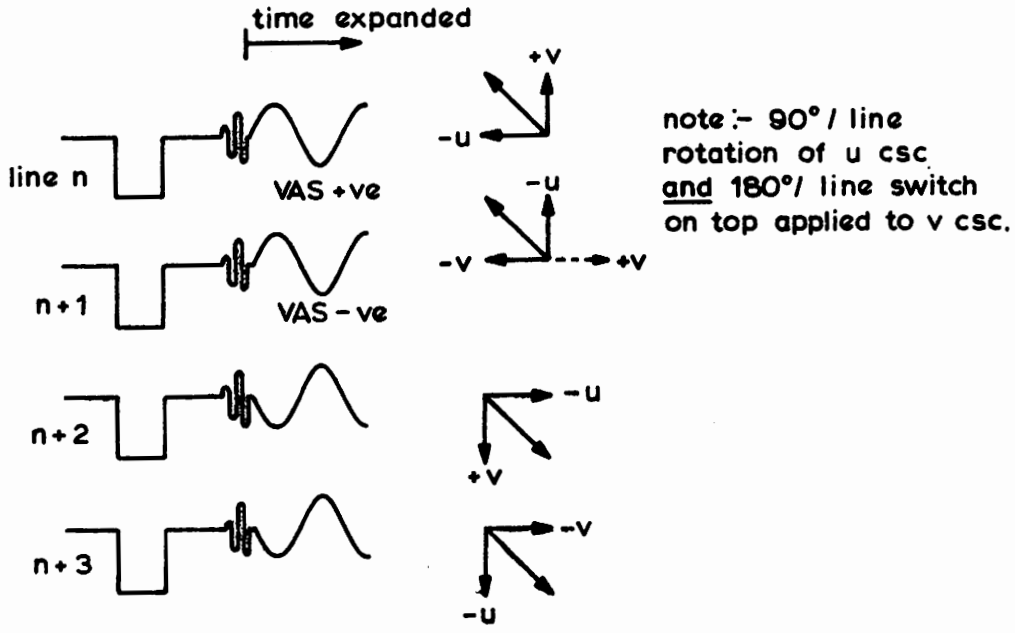

Fig. 4.1 Burst to Line Sync
phase variationsfor PAL

Fig. 4.1 shows that the PAL burst, being a combination of u and switched ∓v subcarrier, has a four-line sequence which has two lines of the same phase, followed by two lines of 180° shifted phase.
Both these vectors would gradually rotate to achieve one extra cycle per 2 fields, ie the PAL 25 Hz component.
A predictor to follow a particular crossing in the burst, approximately 84 clock pulses after sync leading edge, would therefore be:-

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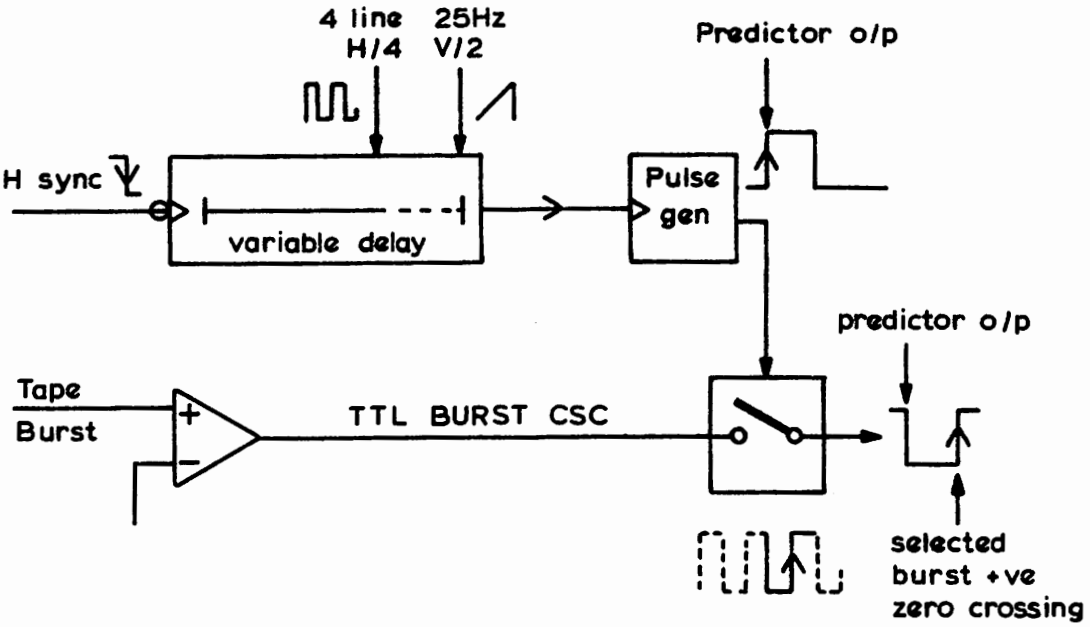

Fig. 4.2 TBC-2 Burst Tracking

The predictor closes the switch just before the selected burst crossing. The steering circuit ensures that the maximum of burst--to-sync differential jitter will be tolerated before 'losing' the selected crossing.

4.3 Write Control Signal

The selected burst-crossing has an H/4 (3.9kHz) modulation backwards and forwards by 113ns (180° at CSC) relative to line sync, plus the one cycle in two fields due to 25Hz.

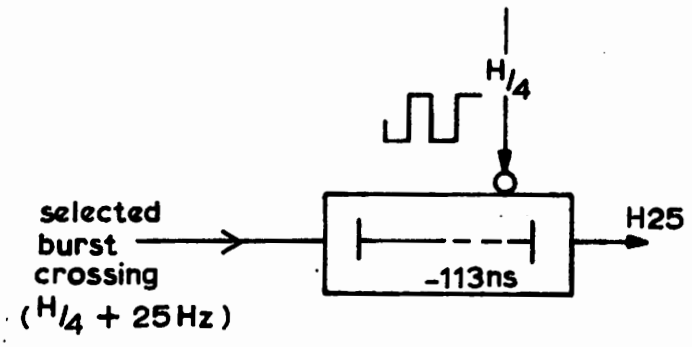

Fig. 4.3 Removal of 4-Line Sequence in Burst Crossing

A monostable is clocked by the selected burst crossing. The time period of the mono is modulated by -113ns using an H/4 square wave, so that the Q +ve transition, ie the end of the time period, is constant.

It still has the V/2 modulation (25Hz) and is basically a line rate signal, so we shall call it H25.

This signal is a once-per-line edge about 84 clock pulses (at 3Fsc) after the leading edge of sync.

The write process needs to start, on each line, at the same point in a CSC cycle to enable the store information to have a known relation to CSC.

The H25 pulse is delayed by 0ns, 56ns, 113ns, 169ns (0°, 90°, 180°, and 270° at CSC) on a four-line sequence controlled by H/2 (VAS) and H/4 (3.9kHz) derived from the i/p signal.

This then starts the writing into store at <u>about</u> the same time on each line, but locked to the CSC phase sequence.

4.4 TBC Write Clocks

A phase-locked loop locks an oscillator to the H25 off-tape line-rate signal previously used to derive write start.

For ease of division the oscillator is run at 4 x CSC, which divides by an integer, 1135, to give a line frequency signal which also has H25 modulation.

Thought we said a phase-locked loop wouldn't follow fast enough? We did. But there is little line-by-line phase variation on the H25, except for that due to time-base errors, so a fairly fast lock-up time can be chosen.

It cannot however lock-up instantly so there <u>will</u> be a following error between the oscillator output and the off-tape H25.

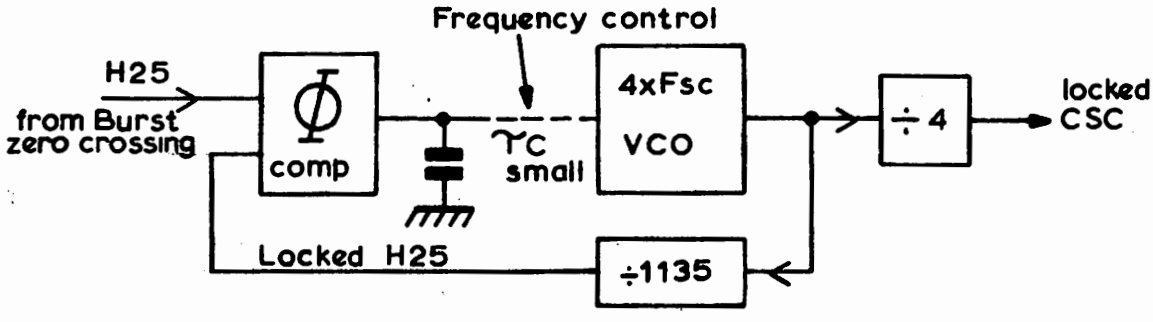

Fig. 4.4 Basic phase-locked Loop

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The CSC can be multiplied by 3 to give 3 x Fsc for the ADC and store clocks.
First however, due to the capacitor filter in the error path of the P.L.L., the full off-tape timing variations have been lost in the locked C.S.C.

So, once per line, the error between the new H25 pulse and the oscillator H25 output is sampled and held, and used to drive a phase modulator to correct the phase of the oscillator output.

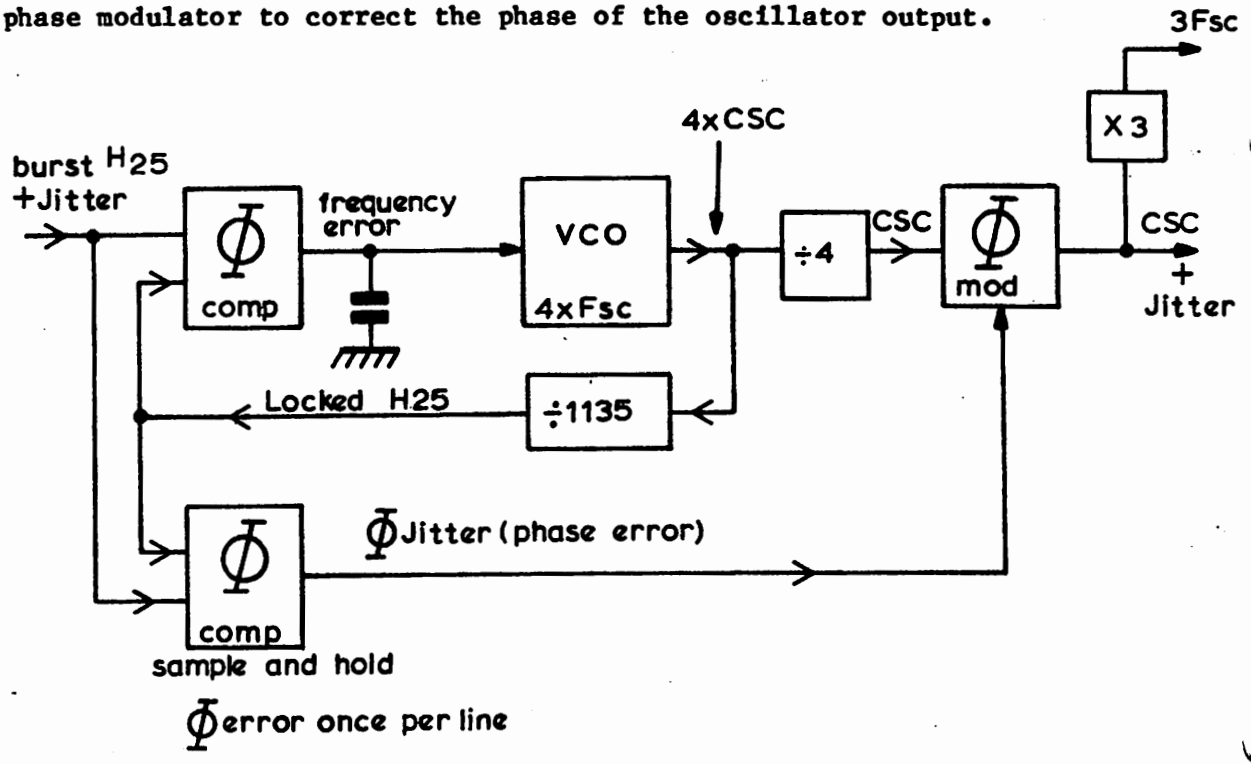

Fig. 4.5 P.L.L. with Output Phase Modulator

The fast timing errors on a line-by-line basis are thus used to ensure that the store write clocks follow tape timing variations.
When store reading occurs under the control of a stable read 3Fsc, the majority of the timing errors will have been removed. Only the very fast errors causing changes across the line (velocity errors) remain to be corrected.
Notice that the read start signal must be a line-rate pulse modulated by a 4-line and 2-field sequence (derived from station syncs) in order to restore luminance vertical lines and give the correct subcarrier frequency at the output.

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24th May 1982