# VIDEO:- TO DIGITS AND BACK

## INTRODUCTION

The analogue video waveform becomes a digitally-encoded signal in two stages.
Firstly, the continuous video waveform is broken up into discrete samples, taken at regular intervals along the waveform.
Secondly, each sample has its voltage level converted to a number, which can then be transmitted in a binary code.

This information sheet gives the terms used to describe digital video signals, and shows how each stage may be engineered.

The aim of this information sheet is to provide a grounding to enable the reader to study synchronisers, time base correctors, standards convertors and digital effects stores using digital video encoding.

## 1. SAMPLING

Each point on an analogue signal has two properties:- Amplitude and Rate of Change. If a regular sample of the amplitude is taken, and held on a capacitor until the next sample time, the rate of change information is lost.

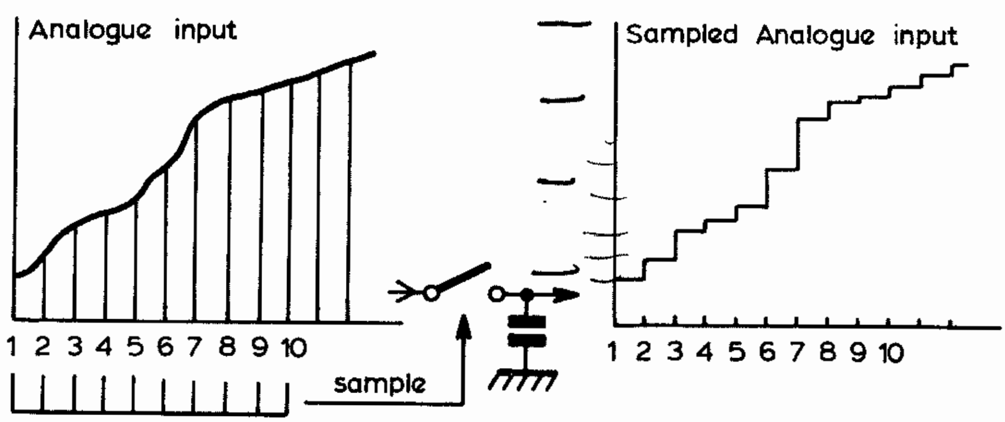



Figure 1.1: Sampling an Analogue Signal

A triangular wave component at sample frequency has been superimposed on the analogue signal. (Imagine subtracting one from the other, using a differential scope).

A triangular wave has components at fundamental frequency and its harmonics, so the spectrum of the sampled signal will have components at sample frequency Fs, and also 2Fs, 3Fs etc.

Since the amplitude of the steps in the sampled signal will depend on the original video, the sampling frequency components will have sidebands around them up to the highest frequency in the original video, ie they are modulated by the baseband video.

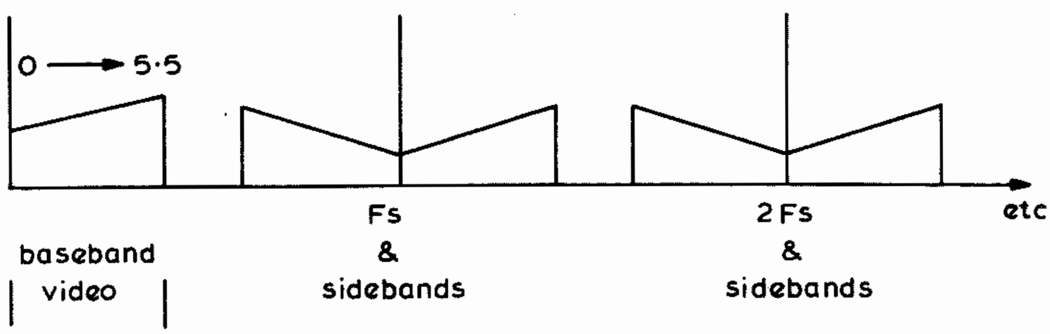



Figure 1.2

## 1.1 Choice of Sampling Frequency - who is this Nyquist they all talk about?

From fig. 1.2, you could imagine that if Fs is lowered below twice the highest video frequency, the signal at baseband will become tangled up with the lower sideband of the sampling frequency.

No amount of simple low pass filtering can remove these side band signals from the wanted baseband video. Any high frequency present in the input video would therefore have a resultant lower sideband component inside the video bandwidth, giving spurious interference and intermodulation products on the baseband video. The effect is called aliasing!

Because an infinitely sharp low-pass filter cannot be made, a safe rule of thumb is that Fs, the sampling frequency, must be at least 2.2 x the highest signal frequency. (Nyquist first formulated this rule).

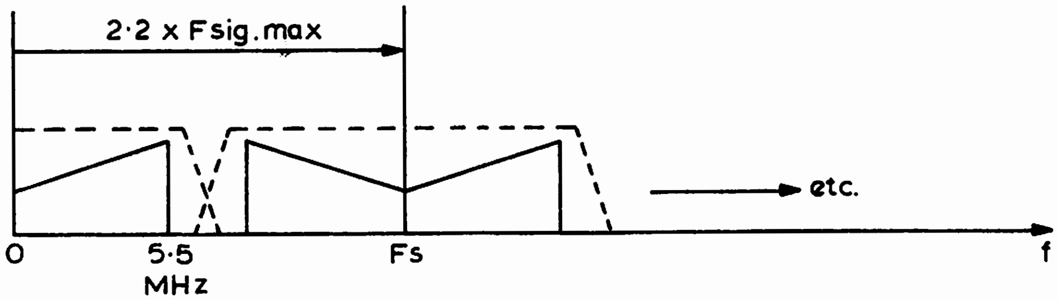



Figure 1.3: A Practical choice of Sample Frequency

The dotted line shows the effect of the low-pass filter before the sampling process, which prevents spurious out-of-band signals on the video source from producing aliases.

For video, a slightly higher sample frequency is preferred, to put the cut-off frequency of the low-pass filter further outside the video band. The phase disturbances around cut-off frequency then have less effect on the video waveform.

## 1.2 Transmission

Each of these discrete samples can then be converted to a number; these numbers can be transmitted sequentially to the destination, where the original sampled waveform, (and its spectrum), are re-generated. A low-pass filter is used at the output to remove the sampling frequency and harmonics, and associated sidebands.

A complete system looks essentially like figure 1.4 below:-

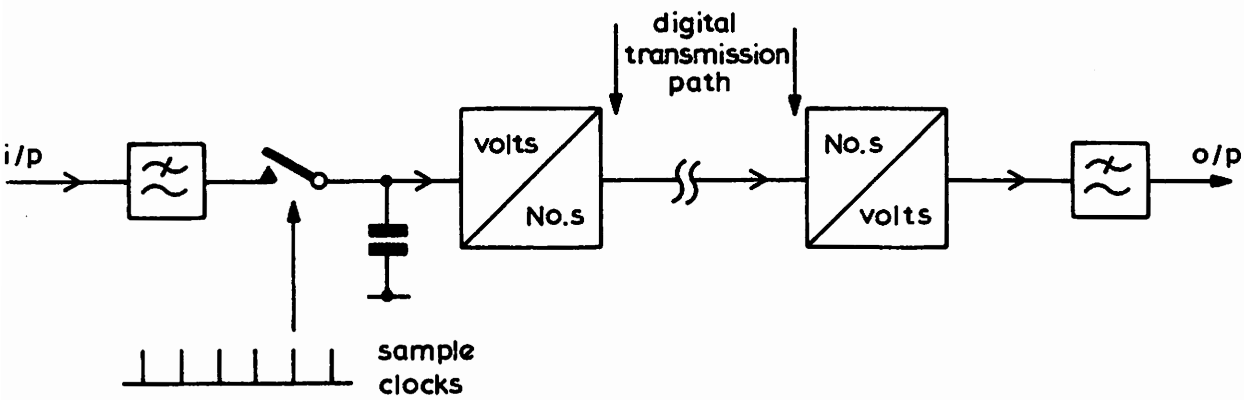



Figure 1.4: Simple Digital Transmission System

## 1.3 H.F. Loss due to Sampling

The sampling process, and the holding of the sample value between sample points, gives rise to high frequency loss on the baseband signal recovered from the output.

This will be explained in the section on Digital to Analogue Conversion, where the equalisation for this loss is located.

## 2. DIGITAL ENCODING

The amplitude of each sample of the signal voltage can be encoded as a binary number for transmission. The sample frequency for video waveforms is high, and a very fast convertor must be used.

### 2.1 How Many bits are needed?

If 8 bits are used to describe the sample's voltage, it may occupy only 256 different levels. For 0.7V p-p picture signal, the output voltage steps would be ≈3mv p-p using 8-bit encoding.

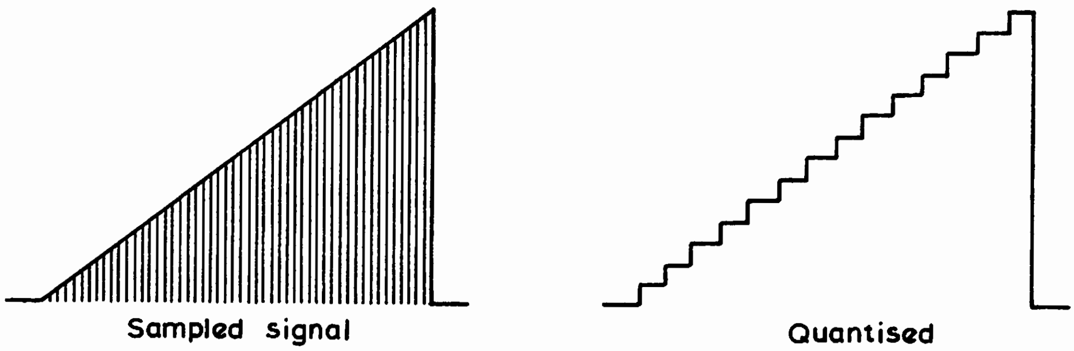



Figure 2.1: Signal Quantisation due to using a finite number of bits during encoding

Since the original continuously-variable analogue input was not composed of multiples of 3mV, the signal is said to have been quantised. (Made up of multiples of the basic quantity, or quantum)
In visual tests, 7-bit coding gives satisfactory pictures at normal viewing distance, using one encode-decode process.

Eight-bits is the minimum acceptable number of bits/sample for broadcast equipment, where several codecs may be used in tandem.

## 2.2 Colour Signals - Effect of Voltage Range

In the previous section we talked about the signal having 0.7V p-p range (It is usual in digital storage to store only the active line period. Syncs do not need to be stored, but are re-generated at the output.)

The composite colour signal, however, extends from the tips of subcarrier on a 100%, fully saturated, yellow, to the subcarrier troughs of a 100% fully saturated blue. (See Figure 2.2).

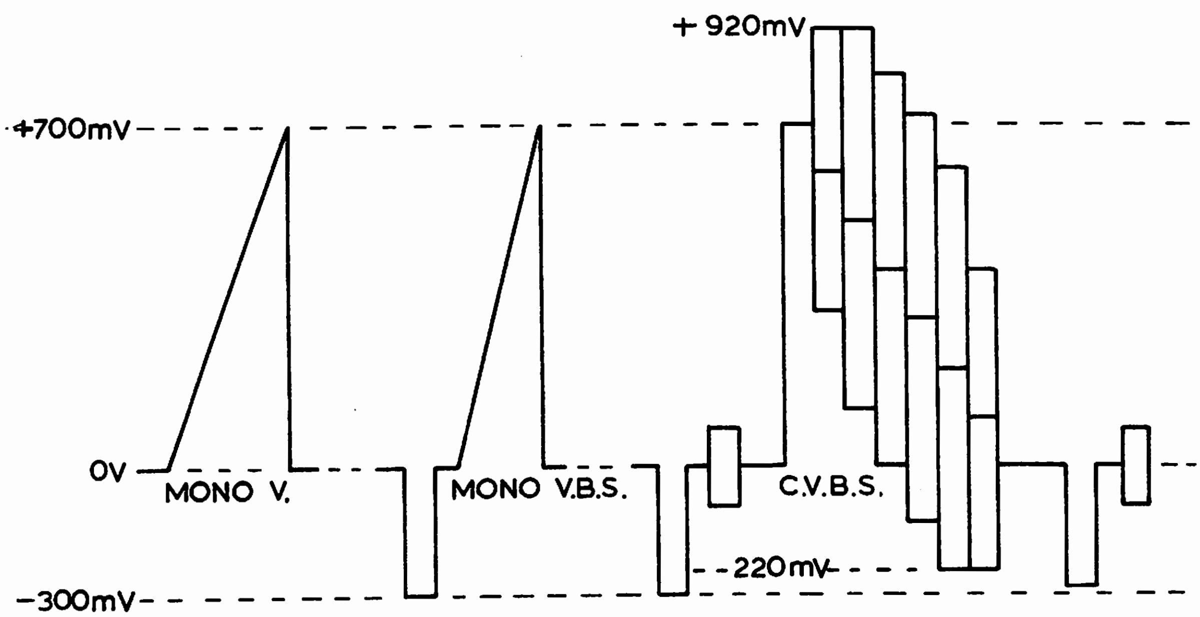



Figure 2.2: Comparison of Mono and Colour Signal Range

For the mono signal, or Y only, each quantising step can be 3mV. For the composite signal each step must be over 4mV, ie the luminance range of the composite signal occupies fewer steps.

Quantising noise is caused by the error between the actual analogue voltage, and the nearest quantised step which will represent that sample through the digital encode-decode process.

The larger the quantising steps, the greater the quantising noise.

This is one reason why the PAL signal may be decoded to its Y, U and V components before storage, each one being sampled and 8-bit encoded. The Y component signal then has a better signal-to-quantising-noise ratio than using the composite PAL waveform. (But a PAL decoder and encoder has to be used either side of the digital process).

2.3 Typical Systems using composite PAL waveforms lock the sampling to a multiple of CSC, eg 3 x CSC frequency (13.3MHz) or 4 x CSC frequency (17.7Mhz) giving bit rates of 106.4 M bits/sec and 141.6 M bits/sec, respectively.

2.3.1 This is very fast for serial transmission, e.g. over satelite, micro-wave, or optical fibre links, especially since error protection (using parity bits) and a framing code, will need to be sent as well, which increases the required bit rate by about 25%.

This has led to much work on reducing bit rates, for example:

1. Using differential pulse code modulation (d.p.c.m.) where only the, usually small, changes in amplitude between samples is sent, using fewer bits; and
2. Sub-Nyquist sampling - where the sampling frequency is less than twice the highest signal frequency, typically using 2 x colour sub carrier frequency sampling. This sampling frequency acting on the video waveform, with its energy concentrated in harmonics of line frequency, puts the video aliases in the gaps in the baseband video spectrum. A comb filter can be used to remove the aliases, with the usual loss of diagonal resolution.

2.3.2 Component video, in the form of Y,U and V video waveforms, can be sampled with a line-locked clock. The internationally agreed sample frequencies are 13.5 MHz for Y, and 6.75 MHz for each of U and V, thus doubling the bit rate over composite sampling.

Component video has a number of advantages:-

1. it is easy to accomplish SECAM-PAL transcoding at the same time.
2. it is easy to add picture manipulation, (size, shape, position) whilst in Y,U,V.
3. slight clock jitter only produces small picture shifts on Y,U,V, compared to serious phase errors in a Composite PAL system. (c/f, a 20ns clock phase error = 1/5th of T, the smallest video element, but 30° phase error at CSC frequency).

## 2.4 Picture Storage - Demultiplexing

For any form of picture storage, parallel data processing is used. (At the serial data rate of, say, 106 M bits/sec, each bit would have to be stored in 10ns).

At the output of the 8-bit Analogue to Digital convertor, an 8-bit word is produced every 75ns (13.3 MHz sampling). This is still too fast for the access time of most stores, so the signal is demultiplexed to occupy more parallel wires at a slower clock rate.

E.g., Ampex TBCs

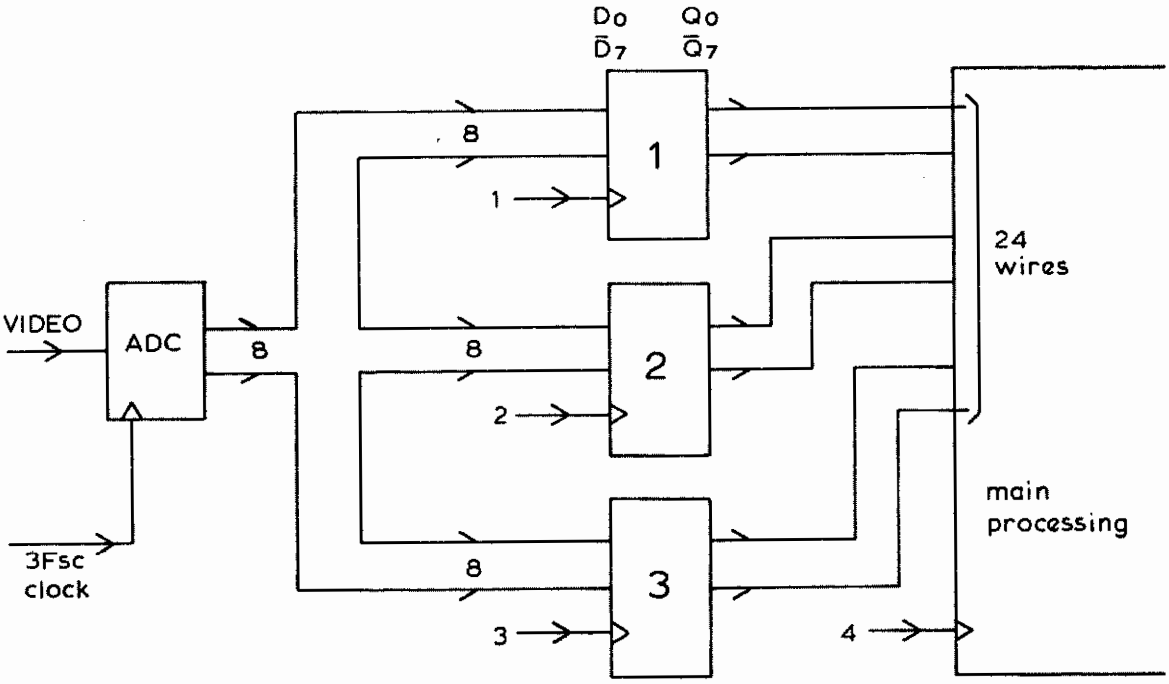



Figure 2.3: Demultiplexing by 3

The samples at 3Fsc from the A.D.C. are held in 8-bit latches. The first sample to latch 1, next to latch 2 and the next to latch 3. At this point, 3 separate 8-bit samples are available on the 24 outputs of the three latches, and are clocked into the main processing.

The main processing clock runs at 1/3rd of the sampling clock, ie CSC rate, with a period of 225ns. The clock waveforms are given in fig. 2.4

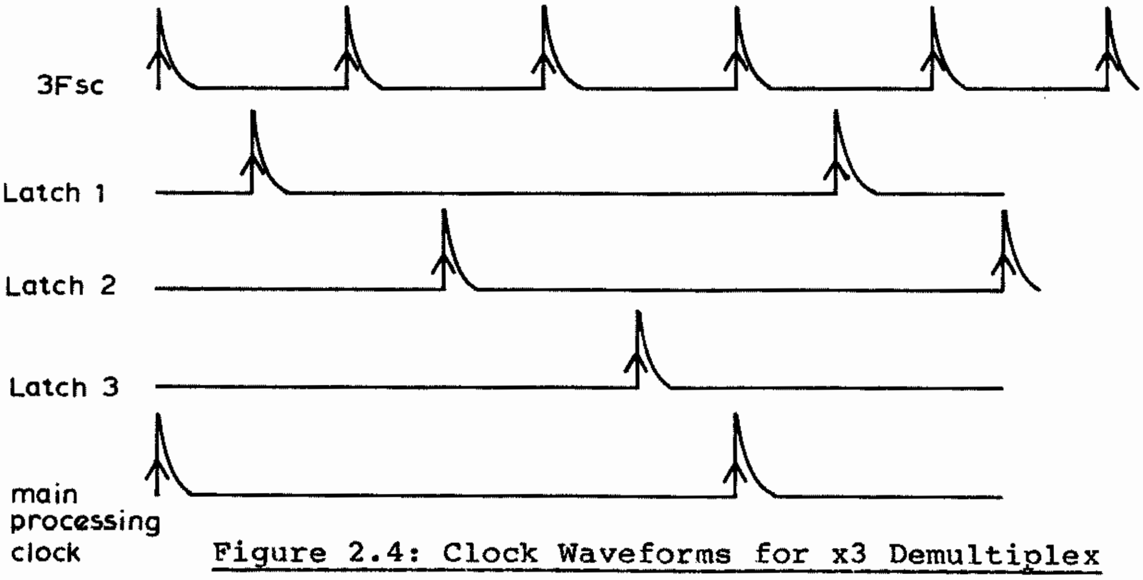



Figure 2.4: Clock Waveforms for x3 Demultiplex

The 24-wide store output is multiplexed to 8-bits at 3 x Fsc before D.A.C.

E.g. Frame Stores.

A typical commercial frame store might have 16 store cards, accepting in sequence 8-bit words from the A.D.C. After 1.2μs each card has its word ready to store, and all 16 cards store their words together. There is plenty of time in the 1.2μs to access the store for a write, and then a read operation before the 16 cards must store their next sample.

The store operation has been demultiplexed by 16.

## 3. ANALOGUE TO DIGITAL CONVERSION (A-D)

A 4-bit convertor is explained here to show how an 8-bit one could work.

### 3.1 4-bit A.D.C. - Level Sensing

The analogue input is sampled, and the voltage held on a capacitor. This forms one input to 16 slicers, whose other inputs come from progressively higher taps on a potential divider from a stable d.c. reference.

Normally, linear encoding is used and the voltage difference between taps is the same all the way up.

Those slicers biased below the sample voltage will go high - those above stay low. After a settling time (some slicers may change state faster than others when the i/p voltage changes) their logic outputs are latched.

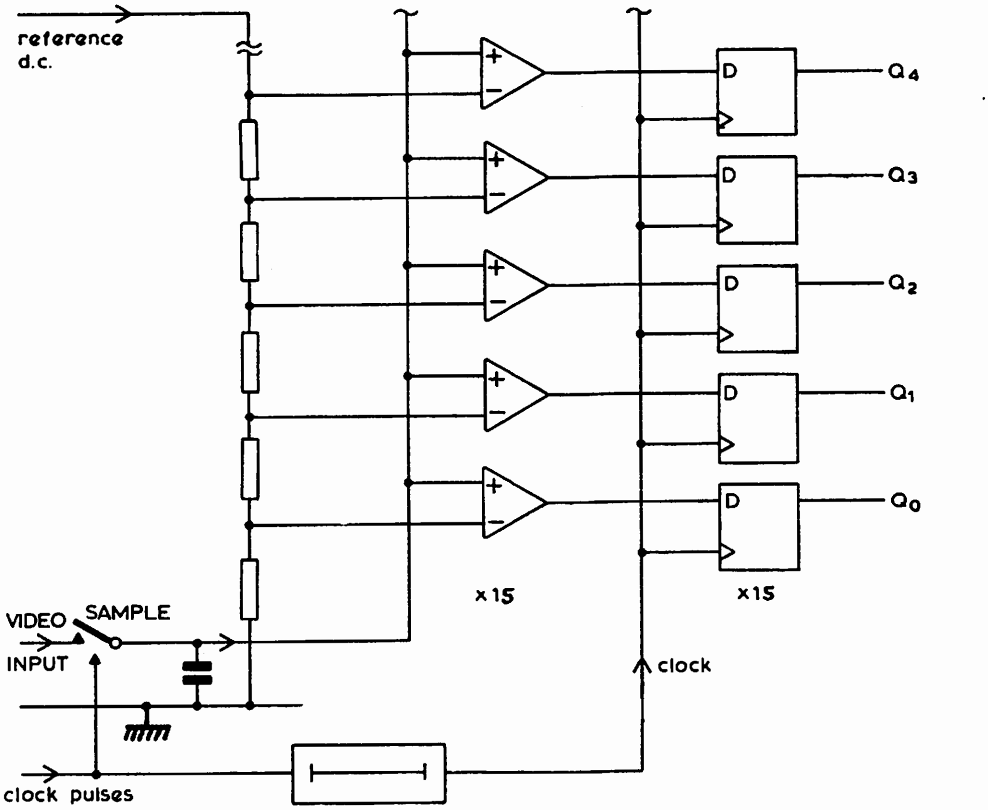



Figure 3.1: Sample Converted to 16 Logic State

There are 15 Q outputs, Q0 - Q14. All those corresponding to bias levels below the sample voltage hold logic 1, and those above logic 0. The actual signal voltage must lie between the two taps corresponding to the highest Q with a logic 1, and the Q above, which holds logic 0.

### 3.2 4-bit ADC. Assembling the output code

A priority encoder from 16-line to 4-lines is constructed using 'exclusive OR' gates.

(Remember, if the 2 i/ps are the same:- o/p = 0
2 i/ps different:- o/p = 1)

Only one of the 15 EX. OR gates outputs a logic 1, and this selects the desired 4-bit logic code, by virtue of its connections to the output summing or gates.

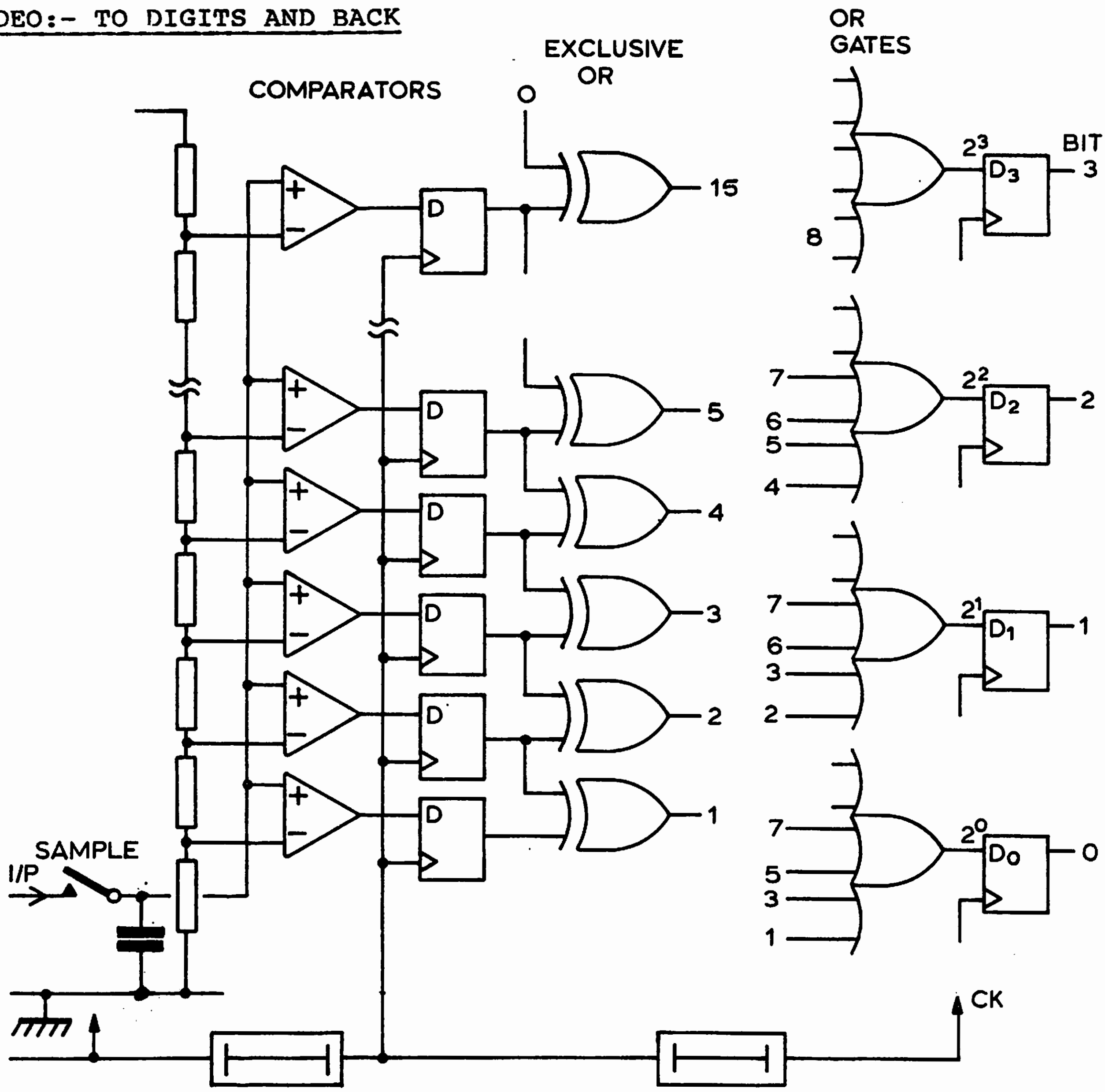



Figure 3.2: Complete 4-bit A-D Convertor

The output code is latched to hold it for one complete clock period, so that the gate settling period is never connected to the output.

This is called a 'One-look' A-D Convertor, to differentiate it from 'Successive Approximation' or 'Ramp and Counter' types; which are too slow for digital video.

## 3.3 Cascading two 4-bit A-Ds The two-look approach

Video is applied to a 4-bit A-D, which gives a 4-bit output corresponding to the level of the video sample to the nearest 16th of the video p-p range, V.

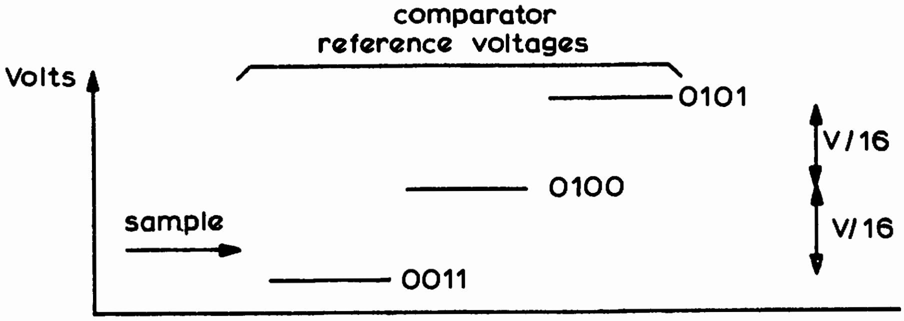



Figure 3.3: 4-bit ADC input and output

If the output is 0011, the sample lies in the range between 3/16 V and 4/16V.

To achieve 8-bit accuracy, the position of the sample within this range must be analysed to 1/16th of V/16.

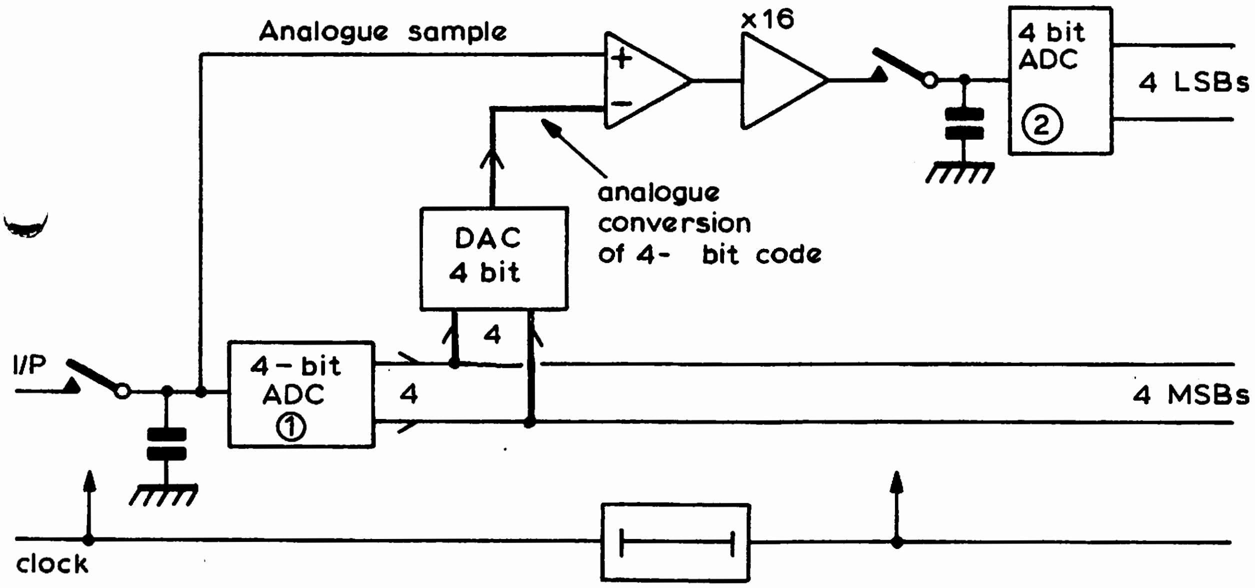


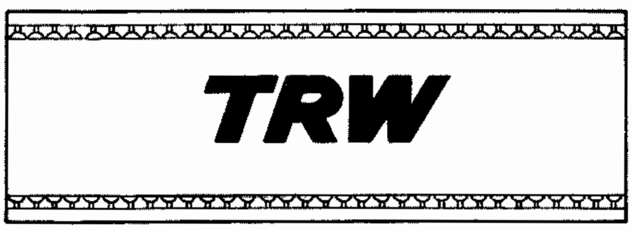

Figure 3.4: Two-look 8-bit A.D.C.

The first 4-bit ADC analyses to V/16 accuracy, with a positive analogue 'remainder'.

How much remains to be analysed? The 4-bits are converted back to analogue and this voltage subtracted from the original analogue sample. The remainder will be less than V/16. This is amplified, and analysed to give the 4 L.S.B.s by the second A.D.C.

## 3.4 One-look 8-bit A.D.C.

The TRW 10007 VJ 8-bit/integrated A.D.C.




Uses I.C. technology to generate an accurate 256-step bias ladder, with 256 comparators, latches, etc., which would have been prohibitive in discrete components. It has replaced a 2-look A.D.C. in discrete form, which occupied two large PC cards, and took much alignment time.

## 4. DIGITAL TO ANALOGUE CONVERSION

This presents little difficulty and can usually be done using an R + 2R ladder, often engineered in an MSI package.

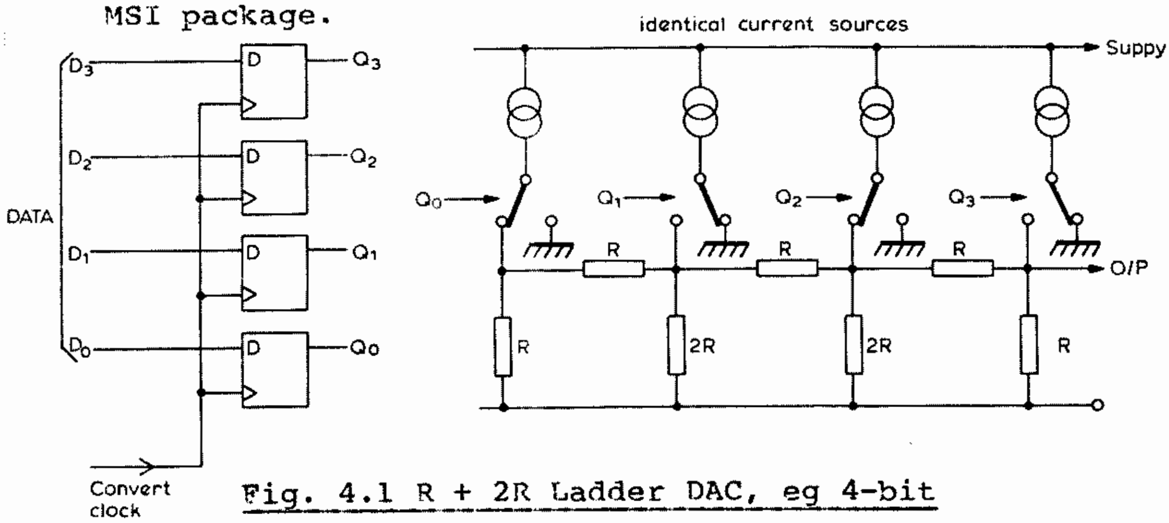



Fig. 4.1 R + 2R Ladder DAC, eg 4-bit

The new 8-bit input is latched into the D.A.C. The switches take up their new positions, and in doing so may cause transients as some switches close before others open.

The analogue output is re-sampled so that it does not get clocked through until the D.A.C. ladder output has settled.

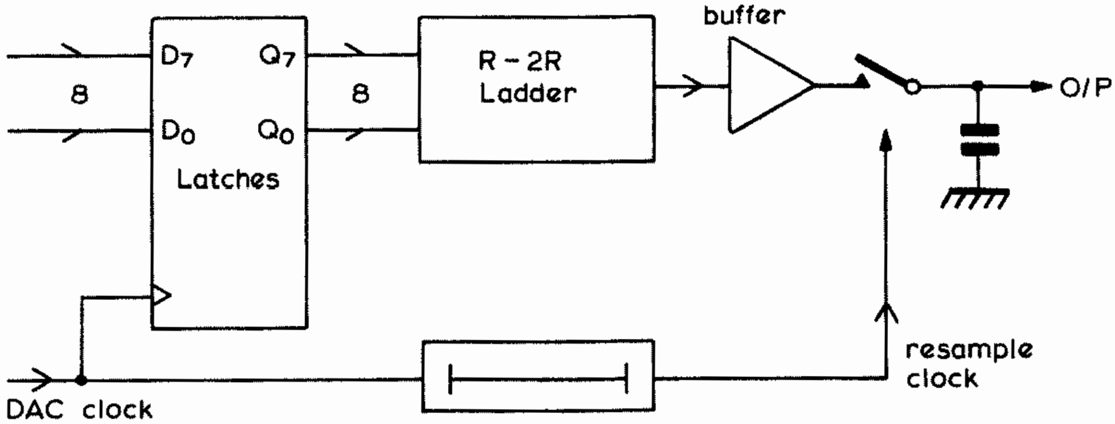



Figure 4.2: Analogue Re-sampling on the D.A.C. o/p

Fig. 4.3 gives a waveform representation of the effect of re-sampling.

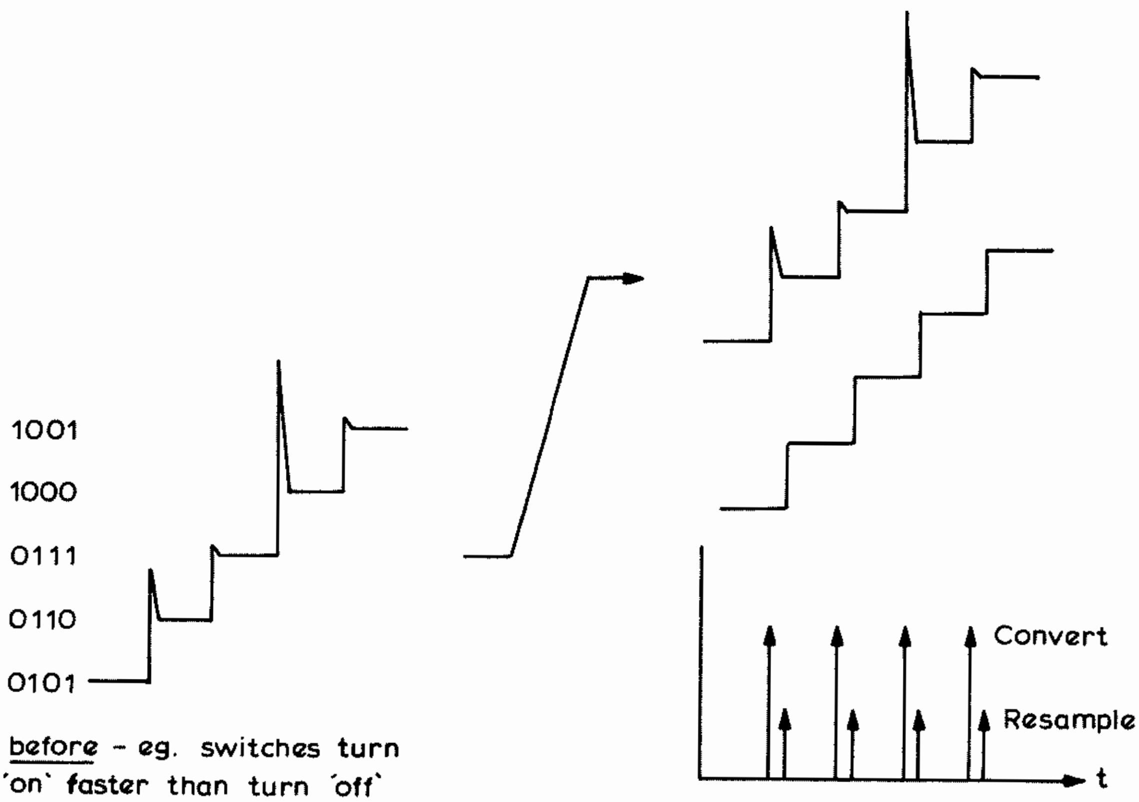



Figure 4.3: D.A.C. waveforms before and after re-sampling

The output has been re-timed but this is applied to the whole signal and is only about 1 extra latch's worth of delay.

## 4.1 h.f. loss due to sampling (Sinx/x)

The sample of the signal voltage is held between sample points. The stepped nature of the sampled signal gives rise to h.f. loss in the baseband signal recovered from the sampled spectrum. The loss curve has a $\frac{\sin x}{x}$ shape.

How does this loss arise?

Take one isolated sample of the input signal, and let it be of zero duration.

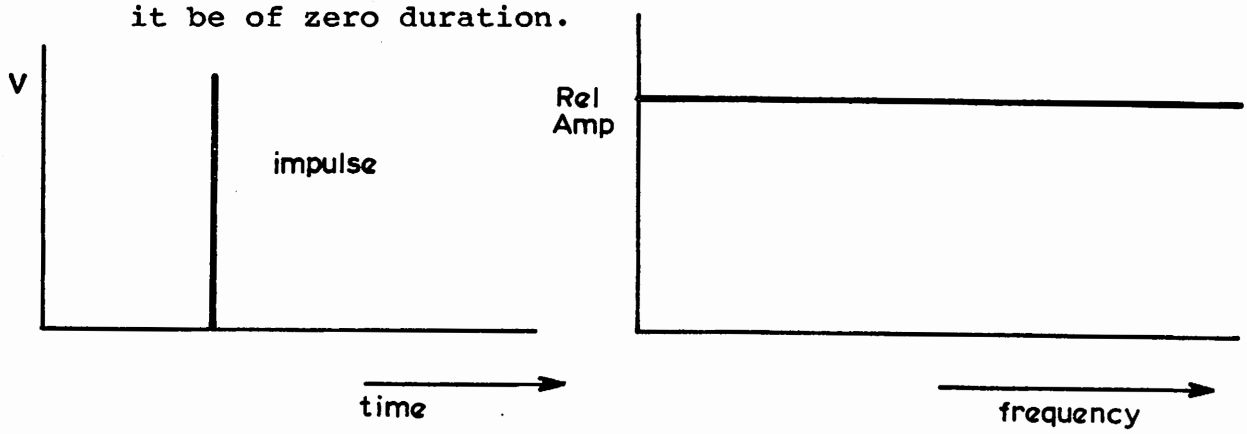



Figure 4.4: Time and Frequency Domain Plots of an Isolated Impulse

An impulse has equal amplitude components over the entire spectrum. In practice, the isolated sample will not be of zero duration, but will last for, say, a time $T_o$.

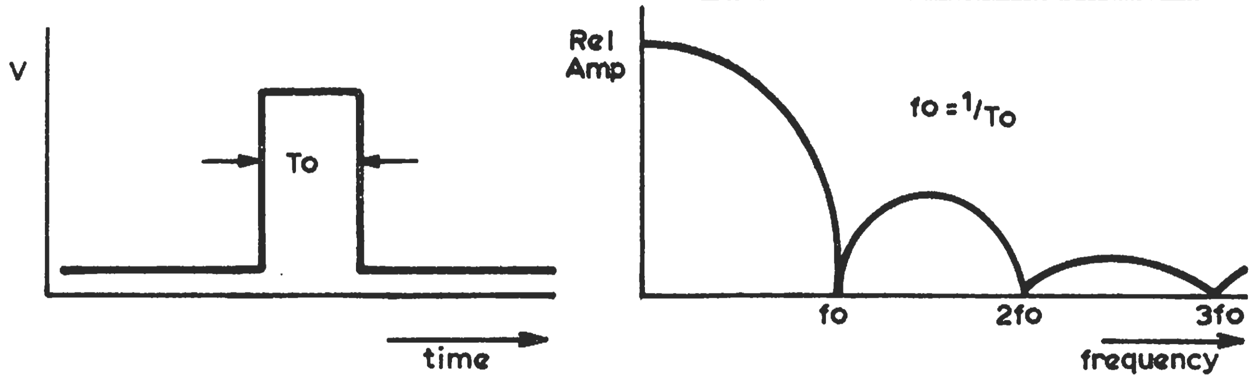



Figure 4.5: Time and Frequency Plots of an Isolated Pulse, Width $T_o$

The spectrum of the zero-duration impulse is modified to have extinction points, corresponding to frequencies which cannot be present in the waveform in figure 4.5. The rectangular shape would be impossible with components at f = 1/T, f = 2/T, f = 3/T, etc.

The shape of this curve is called $\frac{\text{Sin } x}{x}$, where

$x = \frac{\pi f}{fo}$ f is any chosen frequency - fo is 1/To

Now take a 1:1 square wave, which we know has components at fundamental and odd order harmonics, i.e. a spectrum of $1.\sin\omega t + 1/3 \sin 3\omega t + 1/5 \sin 5\omega t$

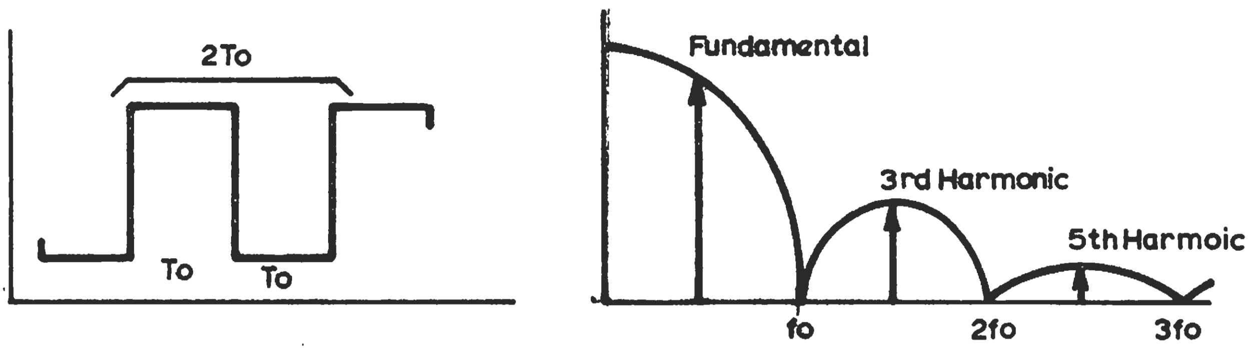



Figure 4.6: Time and frequency plots for 1:1 square wave, period 2To

The amplitude relationships of the component frequencies fit neatly into the envelope of the spectrum of an isolated To pulse.

Similarly, the component amplitude of the harmonics which make up a 2:1 square wave (figure 4.7) and a 3:1 (figure 4.8) are also shown against the $\frac{\sin x}{x}$ curve shape.

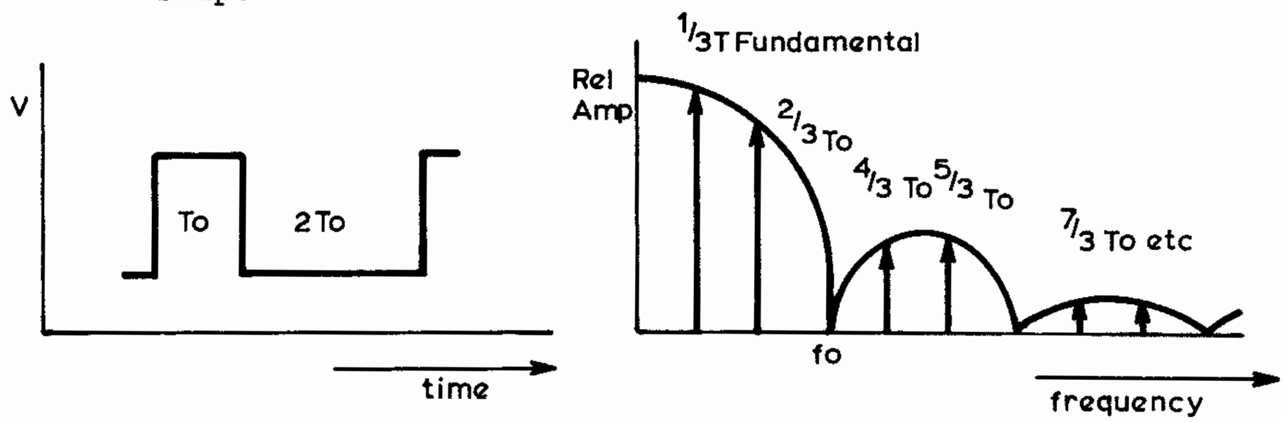



Figure 4.7: Waveform & Spectrum of 2:1 rectangular wave

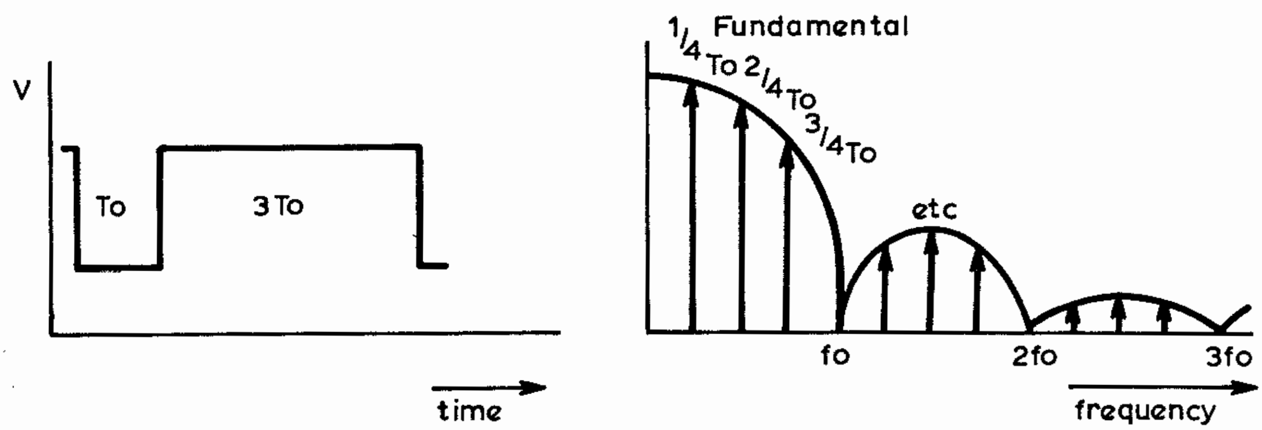



Figure 4.8: Waveform & Spectrum of 3:1 rectangular wave

The conclusion can be drawn that any rectangular waveform composed of multiples of the period To, will have component amplitudes which lie along the $\frac{\sin x}{x}$ curve for an extinction frequency $f_o = \frac{1}{To}$.

But now examine the D-A converter output of a digital video system. It can be considered to be the sum of various rectangular waveforms of multiples of the time period found from 1/Fs, i.e. the reciprocal of the sample frequency.

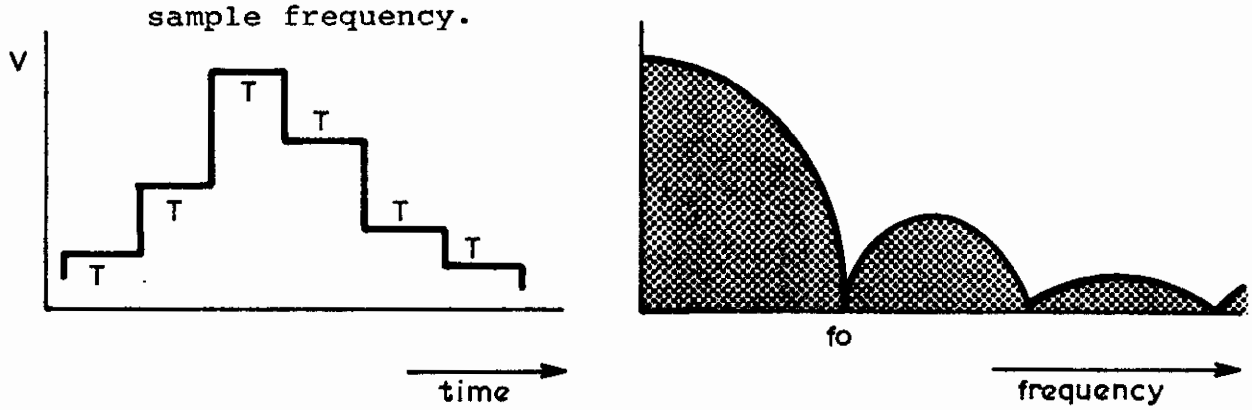



Figure 4.9: Waveform & Spectrum of sample and hold circuit output.

The video baseband signal always occupies less than half the sampling frequency of bandwidth.

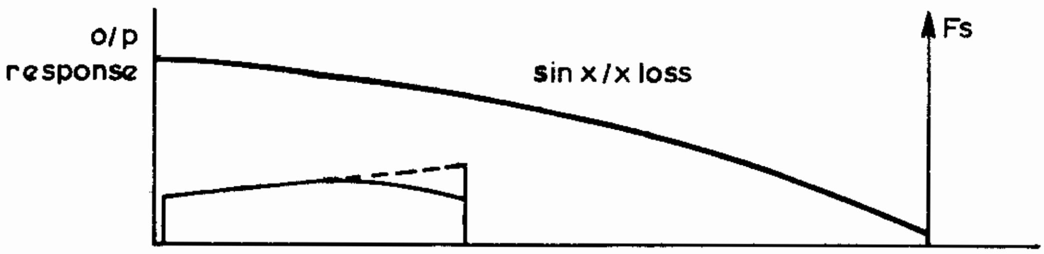



Figure 4.10: Effect of $\frac{\text{Sin } x}{x}$ sampling loss on the recovered video

Let us calculate the loss at 5.5MHz for 3 different sample frequencies.

a. Nyquist (12.1MHz)

b. 3 x CSC (13.3MHz)

c. 4 x CSC 17.7MHz

Output at 5.5MHz with respect to low freqiencies is

$$O/P = \frac{\sin \pi f/fo}{\pi f/fo}$$ Sampling freq

freq being sampled

For, a. Nyquist sampling O/P = 0.69 ≡ 3.2dB loss

b. 3 x CSC sampling O/P = 0.74 ≡ 2.5dB loss

c. 4 x CSC sampling O/P = 0.85 ≡ 1.4dB loss

This provides another incentive to raise the sampling frequency, as the highest video frequency will move up the $\frac{\text{Sin x}}{\text{x}}$ curve, needing less correction.

Equalisation for this loss is usually included in the final low-pass filter response.

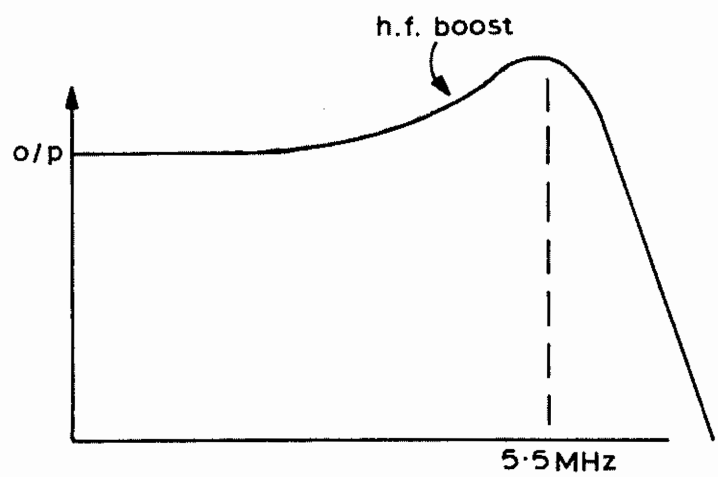



Figure 4.11: Final post-DAC low pass filter response

## 5. SUMMARY DIGITAL VIDEO

5.1 The video waveform is sampled and held at the sample frequency. This should be > 2.2 x the highest signal frequency for simple systems to avoid aliases. A low-pass filter must be used before sampling to prevent any spurious signal, higher than the highest signal frequency, from reaching the sampler, where it would also produce aliases.

5.2 A-D conversion must be very fast, requiring an accurate 'one-look' convertor. An 8-bit word is normally produced from each sample. Quantising noise arises from representing an infinitely variable analogue signal by, for 8-bit encoding, one of 256 fixed voltage levels.

5.3 D-A conversion is straight forward, but the settling time of the D.A.C. must be overcome by re-sampling the analogue D.A.C. output voltage.

5.4 A low-pass filter is used at the system output to remove sampling frequency and its harmonics, with their sidebands. It usually includes (sinx)/x correction for high frequency loss of the wanted signal during sampling.

5.5 The composite PAL signal may be sampled directly, or decoded to Y.U.and V components, which are individually sampled. U and V sample rates can be less than Y because of their smaller band width.

5.6 A typical composite PAL system uses 3Fsc sampling and 8-bit encoding.

5.7 A typical Y.U.V component system uses 13.5 MHz (864 x FLine) Y sampling, and 6.75 MHz for U and V. (Older designs may use lower U and V sampling rates).

12·1 MHz 5·5 MHz

P.J. Harris/MG/VC/VIDEO
21st September 1983