DYNAMIC RAMS AS VIDEO STORES

INTRODUCTION

Dynamic Random Access Memories (DRAMS) were developed as computer memories, but are now widely used to store video data.

This information sheet outlines some of their limitations and the precautions necessary if they are to be used for video storage.

1. CONSTRUCTION AND ORGANISATION

The memory cell in a Dynamic Ram is a small capacitor. These capacitors, together with the associated charging (writing) and reading crcuits are arranged in a matrix of rows and columns. Current devices have a capacity of 16k, 64k or 256k bits. The memory may be 1, 4 or 8 bits wide. e.g. a 64k device may be 64k x 1 bit or 16k x 4 bits.

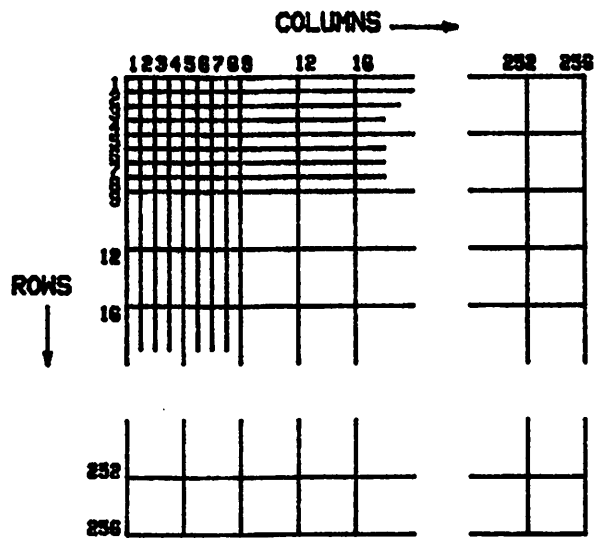

Figure 1.1 Organisation of 64k Dynamic RAMS

To access any paticular cell, the devices needs to receive the address of the row and the column containing that cell. The large memories used for video data employ address multiplexing. In this technique the Row and Column address are sent in turn over the same address lines. Two timed signals, usually active on the negative going edge, are sent to tell the memory which

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address is on the address lines. These are Row Address Strobe (RAS) and Column Address Strobe (CAS). A further signal, Write Enable (WE), instructs the chip to write, otherwise a read will talk place. In the absence of the RAS and CAS signals the device is in an isolated, tristate mode.

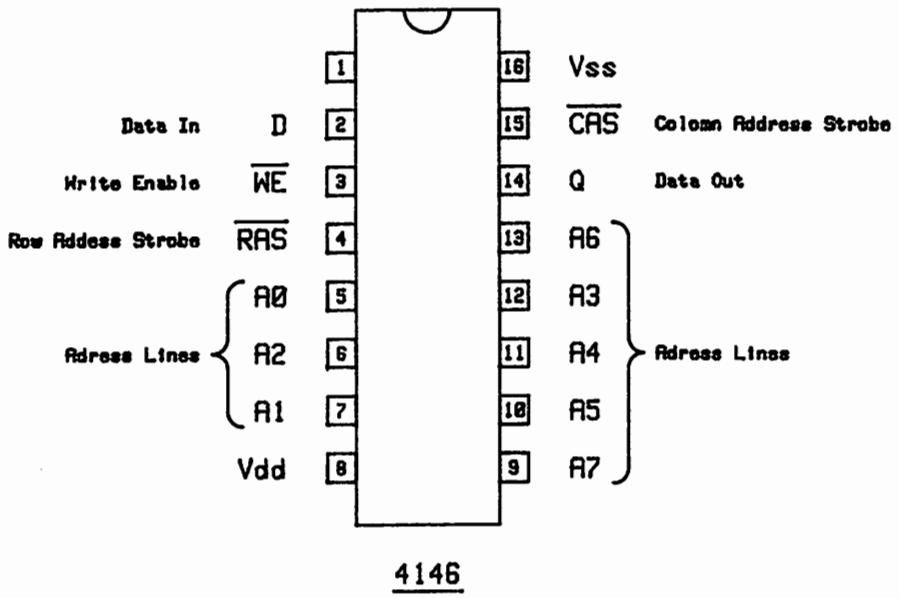

Fig. 1.2 Typical Pin out for 64k RAM

2. ACCESS AND CYCLE TIME

Setting up addresses, activating strobes and latching addresses into the memories takes time. Although only about 100 - 200nS, this time is long compared to the digital video period of 50 - 75nS. Furthermore the access time, usually quoted, is the time between the first address being set up and the data being reliably useable. The minimum time between successive complete access cycles is about twice the access time ie 200 - 400nS. Also the store is usually writing from the input and reading to the output continuously. Thus at least two cycles, and often more, must be allowed between each consecutive access.

The overall cycle time of a video store is at least four times the access time ie upwards of 400nS.

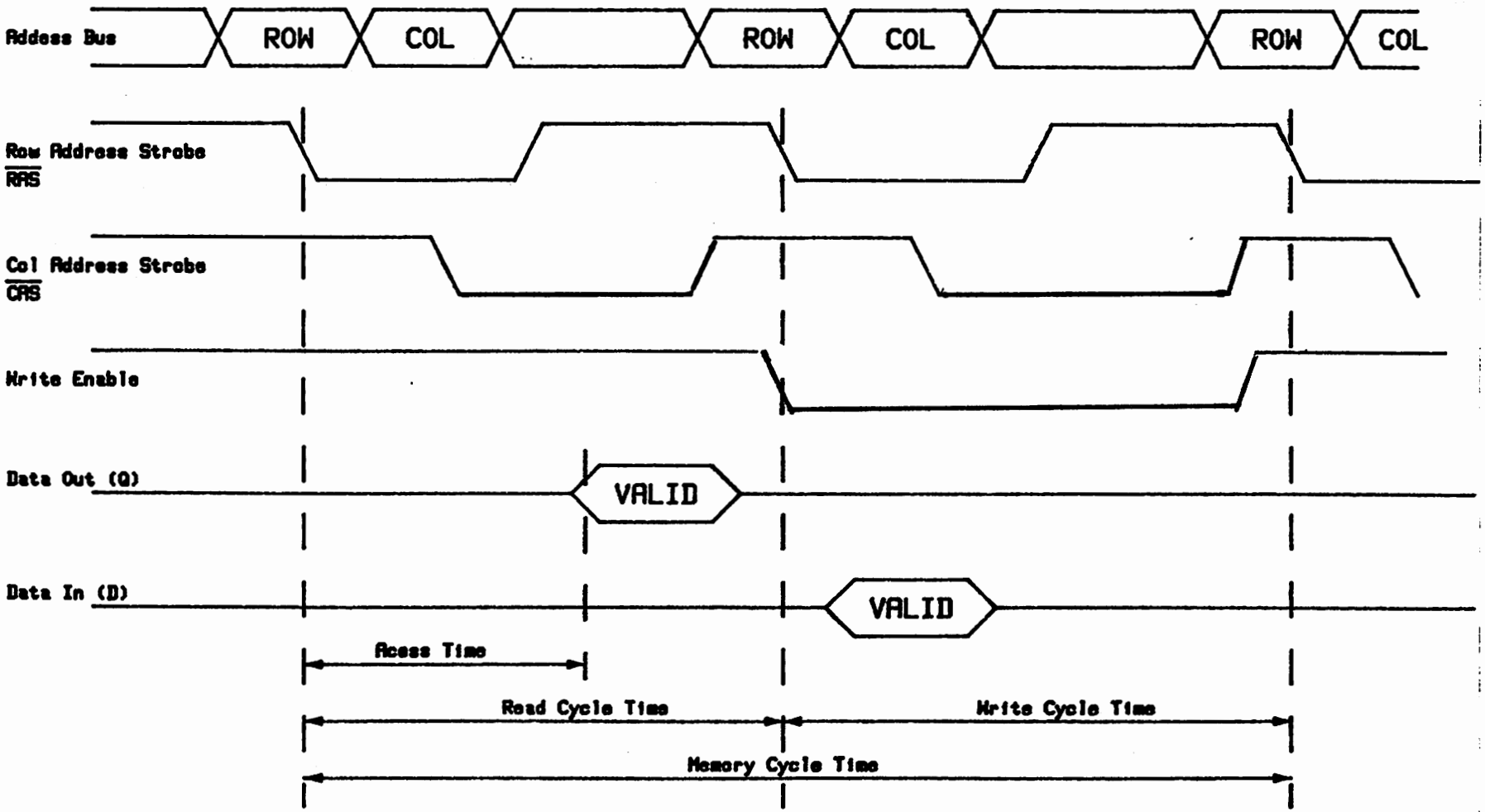

Fig. 2.1 Timings for Dynamic RAMS

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The problem of speed is solved by demultiplexing the video data. If one chip is too slow then several in parallel can be used. The data can be converted back to the higher speed at the output of the store. The demultiplexing and multiplexing can be done either by shift registers or by cycle clocking of a series of latches.

Demultiplex factors of 8 to 60 are used. The higher rates allow more than one read or write to take place in each memory cycle. This can be useful in digital video effects units with more than one input.

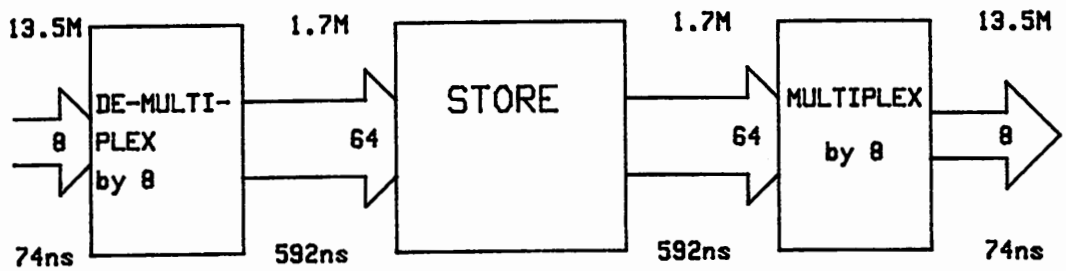


Fig. 2.2 Demultiplex and Multiplex of Video Data

2.1 Refresh

The capacitors which make up the storage cells will only hold their charge for a few milliseconds. They need to be frequency refreshed by over-writing each cell with its own contents. The chips are designed to do this automatically every time a RAS is received. This will refresh every cell in the row which is being addressed at the time.

In computers an automatic system ensures that every Row address is regularly set up even if no output is needed.

In a video store a separate system is not necessary as new data is always required to become the output video. The refresh can be made to be a by-product of the reading process.

3. ADDRESS ORGANISATION

The addresses for a video store are produced by address generators locked to the television line and field rates. Separate generators are required for the input and output: The details of these vary, but a typical example is given.

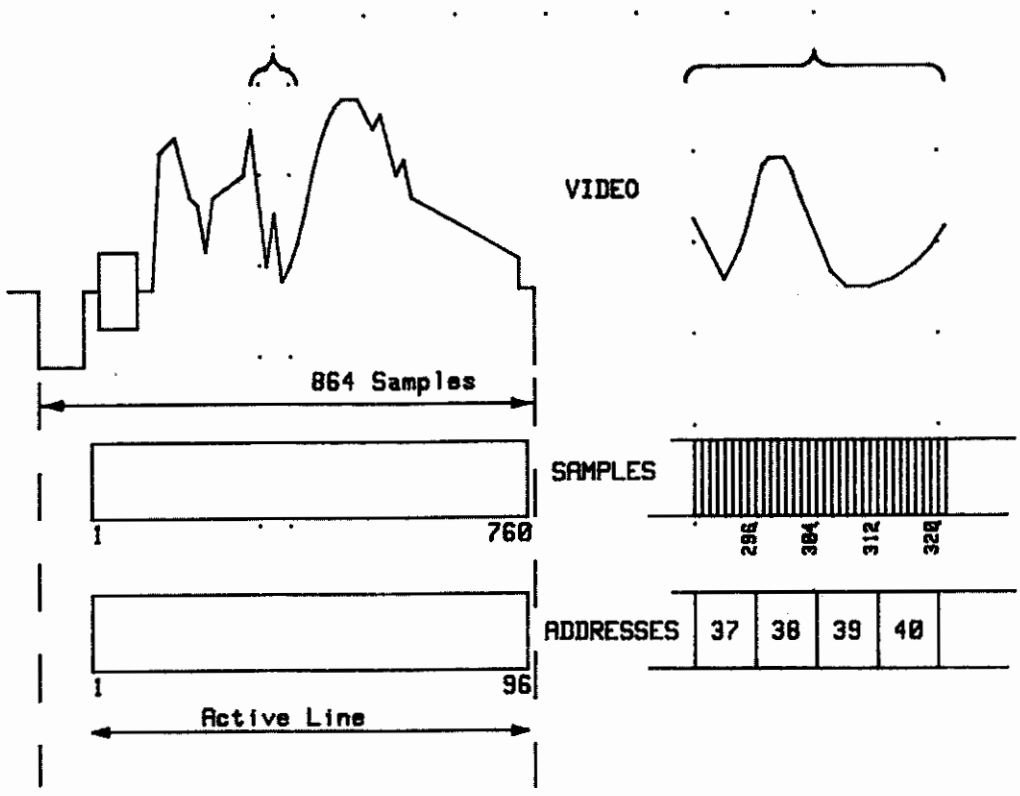
What Size of Chip?

Assume that an EBU digital signal will be stored. The memories will have an access time of 150nS. The memory cycle time will be at least 600nS.

The sample rate of 13.5MHz, has a sample period of 74nS, consequently the data will have to be demultiplexed by $\frac{600}{74}$, or about 8 times at least.

In each active line there are 720 samples, say 768 (3 x 256) for convenience. So in each active line the number of address locations needed will be $\frac{768}{8} = 96$.

Each address location will be used to store 8 x 8-bit samples, making 864 bits in all.



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A television frame of about 600 active lines so needs 600 x 96 = 57,600 separate addresses. These are provided in a 64k chip (which has 65,536 addresses).

How to Organise the Chips

Sixty four off 64k x 1 bit chips will store an active TV frame. The problem is now one of fitting the TV Structure of 600 x 96 addresses into the chip structure of 256 rows by 256 columns.

Two restrictions are:

a. The refresh should be automatic and,

b. The address generators should be as simple as possible.

An obvious first step is to split the chip into two fields. The MSB of the column address can be effectively odd and even fields. The automatic refresh requires the row address to cycle as often as possible, this must therefore correspondto the line structure, with the slower changing field information represented by columns.

The 300 x 96 addresses in each field now need to be fitted into 128 columns and 256 rows. This means about 2 2/3 lines per column. (1 line requires 96 rows).

Thus every row address in a column are used in 2 2/3 x 64μS = 170 μS which is easily fast enough for the refresh requirement.

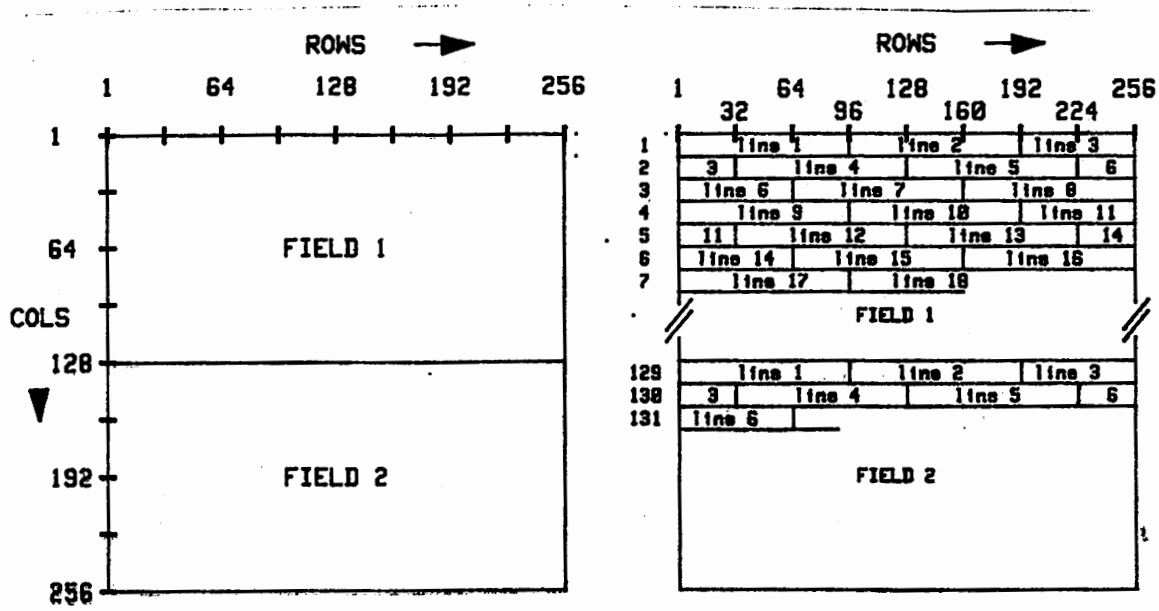

Fig. 3.2 Memory Map of 64K RAM used for Video

4. ADDRESS GENERATION

The details of the store organisation depends considerably on the ease of designing the address generators.

The sample clock is divided by 8, the multiplex rate, to give the address change clocks. This process is reset every line by a start of active line signal.

The address change clocks can be counted to generate the addresses for each line. This count is also stopped during non-active line and may restart from its previous end count rather than zero. That is line 1 may count from 1 - 96 whereas line 2 needs to start at 97 and count to 192 and so on. When 256 is reached the address count is reset to zero but the column address must be changed. In the example this happens part way through a line.

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The basic column address is determined by counting the lines. In the example, where 2 2/3 lines are stored in a column of memory a counter is needed which is effectively dividing by 8/3. This can be formed by decoding the simple line number count with logic or a PROM to give the necessary addresses. The part of the column address which comes from the row counter also has to be added on in an arithmetic unit.

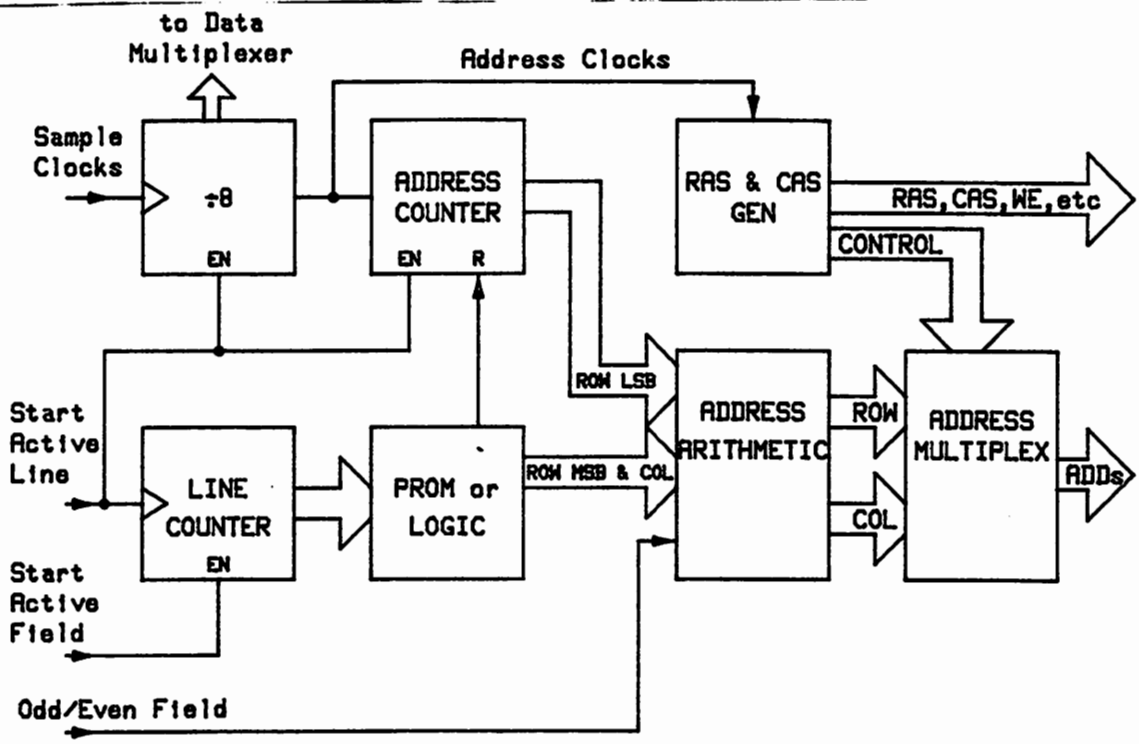

Figure 4.1: Address Generator Simplified

The Address change clocks are used to generate the RAS, CAS and WE signals and also to control the address multiplex switch.

In this way address generators can store the data at known addresses and automatically give refresh at the same time.

It is worth noting that the speed of the 64k chips presently available is just right for video. 256k x 1 bit chips would need to be 4 times faster, although 64k x 4 chips could be used if available.