SYNC PULSE GENERATION, PART II

You will have met the basic principles of sync pulse generation, probably working from Information Sheet 41F, on a previous course.

It is the aim of this Information Sheet to follow on from 41F, through a revision section, to a more detailed description of current S.P.G. techniques.

1. Revision

1.1 S.P.G. Techniques

The set-reset (S.R.) bistable is commonly used as the main building block to generate the output waveforms of the S.P.G. The set and reset inputs are supplied with trigger pulses, known as Edge Timing Pulses, which define the transitions in the bistable output waveforms.

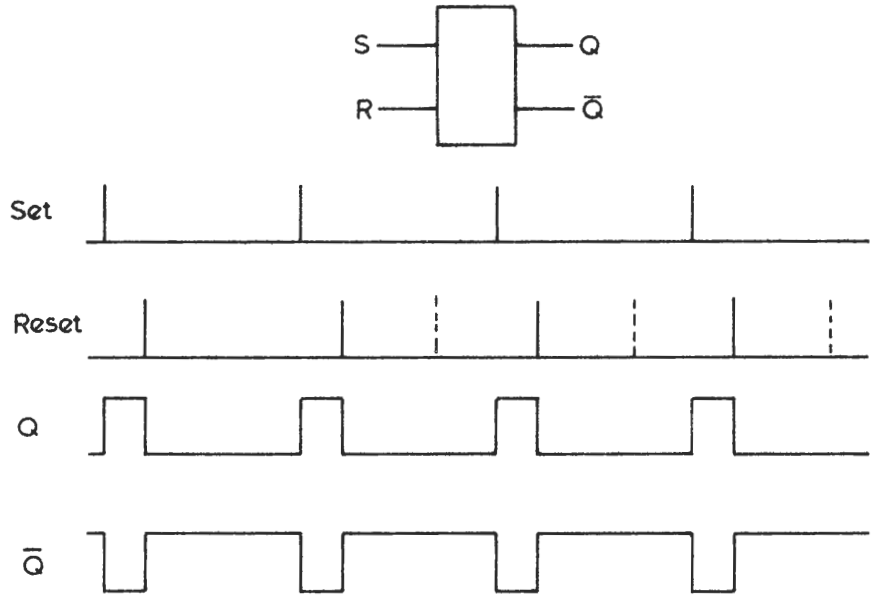

Fig. 1.1 Edge Timing Pulses fed to an SR Bistable

Remember that when a bistable has been triggered to a particular state, further trigger pulses to that input (shown dotted in Fig. 1.1) will have no effect until the other input has been pulsed.

The Edge Timing Generator produces a number of pulses suitable for defining the transitions on all the S.P.G. output waveforms.

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The Edge Timing Generator is clocked at Twice-Line Frequency, which is the highest repetition rate of pulse output waveforms from the S.P.G.

The twice-line frequency, 2H, is derived from a high-frequency crystal oscillator, from which subcarrier may also be generated. For example, the BBC uses 5MHz, which is an industrial frequency standard, as the master frequency. Other manufacturers may use a high multiple of line frequency, or a multiple of colour subcarrier frequency, as the master clock.

The use of a 2H edge timing clock would lead to all the S.P.G. outputs being generated at this rate. To produce lower frequency waveforms, at H and V rate, edge timing pulses must be inhibited from reaching the bistable set and reset inputs except at the required frequency. The 2H clock is divided by 2, to give a line-rate inhibit waveform, and by 625 to give field-rate inhibit waveforms.
Some S.P.G. outputs require a combination of inhibit waveforms at these two rates. The combined inhibit is then used to control the passage of edge timing pulses to the output bistables. All this is done by the inhibit gating.

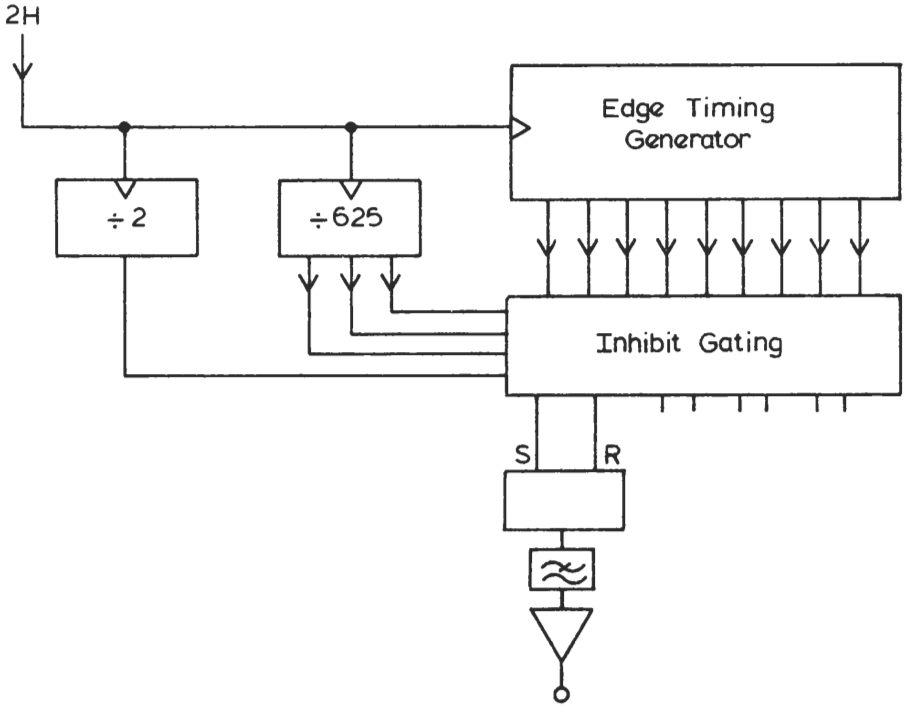

Fig. 1.2 Basic Block Schematic S.P.G.

The output amplifiers produce the standard voltage and impedance conditions for synchronising pulses from the logic level bistable outputs (e.g. 2V into 7SR). The rise-times are controlled to the required specifications by the output filters.

1.2 Basic Logic Techniques

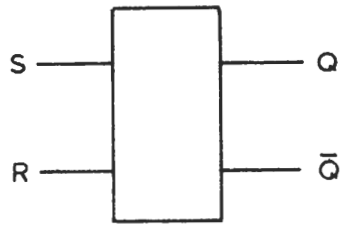

Fig 1.3 SR Bistable

The state-triggered S-R bistable, (using +ve logic,) is triggered to a logic '1' on the Q, by a logic '1' pulse on set; and to a logic '0' on Q by a logic '1' pulse on reset. Alternatively, the bistable may require low-active inputs, as in Fig. 1.4.1.

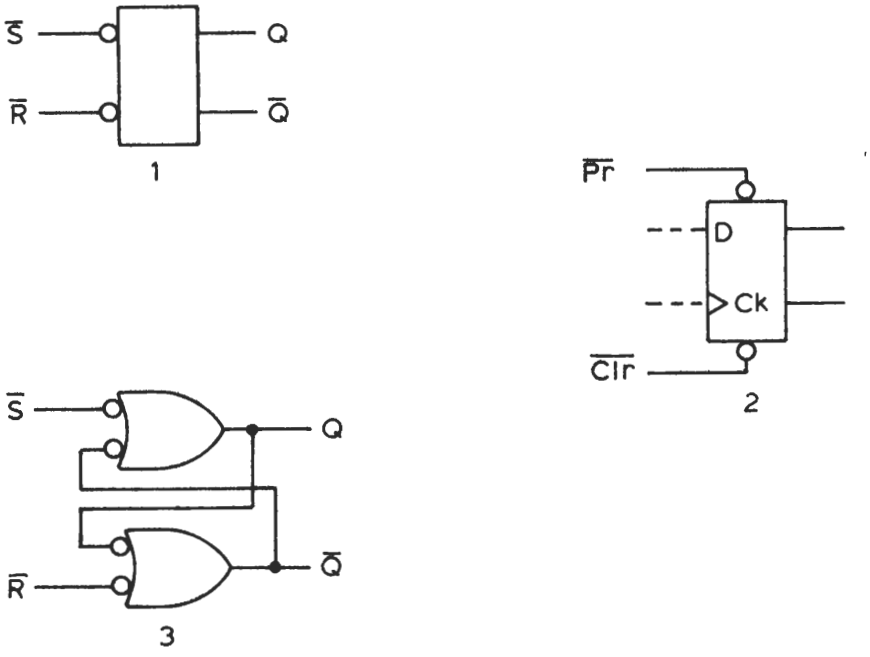

Fig 1.4 S-R Bistable Hardware Options

SYNC PULSE GENERATION, PART II

In practice, the preset and clear inputs of a D-type bistable could be used, as in 1.4.2, shown with low-active inputs.

A pair of cross-coupled NAND gates, drawn functionally in Fig. 1.4.2, can also be used to form a simple S-R bistable.

In some uses the bistable may be required to take a single input, and divide by 2. (Sometimes called a toggle circuit).

Fig 1.5 D type and J-K as ÷ 2

In both cases, the output changes state when a 0-1 transition occurs on the clock i/p. The J and K inputs of fig. 1.5.1 can be used to control whether the circuit toggles or not, when this is necessary.

2. EDGE TIMING GENERATOR

Revision

The edge timing generator is triggered at twice-line rate, producing on its output wires a selection of pulses whose relative timing corresponds to the relative timing of all possible transitions in the S.P.G. output waveforms.

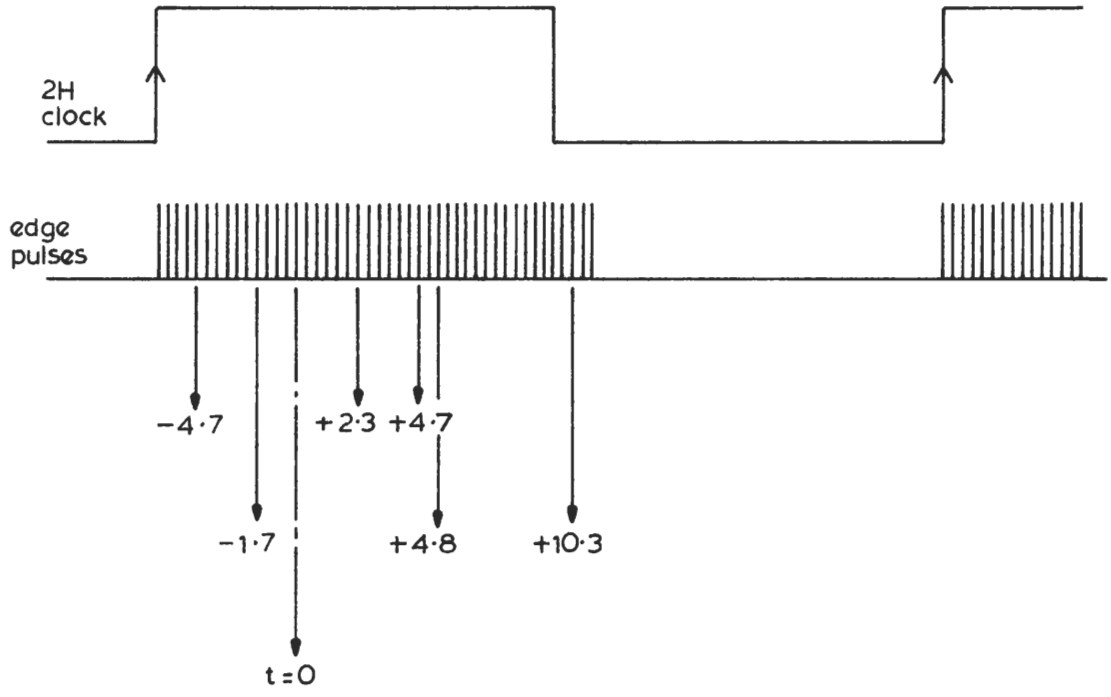

Fig 2.1 Selection of Output Timing of Edge Timing Pulses

Accurate edge timing can be achieved using a delay line, either passive or active; or by a counter with gating.

2.1 Passive Delay Line with Recirculation, BBC S.P.G

From the earliest to latest edge timing pulse is an interval of about 16μs, which would be expensive and bulky using only passive delays.

The BBC design uses 4 off, 1μs delay-lines in series. A pulse is fired down the delay lines by the active edge of twice-line, and re-circulated four times to give a 20μs period when edge timing pulses are being produced.

SYNC PULSE GENERATION, PART II

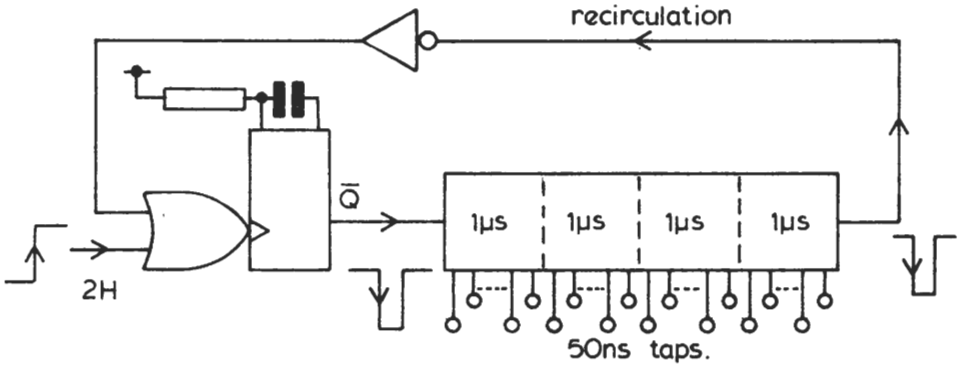

Fig 2.2 Delay Line, showing Simple Re-circulation

Figure 2.2 shows that, since the pulse is regenerated on each pass by the monostable, there "is no way of stopping it"! A counter must be used to stop the re-circulation until the next active edge of the 2H clock. Notice that a low-active pulse is sent along the delay-line, simply for ease in realising the design with the hardware then available.

The counting of the number of recirculations is performed by a shift register. The Qo is loaded with logic 0 by the input edge of the twice-line clock, at the same time as the first pulse is launched into the delays. All other shift-register outputs are high. (see Fig. 2.3).

The recirculated output pulse, 4µs later, clocks this 'low' along the shift register to Q1, and loads '1' into Qo. Each successive recirculation clocks the 'low' further along the shift-register until the sixth output, Q5, goes active low. This blocks the recirculation and clears the delay line ready for the next 2H active edge.

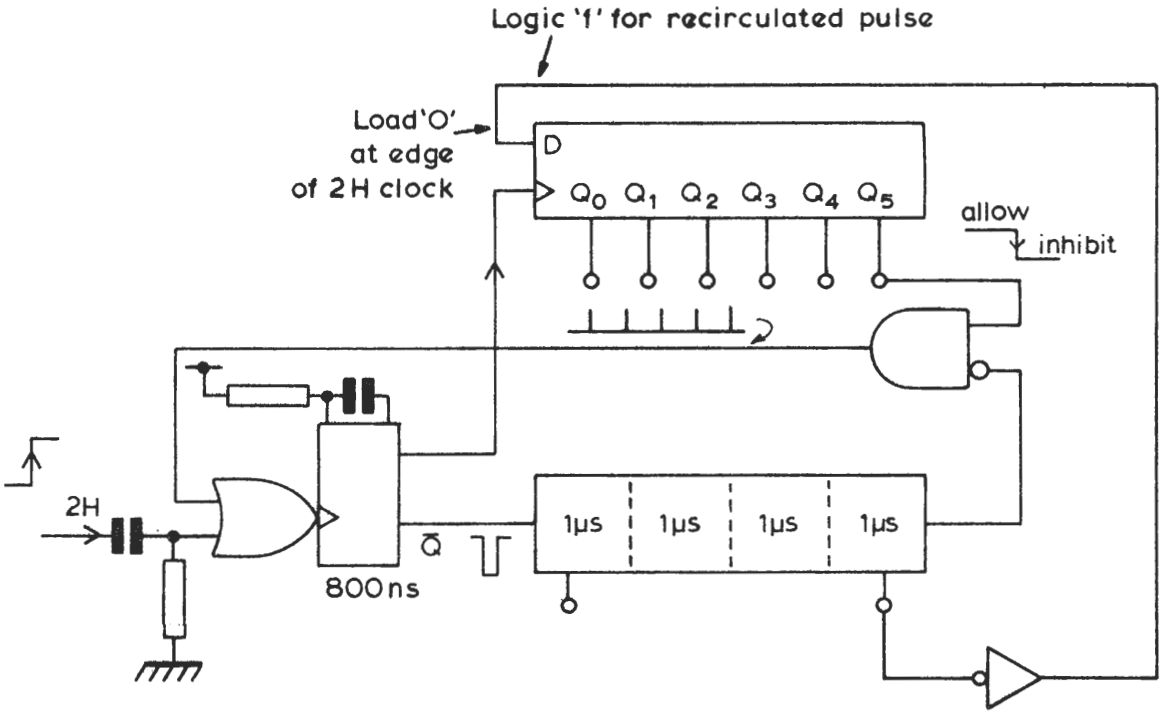

Fig 2.3 D.D. Edge Timing Generator

A low on Qo indicates 0-3µs after the 2H input, on Q1, 4-7µs, on Q2 8-11µs etc.
Each edge timing pulse is selected by gating the required tap and the appropriate Q output e.g. for 8.5µs: - Q2 is active, and the tap midway along the first delay is required.
As both these signals are low-active, the combining is therefore implemented with a NOR gate.

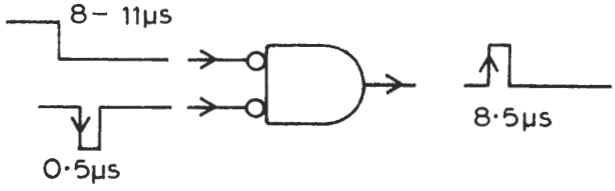

Fig. 2.4 Edge Timing Pulse at 8.5 µs after clock

SYNC PULSE GENERATION, PART II

The final edge timing pulse will be used as a set trigger, via the necessary inhibit gating, for line sync leading edge. All other edge timing pulses are generated similarly.

2.2 Active Delay Line

The Link 250 sync pulse generator aims to produce pulse timings within System I spec, which has a tolerance of ± 0.1μs on most pulse widths. Edge timing pulses within this accuracy can be formed using a deloy line tapped in 800 ns intervals.

e.g. 6 x 800 ns = 4.8μs (4.7 + 0.1μs) L.S.T.E.
2 x 800 ns = 1.6μs (-1.7 - 0.1μs) L.D.L.E.
13x 800 ns = 10.4μs (line blanking T.E.)

Instead of a lumped L-C (passive) deloy line, a shift-register clocked Ω every 800ns is used.

A 2.53 MHz (162 x F Line) clock signal is generated, during production of a correctly-related colour subcarrier on other cards in the S.P.G. This divides by 81 to give twice-line and by 2 to give a 1.26 MHz clock for the shift register (period of 790ns).
The active edge of twice-line enables the next 1.26 MHz clock to load a logic '1' into the shift register's Qo output (labelled A by Link). When the load has been successful,
the load circuit is cleared logic to '0' until the next 2H edge.

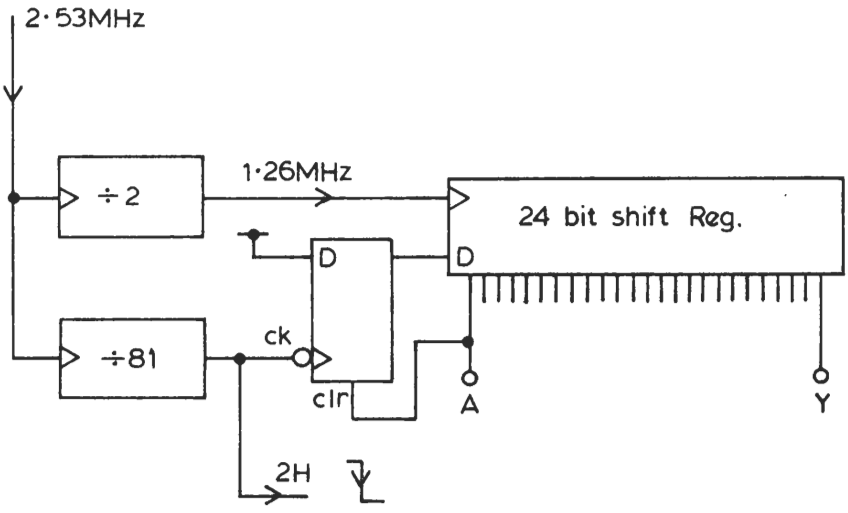

Fig. 2.5 24 bit shift register used as active delay

Each successive 1.26MHz clock pulse, 790ns apart, clocks this '1' along the 24 outputs of the shift-register. Tap H is used as the line sync LE trigger, and figure 2.6 shows the timing of all other required edge timing pulses.

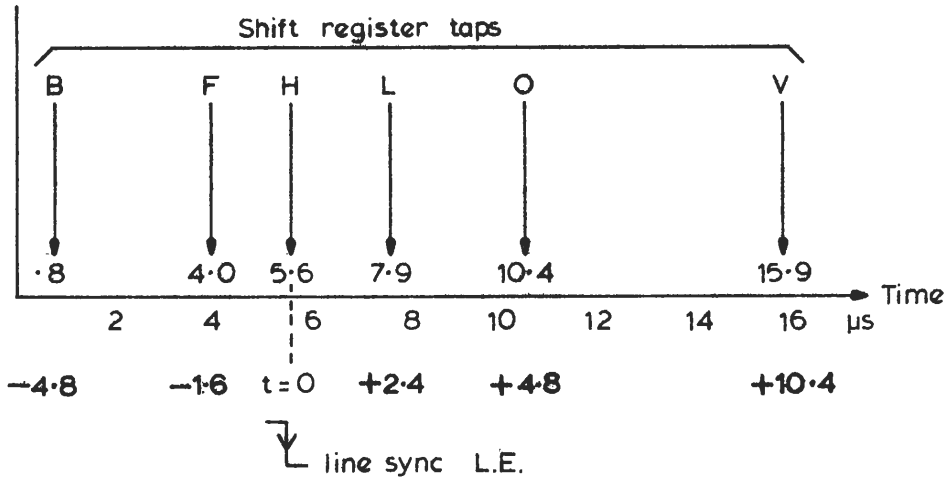

Fig. 2.6 Edge Timing Outputs from Link 250 S.P.G.

2.3 Counter and Gating

A high frequency stable oscillator is divided down to twice-line frequency by a counter. The counter Q outputs, and their inverse ($\overline{Q}$) waveforms, are taken to gates. Each of the gates is then able to select one of the input clock periods from the complete counter cycle. (See 41F, section 6.4).

In the Selteck S.P.G. - 110P, the hf clock is at 3.55 MHz, (227 x FH) which has a period of 280ns. The clock waveform is a 1:1 square wave, and by making this and its inverse available to the gating, either the first or last part of each 280ns period can be chosen, giving edge timing selection to 140ns accuracy.

An 8 bit synchronous counter is used to divide the 3.55MHz clock by 113. Each time the carry appears on TC of IC5, the counter is Parallel Loaded to count 143 by the next clocks pulse, which then deactivates TC and allows the count to proceed to 255 again.

SYNC PULSE GENERATION, PART II

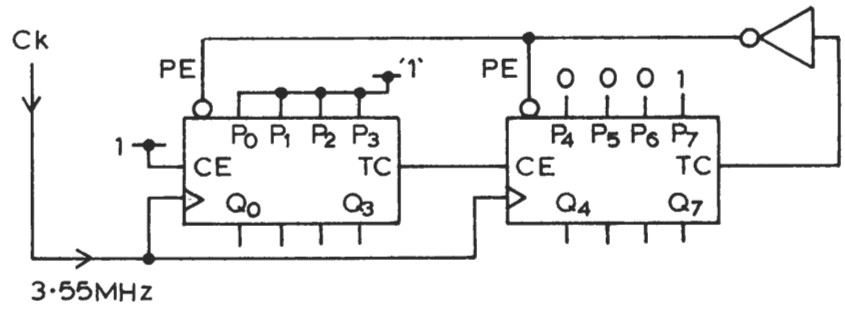

Fig. 2.7 Presetable Counter for ÷ by 113

In fig. 2.7 data on the Parallel inputs Po - P3 of each IC is enabled by the parallel enable at the count 255. It is entered into the counter by the next clock edge, and the parallel enable is de-activated allowing the count to proceed.

Each time the counter reaches 'end of count', the clock phase is inverted, to insert an extra half clock period into the next count, giving a division ratio of 113.5.

The Q outputs of the two ÷ 16 sections in fig. 2.7 are taken to gating, to generate Edge Timing Pulses. For example, line sync leading edge is taken by gating:

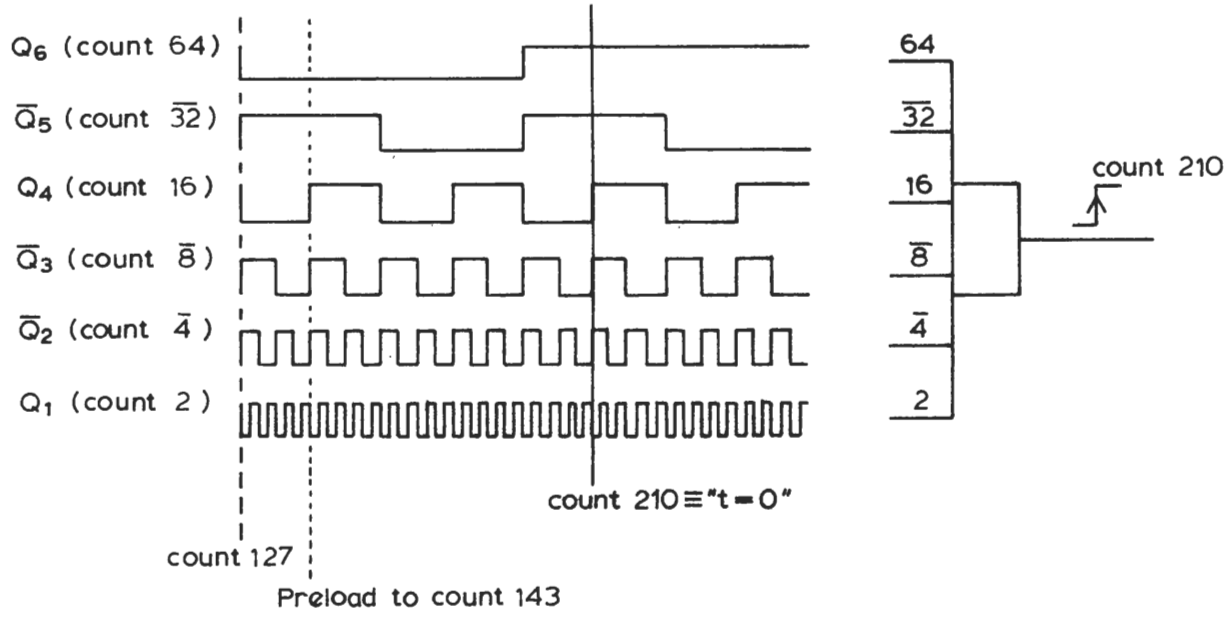

Fig. 2.8 Selteck 110, Edge Timing of L.S.L.E.

INHIBIT GATING

All the edge timing generators described produce edge timing pulses at twice-line rate, which would produce all output waveforms at twice-line. Inhibit gates are therefore put in the path of each edge timing pulse.

The inhibit gates are opened and closed by line and field rate inhibit waveforms, to reduce the repetition rate of the Edge Timing Pulses to the bistables.
They act rather like points on a railway network, they dont affect the timing of the trains (O/P edges), but they do affect whether they go to a chosen place or not! Similarly, the timing of the points operation is not critical as long as it's a little before the train is due!

3.1 Line Drive

The simplest of all waveforms, line drive, requires its leading edge trigger to occur once per line.

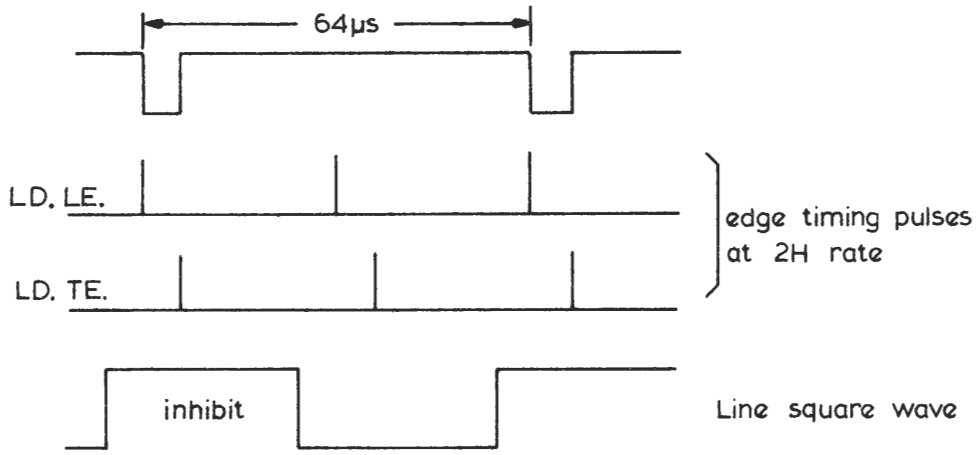

Fig. 3.1 Line Drive Generation - Waveforms

The inhibit waveform unblocks an 'And' gate, once per line, in the L.E. trigger feed to the output bistable.

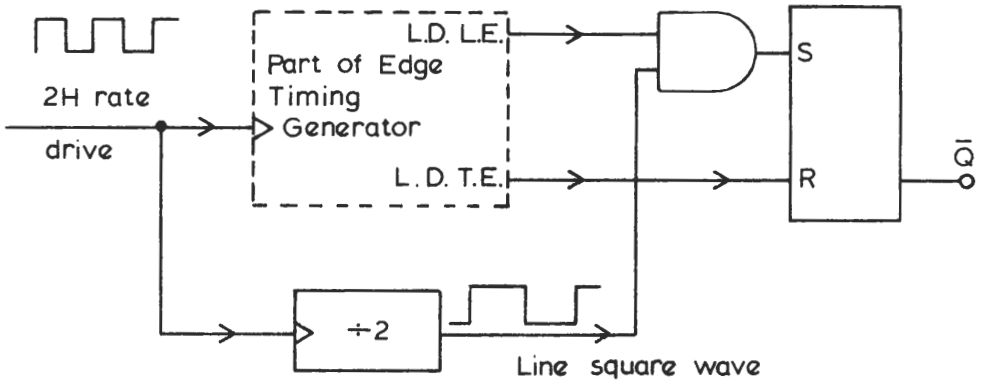

Fig. 3.2 Inhibit gating for Line Drive

3.2 Mixed Syncs

Mixed syncs is a basically line-rate signal, similar to line drive, for most of the field except for a period of seven and a half lines during the field interval.

In the field interval, output pulses are generated every 32 μs for this period of seven and a half lines. The first five intervals contain equalising pulses 2.3 μs long; the next five contain broad pulses, 27.3 μs long; and the last five contain equalising pulses again, all with leading edge at t = 0 and t = +32μs.

Mixed Sync Leading Edge pulses occur normally at 2.LF from the Edge Timing Generator, and for most of the field every other one is inhibited by the line square wave. A seven and a half line long pulse is used to remove this inhibit to give the twice-line rate L.E. triggers, once per field.

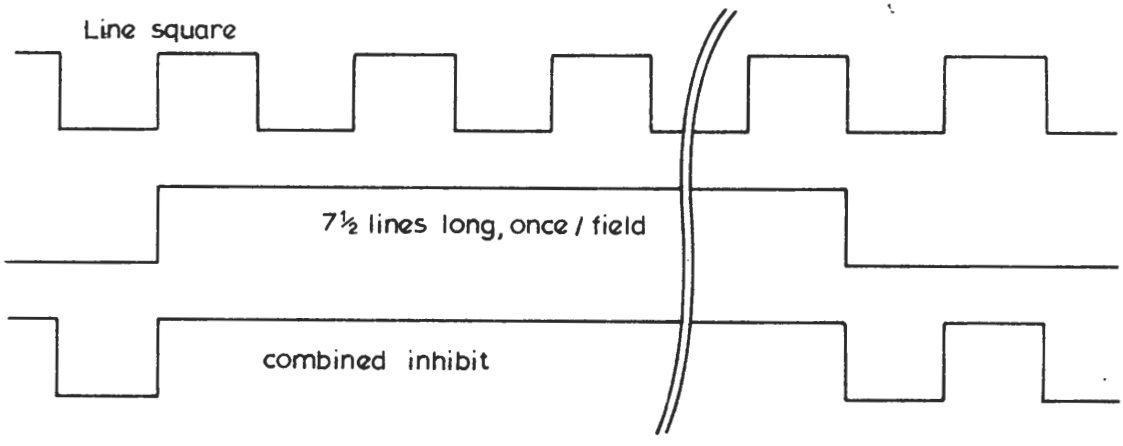

Fig. 3.3 M.S. Leading Edge Inhibit Generation

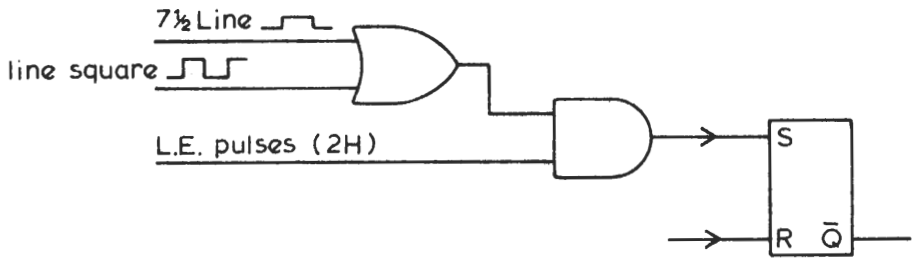

Fig. 3.4 Hardware for M.S. L.E. Inhibit

The OR gate is used to form the combined inhibit waveform to control the set triggers to the bistable.

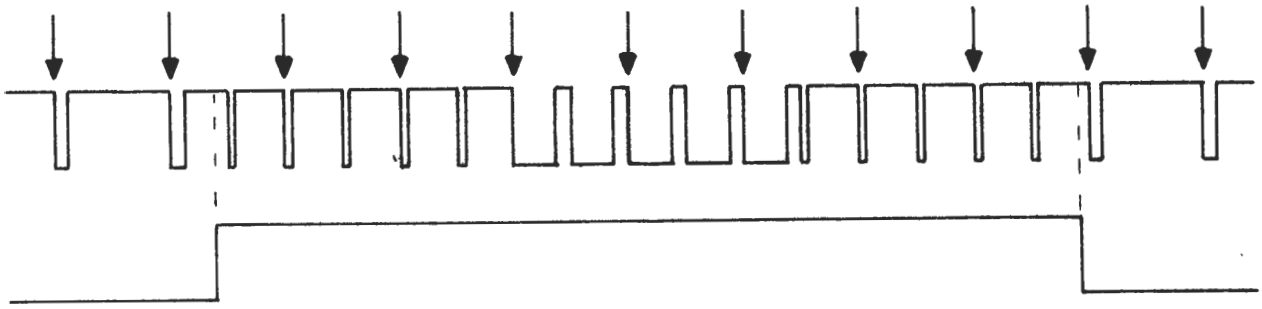

Fig. 3.5 Mixed Syncs; - Field Sync Period,
Shown Relative to the Seven and a Half Line w/f

The trailing edges will be at +4.7μs for most of the field, except during the field sync period.

Line sync trailing edges allowed except when seven and a half line waveform present. Seven and a half line is inverted and used to inhibit line sync trailing edge triggers for this period.

SYNC PULSE GENERATION, PART II

Equalising pulse trailing edges must be produced for two and a half lines, stopped for the next two and a half lines to allow 5 broad pulses, and then produced for a further two and a half lines.

Broad pulses trailing edges are the latest timing pulse required for mixed syncs, at +27.3μs (and +59.3). These edge timing pulses do not need inhibiting, since an earlier pulse will reset the bistable, except where broad pulses are required.

The generation of mixed syncs using typical functional blocks is shown below.

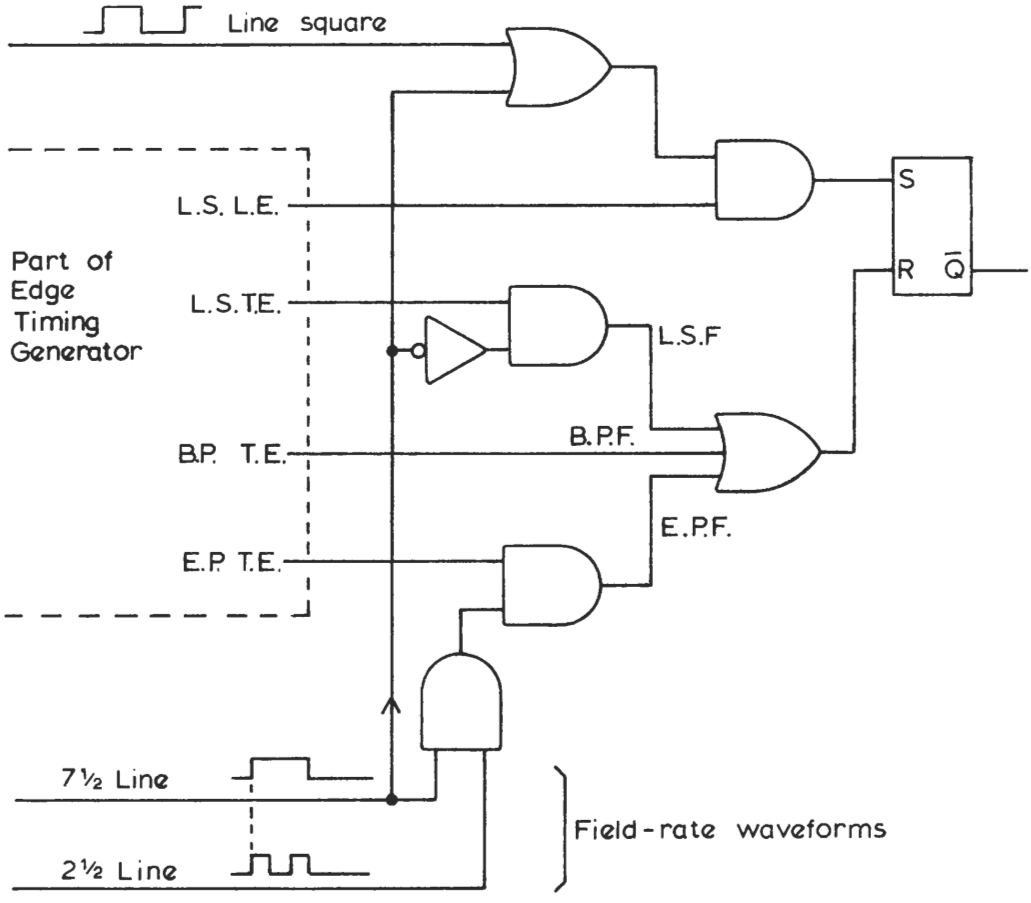

Fig. 3.6 Mixed Sync Generation, showing line and field rate Inhibit

3.3 Field Drive

Field drive starts coincident with blanking ie before the first equalising pulse. The trailing edge timing is not needed to any critical accuracy.

A suitable circuit might be as in Fig. 3.7.

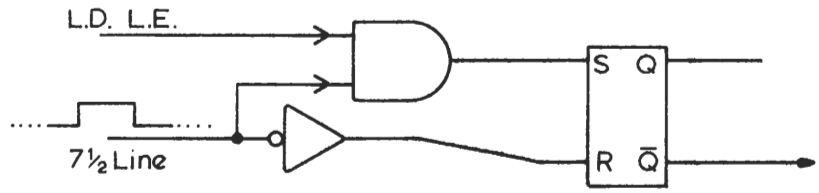

Fig. 3.7 Field Drive O/P

3.4 Mixed Blanking

A simple line rate pulse is required for most of the field. It starts coincident with line drive, t = - 1.7, and ends 12 μs later at t = +10.3. Note that the same L.E. pulse as line drive may be used.

Field Blanking must stay active for 25 lines each field and start just before the first equalising pulse on each field. Every other field the first equalising pulse occurs half way through a line, so that the line-rate Leading Edge inhibit must be removed to give the correct field blanking start time.

In addition, the Trailing Edge pulses must be blocked for a period of 25 lines, requiring an extra waveform from the field divider.

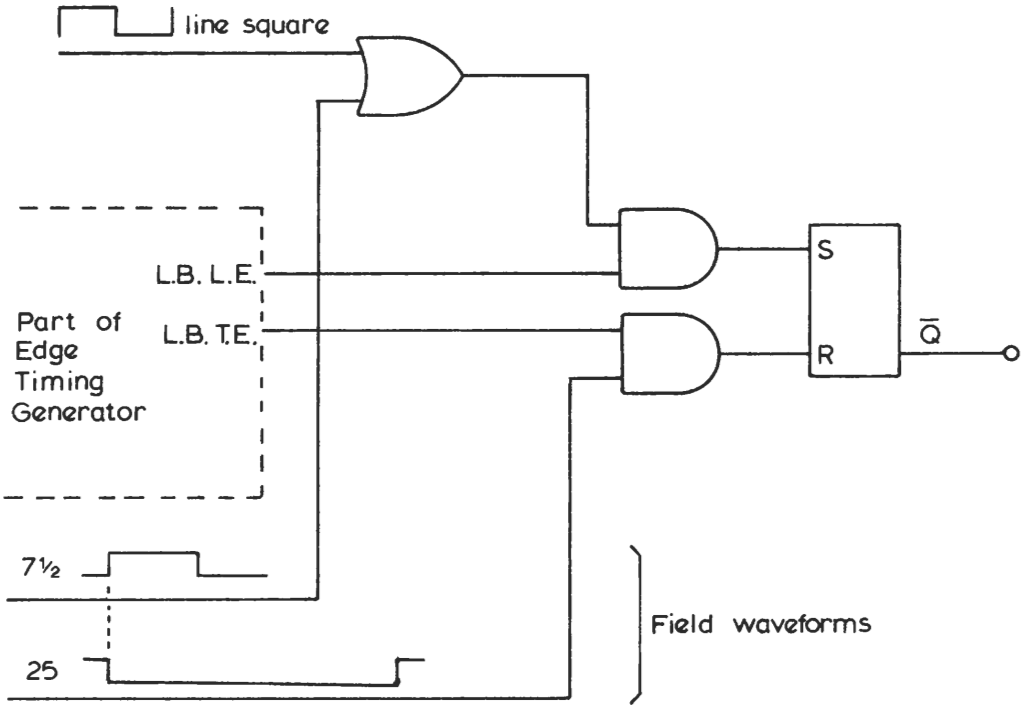

Fig. 3.8 Mixed Blanking - Typical Schematic

4. Field Divider

The field divider must divide twice-line frequency to field frequency, and give out the two-and-a-half line, seven-and-a-half line and twenty five line inhibit waveforms at field rate.

4.1 Simple Field Divider

Four ÷5 stages can be cascaded to give ÷ 625. Each ÷5 uses gated reset applied to a 3 stage binary up-counter.

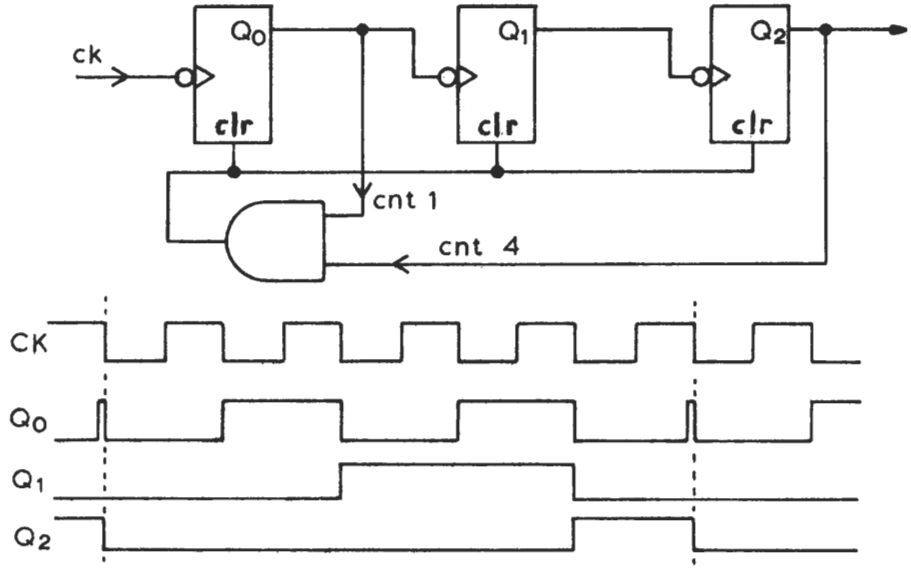

Fig. 4.1 Divide by 5 Counter and Waveforms

At the fourth count after the divider is cleared, Q2 goes high. At the fifth count Qo goes high momentarily, and gated with Q2 produces a 'clear' to all bistables.
Cascading 4 of these stages produces ÷625.

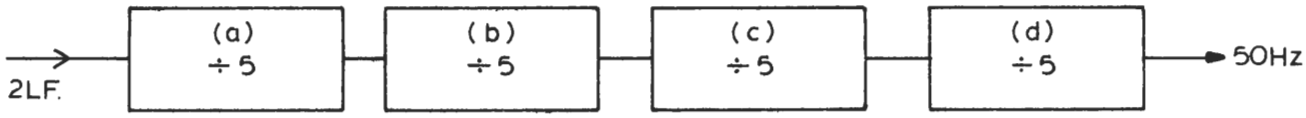

Fig. 4.2 Field Divider using ÷5 Stages

The output of stage a has a two and a half line period. The first bistable of counter b therefore produces the inverse of the two and a half line waveform, ie two and a half lines down, two and a half up, two and a half down, needed for mixed sync equalising pulse inhibiting. From counter b, gating of bistable 1 and bistable 2 can produce a seven and a half line (two and a half + five) waveform.
The output of counter b has a period of 2LF/25, ie twelve and a half lines. The counter c therefore has outputs of 25 line period from the first bistable and 25 line half-period from the second stage.

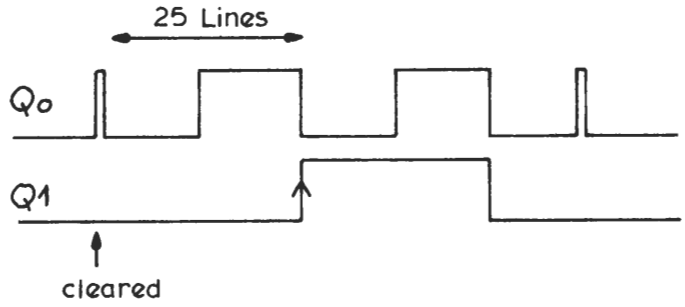

Fig. 4.3 Field Divider Third Stage Q0 and Q1 Outputs

The field inhibits are therefore generated by setting two bistables once per complete count of the divider. One is reset with an edge seven and a half lines later, and the other with an edge twenty-five lines later. Although these reset edges will occur several times in a complete count, they will be ignored until a set pulse occurs 20 ms later.

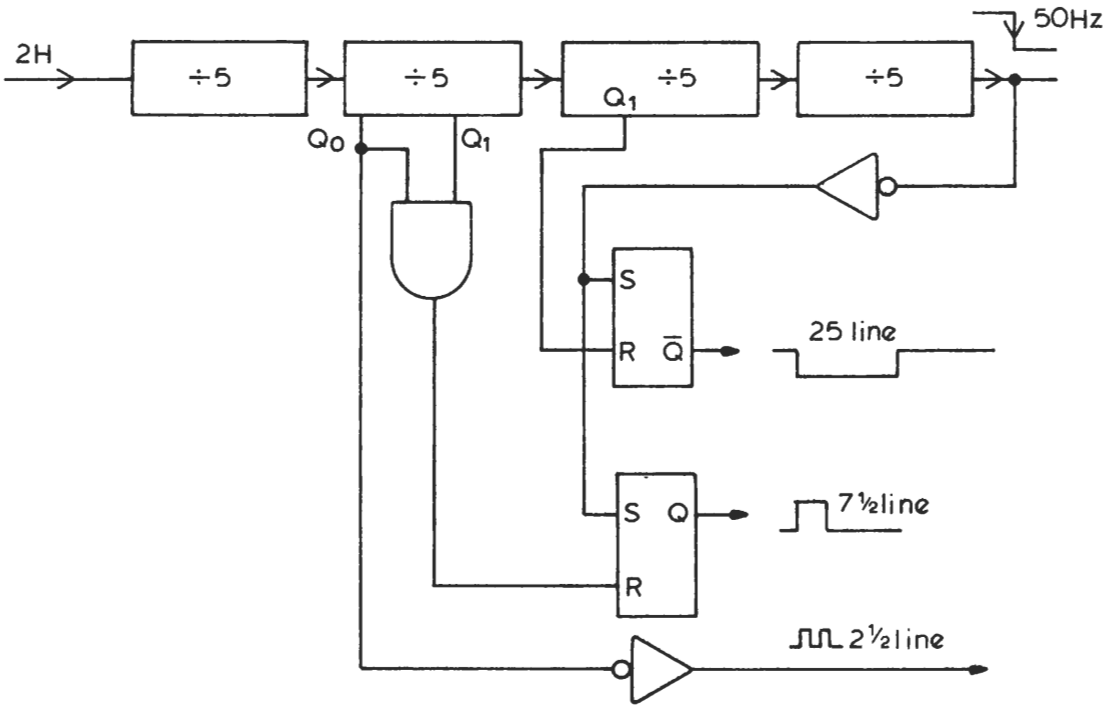

Fig. 4.4 Field Inhibit Waveform Generation

4.2 Preseltable Counter

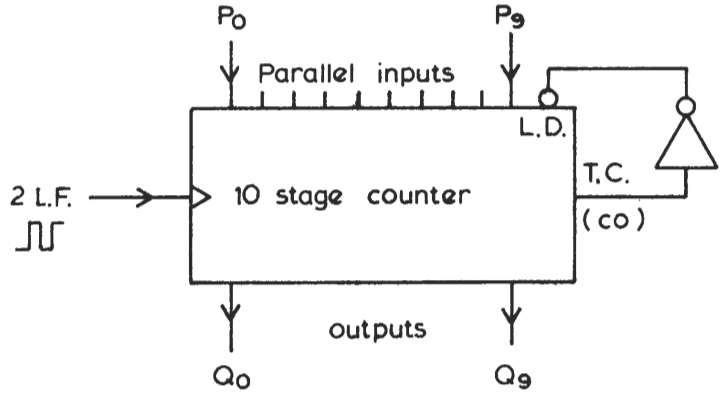

Fig. 4.5 Presettable ÷625 Counter

Here Po - Pq are parallel inputs hard-wired to decimal 399 in binary. The ten stage counter counts clock pulses to reach count 1023, all '1's on the outputs Qo - Q9. Terminal Count TC, (or Carry out, Co) then goes high and enables parallel load. In a synchronous counter parallel load takes place on the next clock pulse after PE is active. Thus the counter loads 399 and the carry out disappears. A futher 624 pulses are now required to re-enable the load, which itself takes 1 clock pulse.
The ÷625 action can be changed by ± counts in order to shorten or lengthen the field period for Variable Line Number Synchronising. This is done by changing the pre-load input, using control logic on the binary pre-load number.

5. P.A.L. V-Axis Switch and Burst Gate

5.1 V-Axis Switch (V.A.S.)

To alternate the polarity of the V signal in the coder on a line-by-line basis, the V.A.S. waveform is a square-wave at half-line frequency (7.8KHz.) The transitions should occur at the leading edge of line sync.
Leading edge triggers from the edge timing generator are inhibited to line frequency and fed to the clock input of a ÷2 circuit. The circuit and waveforms are show in Fig. 5.1.

SYNC GENERATION, PART II

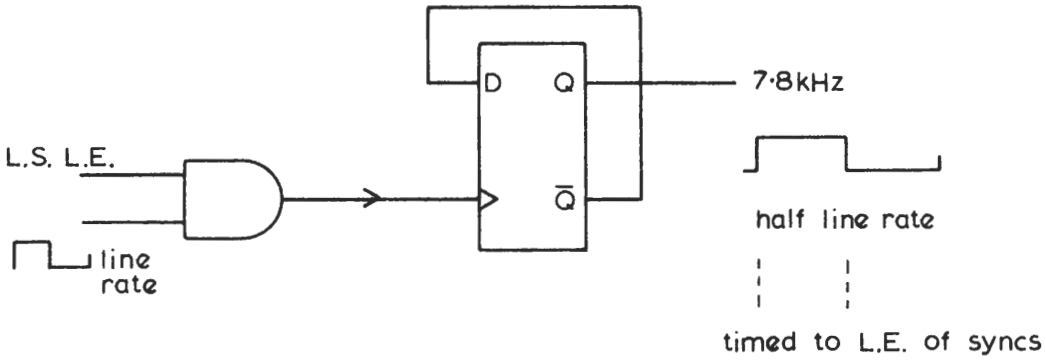

Fig. 5.1 V.A.S. Generation

5.2 Burst Gate

Burst gate is a line-rate waveform, using Leading Edge and Trailing Edge triggers positioned in back porch.

The burst must be blanked during the field sync interval - no good having bursts on the bottom of the broad pulses!

The burst is blanked over 9 lines, but the position of these 9 lines, relative to the field sync, changes in a sequence known as Bruch Blanking over 4 fields.

The object of Bruch Blanking is to ensure that the:

1) last burst before burst blanking, and

2) the first burst after, are both of the same phase, and correspond to +ve V.A.S. polarity.

A look at the field interval of fields 1-4 (Information sheet 44E) shows that burst blanking may be started as much as one and a half lines before the start of normal mixed blanking field component. (The last burst must occur on a complete line, not a half-line.)

A further waveform is generated from the field divider, to start one and a half lines ahead of the normal reset, and last for nine lines. This is then combined with V.A.S. to set a bistable to produce a Bruch Blanking pulse of 9-lines timed correctly on each field.

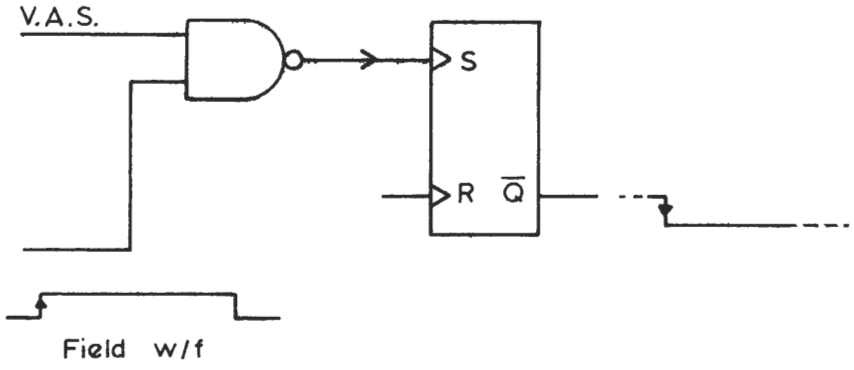

Fig. 5.2 Generation of Burst Blanking Start

The use of a NAND gate means that its output is tied high, until the field waveform goes high, gating through the VAS, but inverting it. The bistable is the edge triggered, and so at the end of a line with VAS high and field w/f active, a +ve edge will set the bistable, which will be used to inhibit B.G.L.E. pulses. When the 9-line field w/f relaxes to '0', the next line of +ve VAS polarity can have a burst, and the blanking bistable can be reset.
This is satisfied by gating the inverse of VAS with the inverse of the field w/f using a NAND to feed the +ve edge-triggered reset.

To recap, a 9-line field waveform is produced by the field divider, having a fixed relationship to the start of field pulses. This is re-timed by VAS so that a 9-line waveform is produced, such that the line before it and the line after it have positive VAS.

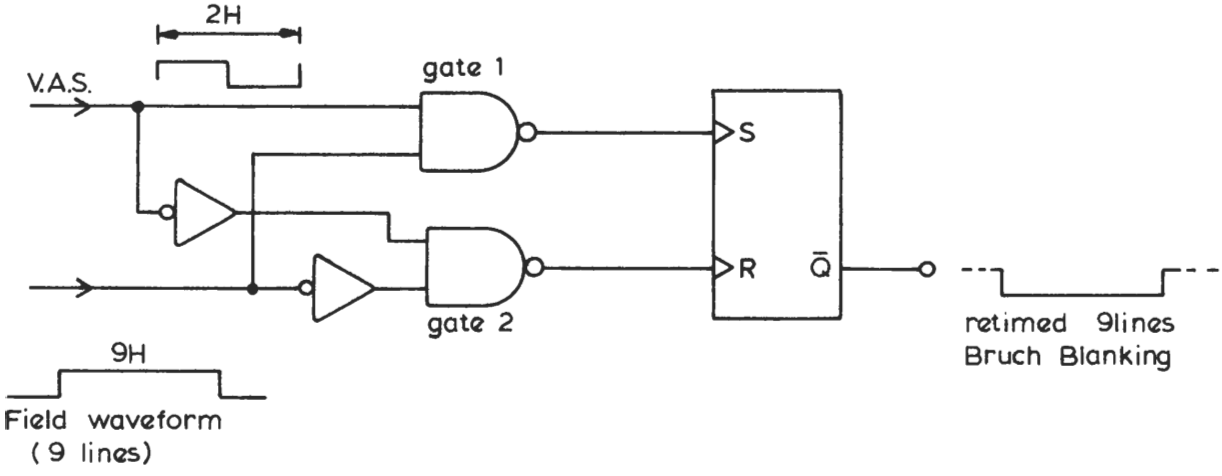

Fig. 5.3 Complete 9-line Inhibit Generator

SYNC PULSE GENERATION, PART II

This is shown in Fig. 5.4 for field 1 waveforms, and in Fig. 5.5 for field 3

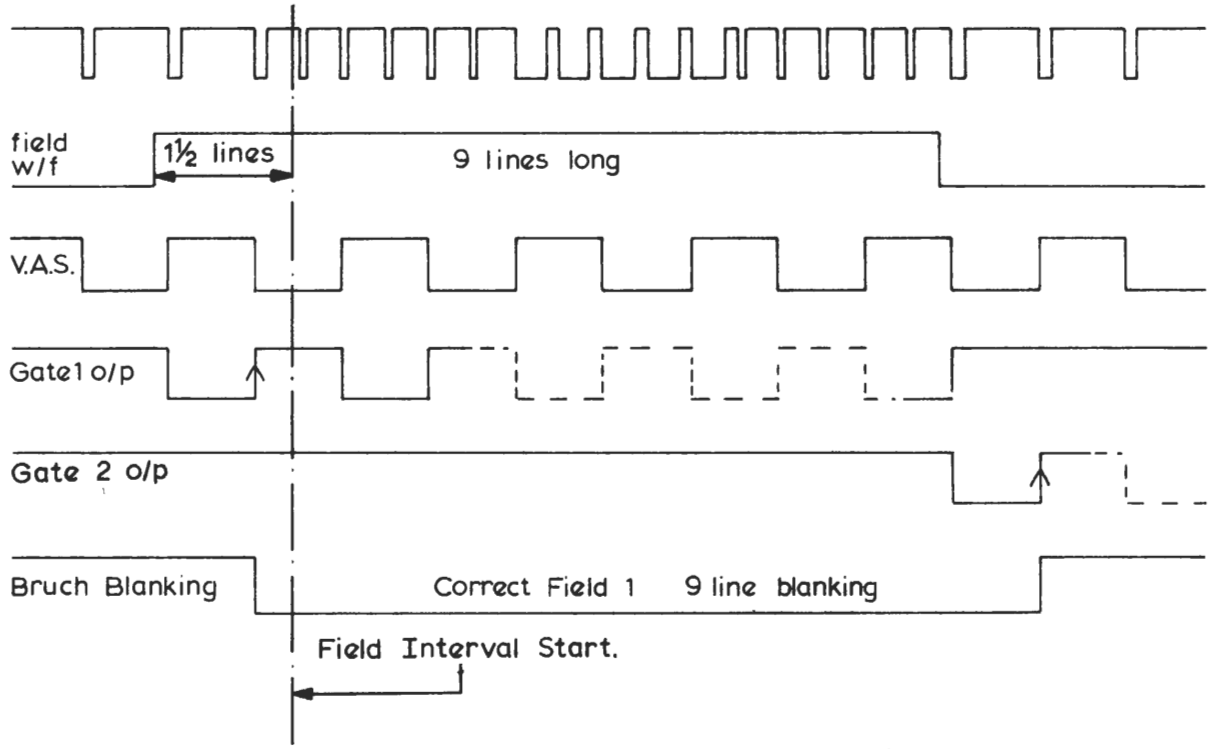

Fig. 5.4 Derivation of Bruch Blanking, Field 1

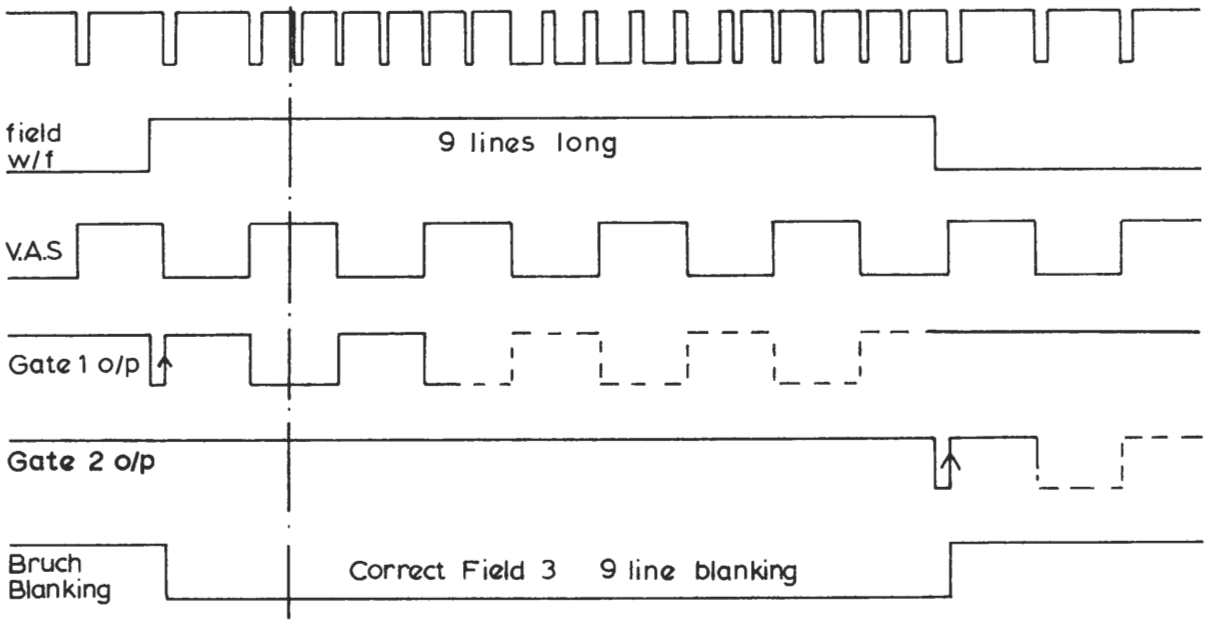

Fig. 5.5 Derivation of Bruch Blanking, Field 3

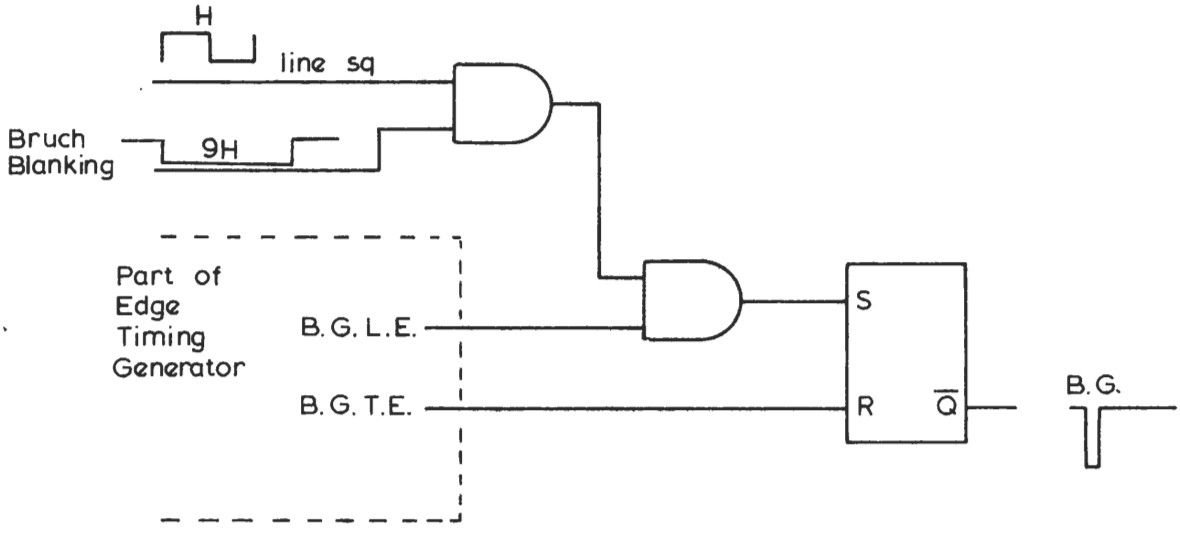

Fig. 5.6 Burst Gate Waveform

The Bruch Blanking is combined with the line frequency square wave to give the combined inhibit for burst gate leading edge pulses, as in fig. 5.6.

P.J. Harris/MG/SYNCGEN2

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