THE GENLOCK S.P.G.

INTRODUCTION

Many installations require sync pulse generators which can be synchronised to an external video signal as a timing reference (Genlock). This information sheet looks at the basic principles embodied in such a generator. As a conclusion the PAL eight field sequence is studied with particular reference to the need for sync pulse generators to match defined standards.

A convenient example of a generator embodying these features is the Seltech 110.

1. GENLOCK PRINCIPLES

The basic idea of genlock is shown in figure 1.1. A studio wishes to make an incoming contribution synchronous. Synchronism can be achieved by referencing the sync pulse generator supplying the studio to the contribution. Similar arrangements apply in respect of colour black installations, where each area in a studio complex has its own sync generator. A reference signal (usually black and burst) is distributed to all the generators to maintain synchronism between them.

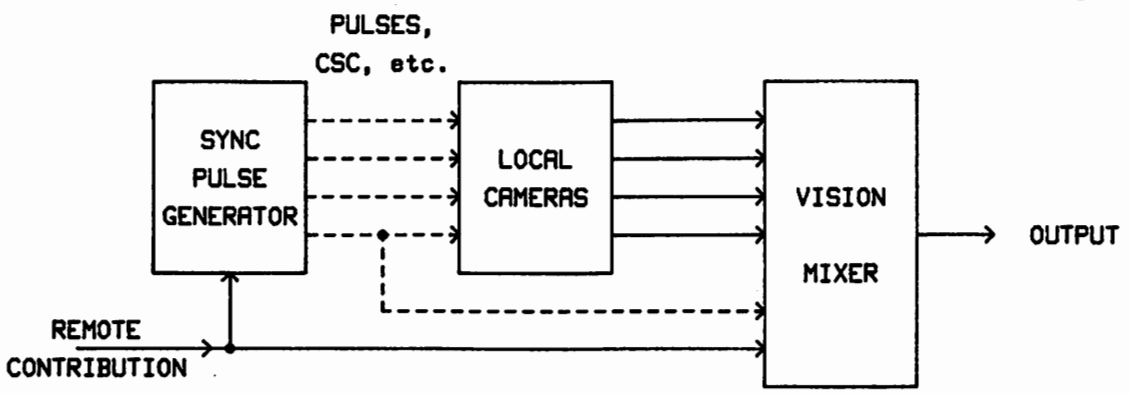

Figure 1.1: Basic Genlock Arrangement

1.1 Horizontal Timing Delays

Figure 1.1. shows the basic principle of genlock but takes no account of the delays exhibited by the various cable paths. In a typical installation there will be a delay between the sync generator outputs and the mixer inputs. Figure 1.2 shows one possible condition.

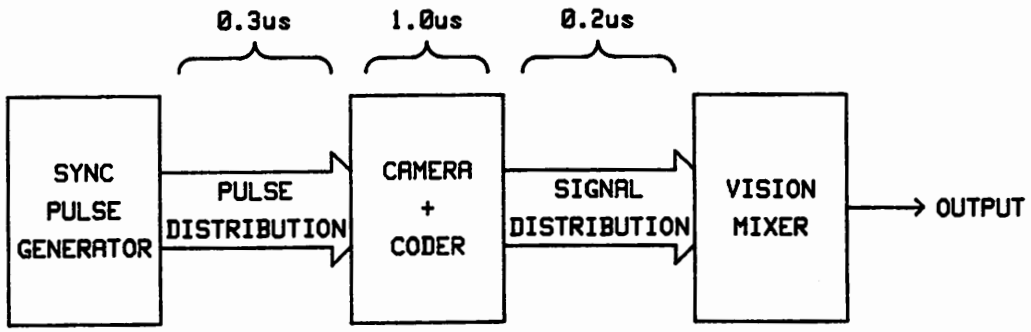

Figure 1.2: Timing Delays in Studio Installation

In the example of figure 1.2 there is a total delay of 1.5µs between the output of the sync generator and the input to the vision mixer. This doesn't matter if the studio stands alone, but consider the genlock case. Let's first of all take a look at the basic genlock s.p.g.

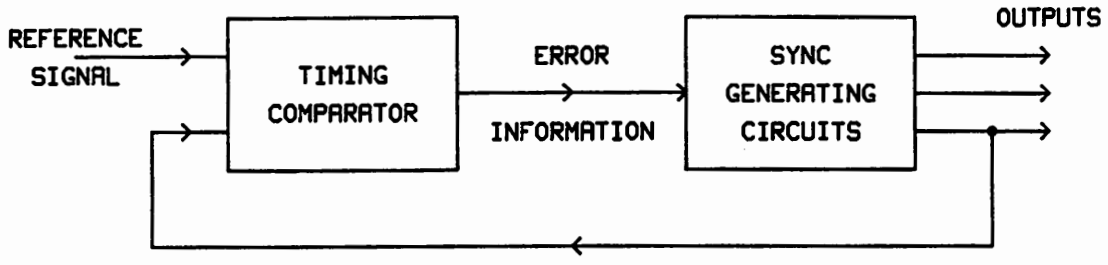

Figure 1.3: Simple Genlock S.P.G.

Figure 1.3 represents a simple sync pulse generator with a genlock capability. Suitable outputs from the generator are compared with the corresponding components of the input reference in a timing comparator. Error information from the timing comparator causes the

sync generating circuits to modify the timing of the output waveforms so that they match the reference. When the steady state condition is reached there will be no difference in timing between the reference signal and the spg outputs.

If we now relate this to the example of figure 1.2 a problem is revealed. SPG outputs and remote contribution timings will coincide. The local sources do not arrive at the mixer until 1.5µs later however. Even allowing for some delay to the remote signal in the distribution system between spg and mixer it will arrive well in advance of the local sources. There are two possible solutions - delay the remote source into the mixer or advance the spg outputs relative to it. The latter course is inevitably chosen as, apart from not requiring expensive, wideband, delays, it can be much more flexible.

1.2 Horizontal Timing Offsets

The problem therefore is how to offset the timing of the spg from its reference. Consider the example of figure 1.4.

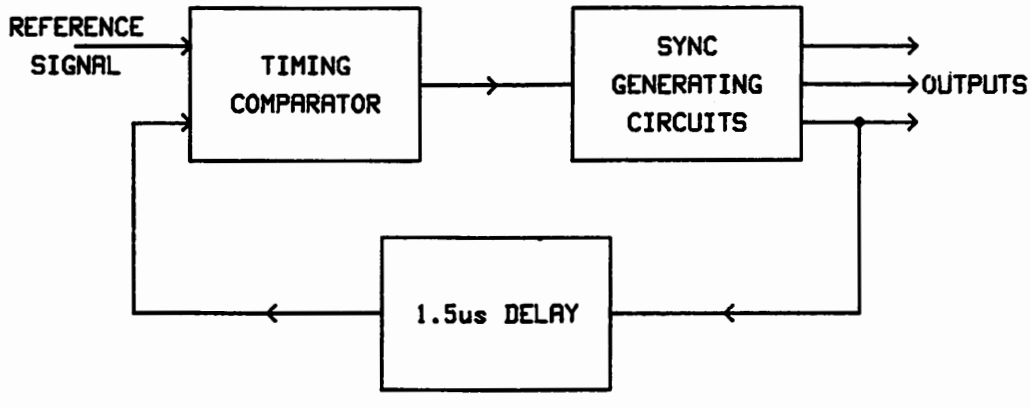

Figure 1.4: Genlock SPG Modified to Introduce Timing Offset

In this example the feedback loop has been modified to include a delay of 1.5μs. The comparator will cause the spg to change its timing until there is no difference between the comparator inputs. The spg output was delayed by 1.5μs however before it was connected to the comparator. This means that the spg outputs are being produced 1.5μs earlier than the reference. Figure 1.5 shows another example.

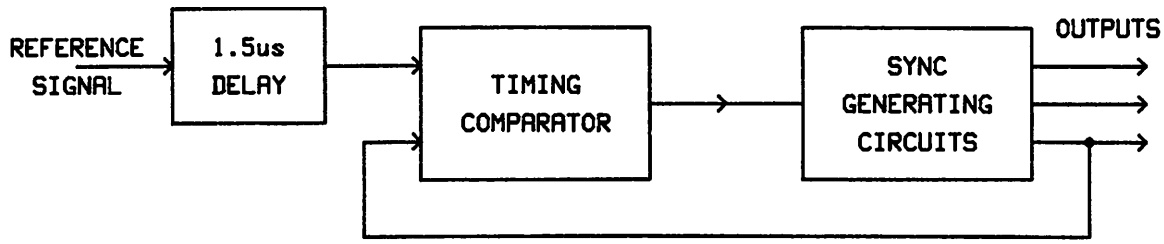

Figure 1.5: Genlock SPG with Delayed Outputs

In figure 1.5 the 1.5μs delay has been placed in the reference path. The spg is thus effectively being locked to a signal 1.5μs later than the reference, its outputs will also be produced 1.5μs later.

So, a delay in the feedback path advances the timing, delay in the reference retards it. For maximum flexibility timing advance or retard may be required. Figure 1.6 shows how this can be achieved.

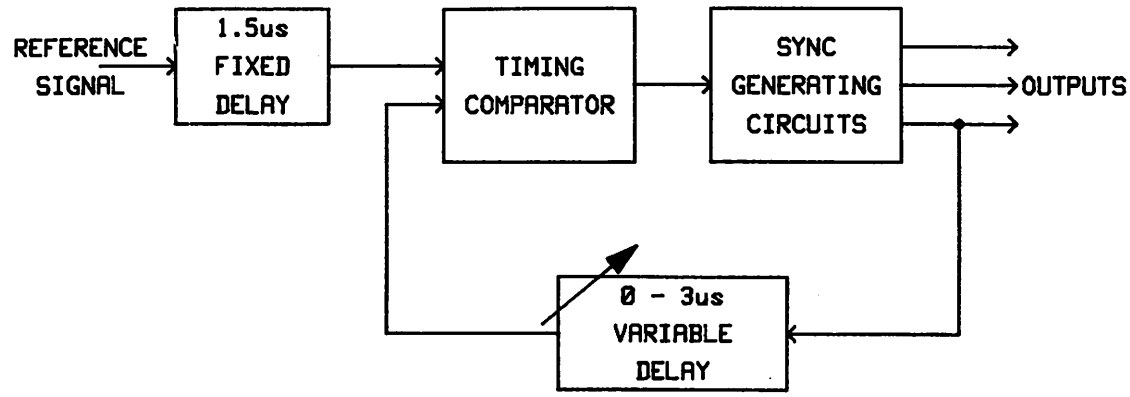

Figure 1.6: Genlock SPG with Adjustable Output Timing

If the variable delay is set to 1.5μs then both reference and feedback paths have been delayed by the same amount. The generator outputs are therefore time coincident with those of the reference. Reducing the variable delay effectively delays the reference relative to the feedback path, the output timing is retarded. Increasing the feedback delay similarly causes the output timings to be advanced.

Note that as an alternative to delaying the reference, output timing delay can be achieved by providing an early timed output for feedback to the comparator.

1.3 Practical Horizontal Delay Circuits

The genlock spg described requires an output signal, with adjustable timing, which can be fed back to the comparator for comparison with the input signal. The timing should be capable of advancing or delaying the feedback signal to the comparator in order to delay or advance the spg outputs relative to the reference.

Fortunately the spg, by its very nature, includes suitable delay stages in the form of the edge timing generator. Feedback signals can be picked off at the appropriate times to generate the offset required. If continuous variation is required a ramp and sample delay circuit can be included. Figure 1.7 shows this.

THE GENLOCK SPG

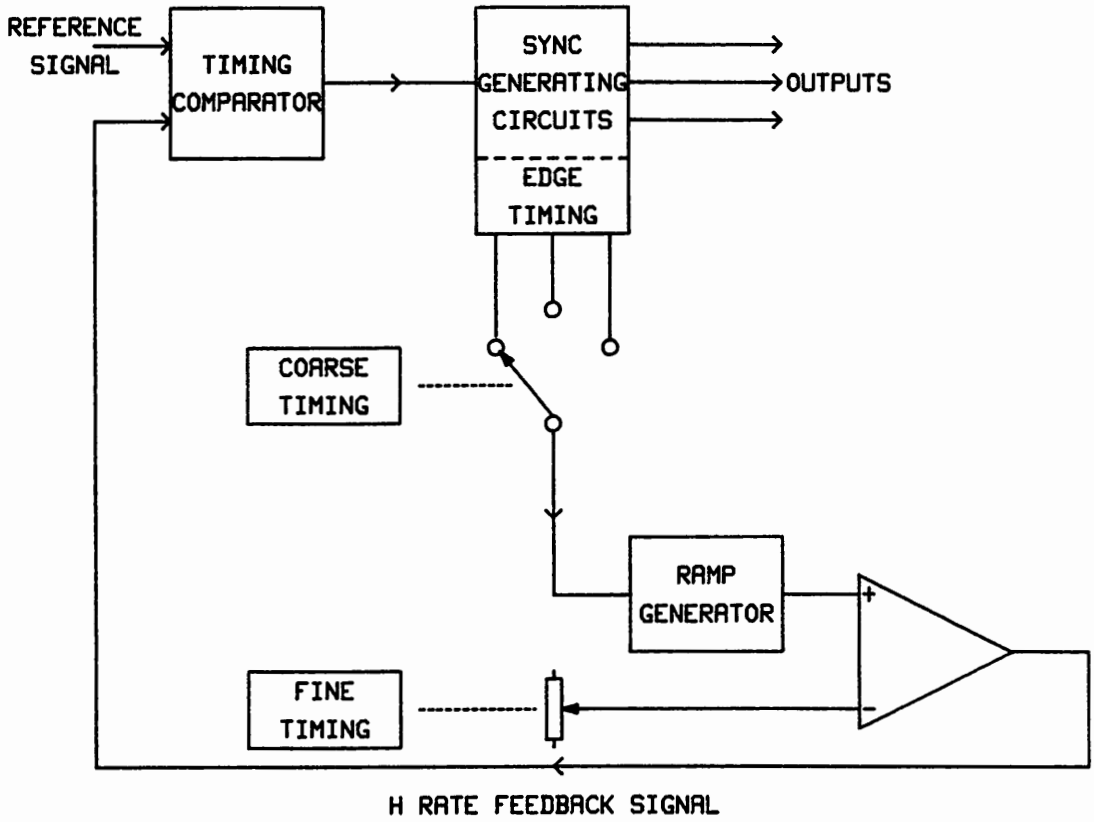

Figure 1.7: Genlock SPG

The Seltech offers eight coarse timing steps of 2.25µs covering 2.25µs output delay to 15.75µs advance. The variable delay stage modifies this so that a continuously variable delay adjustable from 3µs delay to 15µs advance is available.

2. METHODS OF ACHIEVING SYNCHRONISM

The preceding sections which have discussed the means whereby timing offsets can be introduced have assumed one basic fact, that the spg outputs can be synchronised to the reference. This section looks at the way in which synchronism can be achieved.

2.1 Colour Subcarrier Lock

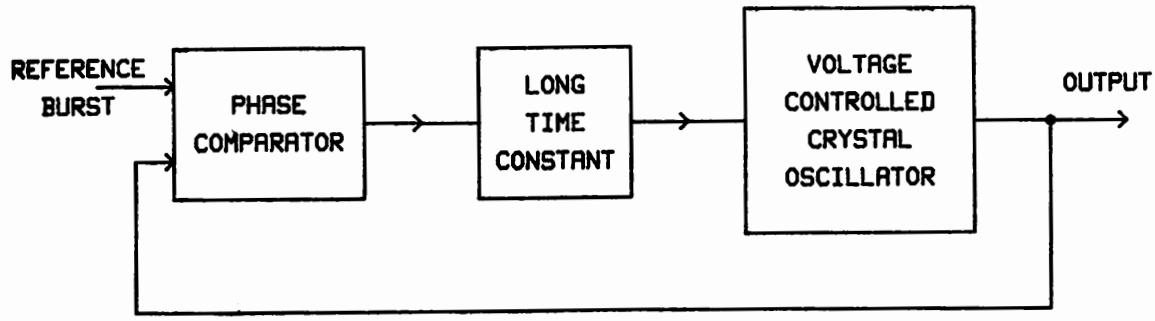

Figure 2.1: Colour Phase Lock

The bursts separated from the genlock video are phase compared with the genlock spg's subcarrier oscillator and a lock achieved with a long time constant to reject the burst 90° phase change on alternate lines; (as in a PAL colour decoder). As with the decoder, a shorter time constant output is used to regenerate the VAS sequence of the remote bursts.

In the case of the Seltech 110 the phase comparator controls the 4 x CSC subcarrier oscillator. The feedback path is taken from the output ÷ 4 circuit, but independent of the phase shifting circuitry. This gives 360° adjustment of the subcarrier as generated relative to the reference. Figure 2.2 shows this.

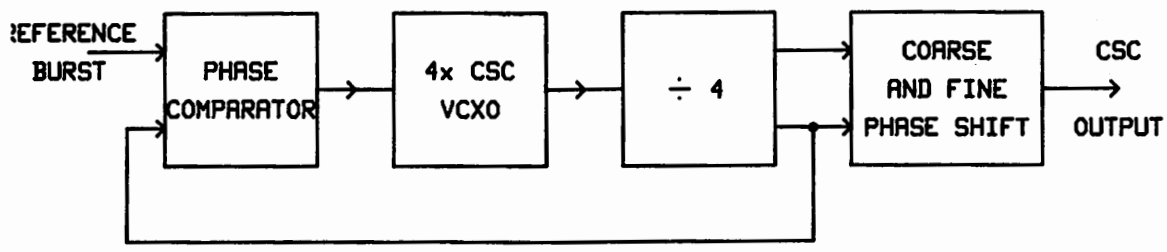

Figure 2.2: Seltech 110 Subcarrier Locking

2.2 Line Lock

Line and field rate spg outputs are derived from a 2H clock. This can be supplied by a phase-locked loop, which is used to lock the spg line rate outputs to the incoming H syncs of the genlock video.

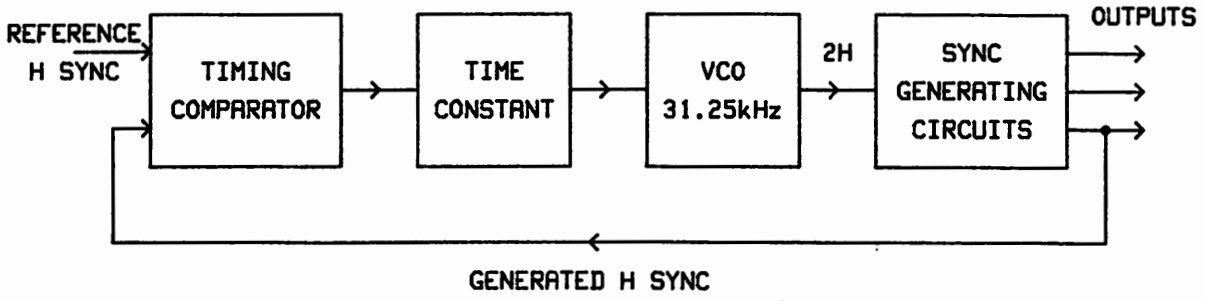

Figure 2.3: Phase Locked Loop for Line Timing

In the Seltech spg two horizontal locking modes are possible - digital and AFC. In the AFC mode the 2H source is basically a VCO and locks directly to the line frequency of the incoming source.

In the digital mode the 2H signal is derived from the 4 x CSC oscillator via the 100Hz offset removing stage. The frequency of the offset generator is changed under the control of the timing comparator. A small increase in the offset frequency causes the output timing to retard (2H goes down) whilst a small decrease causes timing advance. Once zero error is detected within the limits of the timing comparator window (less than 10ns) horizontal correction effectively stops. Synchronism is maintained via the subcarrier locking loop, from which the 2H is ultimately derived.

For digital locking to succeed the CSC - H relationship of the input signal must be standard PAL. If this is not so, or the input signal is monochrome, the AFC mode must be used. Using the AFC mode with standard PAL sources does work, of course, but the output timing jitter is much increased compared to the digital mode.

Once this loop is locked, the line phase and frequency is matched to the remote video, and therefore the field frequency is matched. (Generated by the same 2H clock). Since there is no telling which line number of the remote video is locked to a particular line of the generator o/p, the field phase still needs correcting.

2.3 Field Timing Correction

The basic technique used is to compare reference and generator vertical timing. Any difference causes the field divider to miscount, generating either more or less lines per field than usual until coincidence is detected. Figure 2.4 shows this.

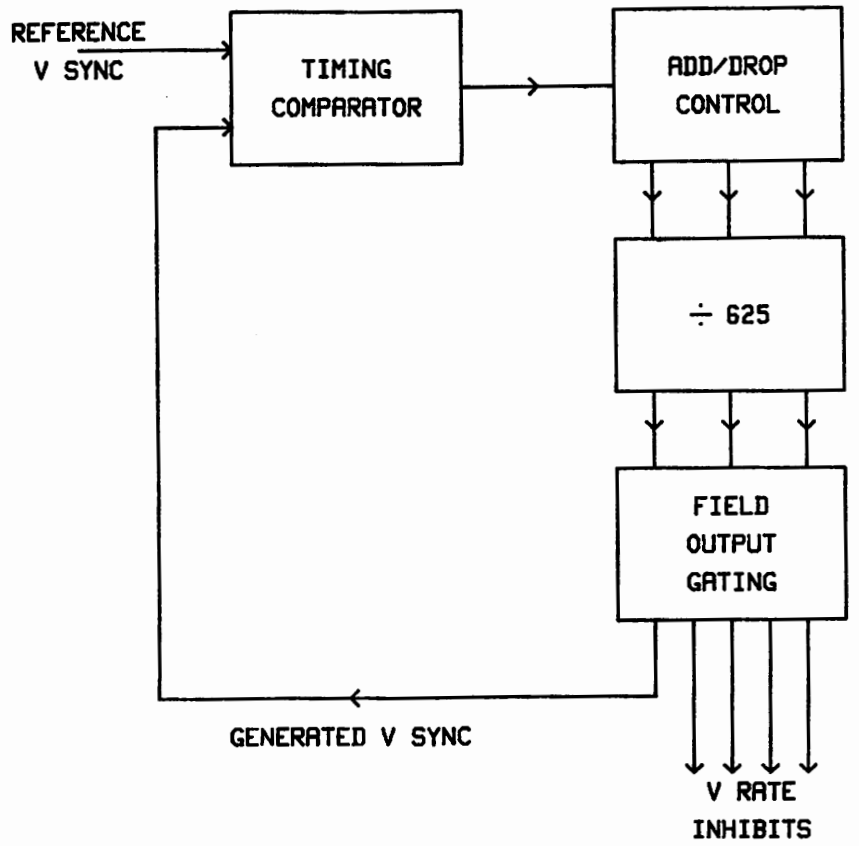

Figure 2.4: Vertical Sync Locking

If the field divider count ratio is changed to ÷627, the time to the next generated field interval will increase by one line. The generated field interval will retard by one line/field relative to the field period on the input video.

Change to ÷623, and the generator field period advances by 1 line per field.

The field timing comparator causes a change in division ratio if an error in field phasing exists when the line timing has been locked.

2.4 Speed of Timing Correction

The time constant of lock for both the CSC and line timing oscillators can be of the order of a few lines, or tens of lines, so that both lock very quickly after a non-sync cut in the genlock video. The rate of field lock should be slowed down to an acceptable rate for the following reasons:-

a. Monitor and receiver field timebases are often driven by a crudely synchronised oscillator. If the input signal suffers a sudden large change in field sync timing, the oscillator will free-run at its natural frequency until its output phase is close to the new field sync pulse, then lock will occur.

   The period of free running causes a 'field roll' which is disturbing to the viewer.

b. Mechanical devices such as TK and VT are usually servo-locked to the television field component. A jump change in field phase of the VT reference could cause older servos to completely unlock, taking more time to re-phase and stabilise during which time the output was unusable.

For both these reasons, a controlled slewing of the generator output field phase was desirable, at a rate which timebases and servos could follow without losing lock.

2.5 Practical Field Divider Division Changes

The rate of field correction depends on the number of lines/field by which the field divider is allowed to miscount.

a. ±1 count per field (±0.5 line/field). The position of field syncs relative to line syncs is advanced or retarded by 0.5 a line per field, each field, until lock is achieved. Maximum error needing correction ±0.5 field, i.e. 150 lines at 0.5 line per field ≡ 6 seconds. During correction each field length is an integral number of lines, ie 312 or 313, therefore interlace is lost.

b. ± 2 counts per field (± 1 line per field). Field sync stepped by ± 1 line per field until lock occurs. Maximum error 312 lines - correction time still 6 seconds. Interlace is maintained since each field is still n + 0.5 lines long.

Neither of these methods take account of the 4 field PAL colour sequence involving VAS. Generators using this method apply a sudden reset to VAS to invert its phase if the four field sequence is 180° out when field lock is achieved. This may cause a colour flash under certain conditions.

c. ± 4 counts - ± 2 lines per field.
This method can be used so that the VAS sequence does not have to be disturbed - a field 1 is followed by a field 2 etc. - but therefore the maximum error may be up to 624 lines, still taking 6 seconds to correct.

A consequence of correcting by 2 lines/field is that the local and remote VAS must already be matched. The solution is to lock the line timing (section 2.2) using a comparison of local and remote VAS, thus giving a two-line lock before field correction occurs.

In the case of the Seltech 110 0.5 line/field correction is used. No account of VAS polarity is taken by either horizontal or vertical locking loops. Local VAS polarity is compared with the incoming burst, and shouold it be incorrect a reset signal reverses the local VAS polarity. This method does cause problems however, as many monitors and receivers cannot cope with this rapid change in chroma phase and exhibit colour flashing.

3. PAL EIGHT FIELD SEQUENCE

Earlier we studied methods of ensuring that the CSC-H relationship was correct. The methods discussed only took account of the frequency relationship however. What was not done was to pay any attention to the phase relationsip between CSC and horizontal timing.

One reason is that until comparatively recently no standard existed for the eight field relationship. The EBU has now adopted a standard, which compares the phase of the U axis subcarrier to the leading edge timing of H sync. Colour field one is defined as the field where a positive going zero crossing of the subcarrier is time coincident with the field sync datum for field one. Figure 3.1 shows this.

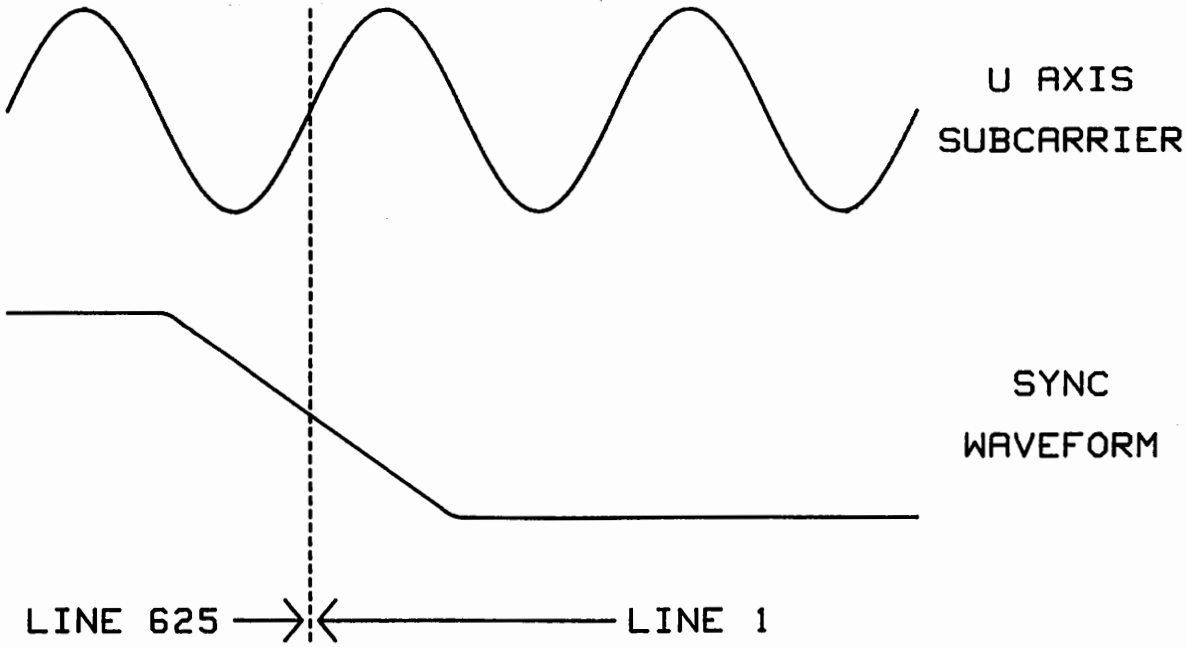

Figure 3.1: CSC-H Relationship at Start of Colour Field 1

BBC designed SPG's have never taken account of this type of relationship, however much effort has been put into it by the commercial world. A guaranteed eight field sequence does assist in VT editing, particularly so when animation sequences are involved. The majority of facilities house work is often involved in animation, with the preparation of adverts, commercials etc.

3.1 Guaranteeing the Eight-Field Sequence - Master SPG's

An spg designed for use as the master in a studio installation should include circuitry designed to guarantee the eight field sequence on switch on. Additionally it would generally use a high stability oscillator for minimum subcarrier drift.

To correct the CSC-H relationship the subcarrier phase is compared with H sync edge timing. The Seltech 110 uses a D-Type for this, and examines the CSC-H phase on certain lines during what is intended to be colour field one. The error signals drived are used to control the horizontal timing via the horizontal correction loop, i.e. by changing the offset frequency. Figure 3.2 shows this in simple terms.

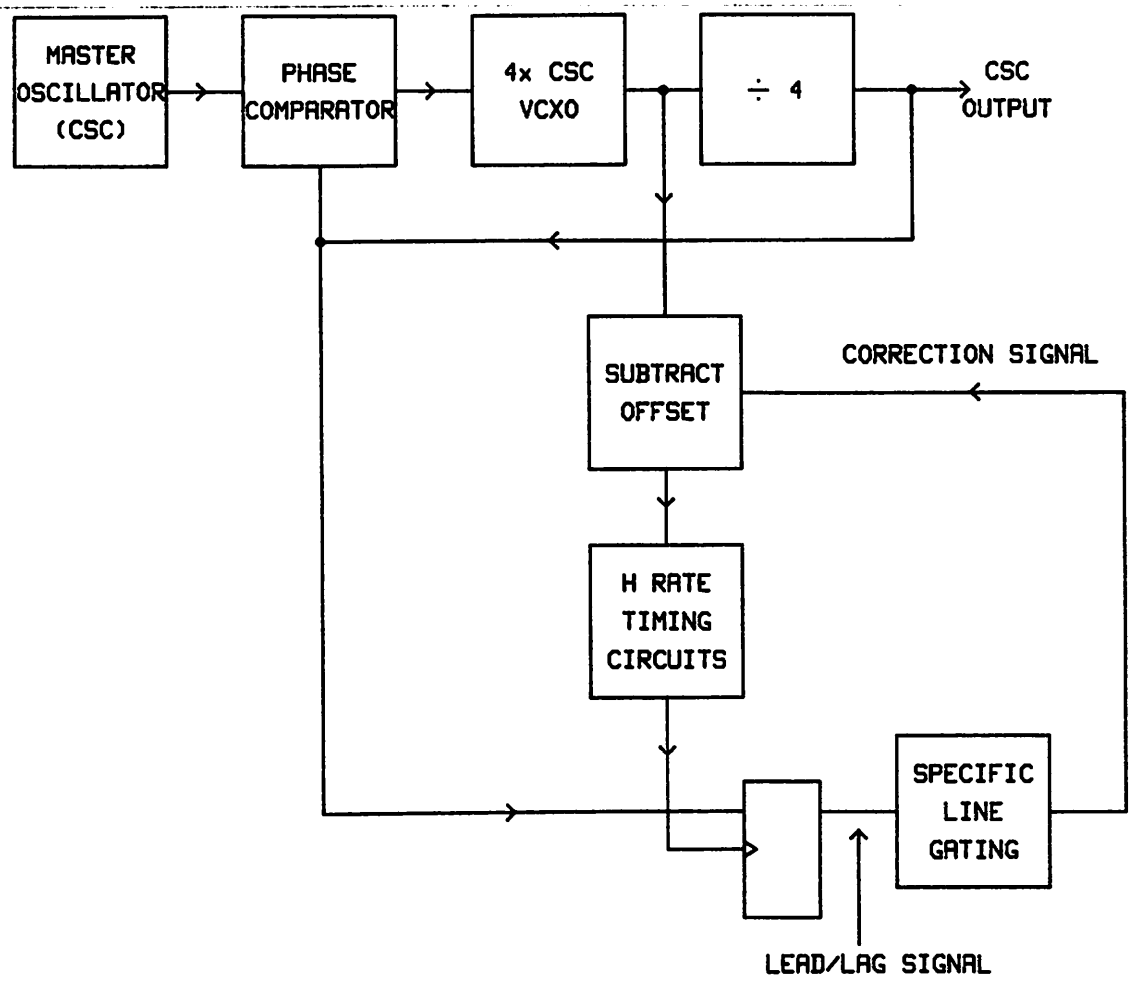

Figure 3.2: CSC-H Correction in the Seltech 110

3.2 Slave SPG Arrangements

It might be thought that once an spg is referenced to a signal with guaranteed CSC-H then its outputs too would meet such specifications. This is not so however. There will be a tolerance window within which the horizontal locking loop will declare the H components to be synchronous, similarly for CSC. If the H comparator deadspace is, say, ±50ns then an error in the CSC-H relationship of up to ±90° could exist.

The Seltech affords a means of preventing this. The correction circuitry also drives LED indicators which show the CSC-H state. Both are on when the relationship is correct. An error in CSC-H phase is corrected by

manually offsetting the horizontal phasing control which determines the timing of the horizontal rate outputs relative to the reference. The LED's even tell you which way to turn the pot! (Why can't the spg automatically correct the CSC-H relationship when genlocked?)

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28th June 1984